

**PowerMOS transistor  
Logic level FET**

**BUK542-100A/B**

**GENERAL DESCRIPTION**

N-channel enhancement mode logic level field-effect power transistor in a plastic full-pack envelope.  
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

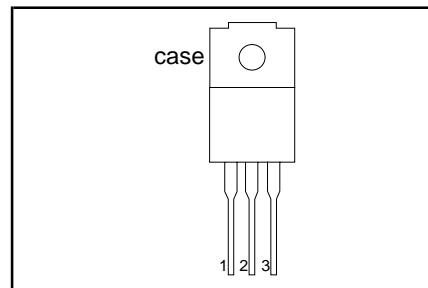
**QUICK REFERENCE DATA**

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	<b>BUK542</b>			
$V_{DS}$	Drain-source voltage	-100A 100	-100B 100	V
$I_D$	Drain current (DC)	6.3	5.6	A
$P_{tot}$	Total power dissipation	22	22	W
$R_{DS(ON)}$	Drain-source on-state resistance; $V_{GS} = 5\text{ V}$	0.28	0.35	$\Omega$

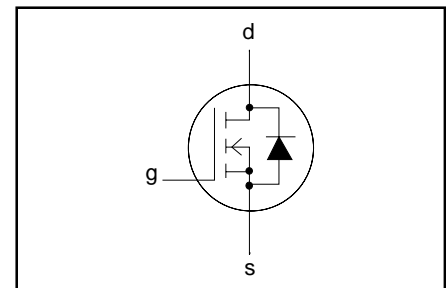
**PINNING - SOT186**

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

**PIN CONFIGURATION**



**SYMBOL**



**LIMITING VALUES**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	Drain-source voltage	-	-	100	V
$V_{DGR}$	Drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50\ \mu\text{s}$	-	20	V
$I_D$	Drain current (DC)	$T_{hs} = 25\text{ }^\circ\text{C}$	-	-100A 6.3	A
$I_D$	Drain current (DC)	$T_{hs} = 100\text{ }^\circ\text{C}$	-	4	A
$I_{DM}$	Drain current (pulse peak value)	$T_{hs} = 25\text{ }^\circ\text{C}$	-	25	A
$P_{tot}$	Total power dissipation	$T_{hs} = 25\text{ }^\circ\text{C}$	-	22	W
$T_{stg}$	Storage temperature	-	-55	150	$^\circ\text{C}$
$T_j$	Junction Temperature	-	-	150	$^\circ\text{C}$

**THERMAL RESISTANCES**

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	5.68	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient		-	55	-	K/W

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### STATIC CHARACTERISTICS

 $T_{hs} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.25\text{ mA}$	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 1\text{ mA}$	1.0	1.5	2.0	V
$I_{DSS}$	Zero gate voltage drain current	$V_{DS} = 100\text{ V}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^{\circ}\text{C}$	-	1	10	$\mu\text{A}$
$I_{DSS}$	Zero gate voltage drain current	$V_{DS} = 100\text{ V}; V_{GS} = 0\text{ V}; T_j = 125\text{ }^{\circ}\text{C}$	-	0.1	1.0	mA
$I_{GSS}$	Gate source leakage current	$V_{GS} = \pm 15\text{ V}; V_{DS} = 0\text{ V}$	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 5\text{ V}; I_D = 5.5\text{ A}$	-	0.25	0.28	$\Omega$
		<b>BUK542-100A</b>	-	0.3	0.35	$\Omega$
		<b>BUK542-100B</b>	-			

### DYNAMIC CHARACTERISTICS

 $T_{hs} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$g_{fs}$	Forward transconductance	$V_{DS} = 25\text{ V}; I_D = 5.5\text{ A}$	4.5	6	-	S
$C_{iss}$	Input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}$	-	400	600	pF
$C_{oss}$	Output capacitance		-	90	120	pF
$C_{rss}$	Feedback capacitance		-	35	50	pF
$t_{don}$	Turn-on delay time	$V_{DD} = 30\text{ V}; I_D = 3\text{ A};$	-	12	18	ns
$t_r$	Turn-on rise time	$V_{GS} = 5\text{ V}; R_{GS} = 50\text{ }\Omega;$	-	45	70	ns
$t_{doff}$	Turn-off delay time	$R_{gen} = 50\text{ }\Omega$	-	50	70	ns
$t_f$	Turn-off fall time		-	30	45	ns
$L_d$	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
$L_s$	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

### ISOLATION LIMITING VALUE & CHARACTERISTIC

 $T_{hs} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{isol}$	Repetitive peak voltage from all three terminals to external heatsink	R.H. $\leq 65\%$ ; clean and dustfree	-		1500	V
$C_{isol}$	Capacitance from T2 to external heatsink	$f = 1\text{ MHz}$	-	12	-	pF

### REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

 $T_{hs} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{DR}$	Continuous reverse drain current	-	-	-	6.3	A
$I_{DRM}$	Pulsed reverse drain current	-	-	-	25	A
$V_{SD}$	Diode forward voltage	$I_F = 6.3\text{ A}; V_{GS} = 0\text{ V}$	-	1.2	1.5	V
$t_{rr}$	Reverse recovery time	$I_F = 6.3\text{ A}; -di_F/dt = 100\text{ A}/\mu\text{s};$	-	80	-	ns
$Q_{rr}$	Reverse recovery charge	$V_{GS} = 0\text{ V}; V_R = 30\text{ V}$	-	0.30	-	$\mu\text{C}$

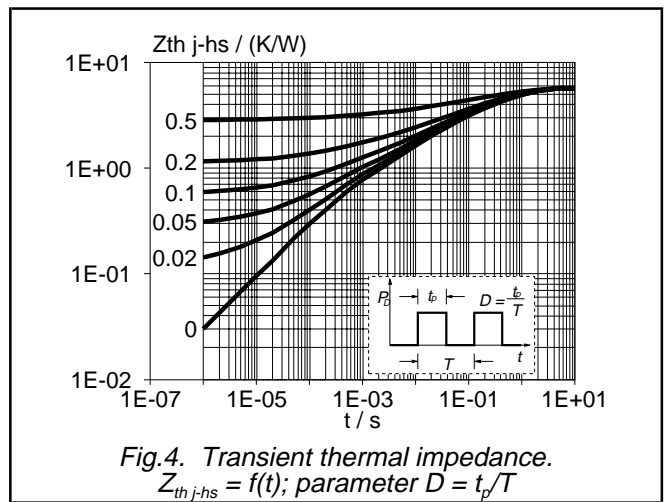
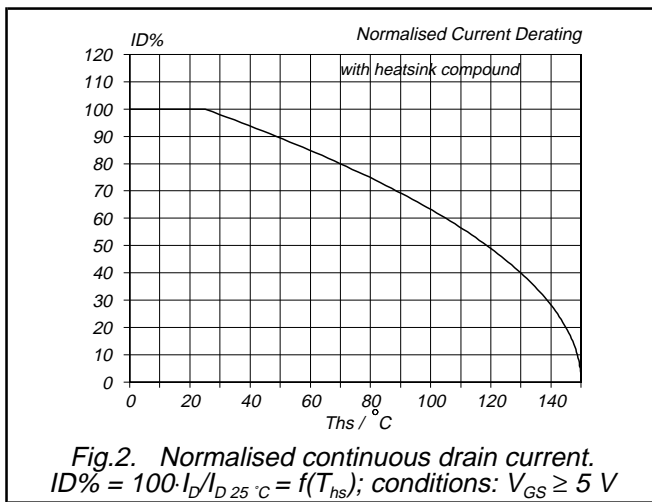
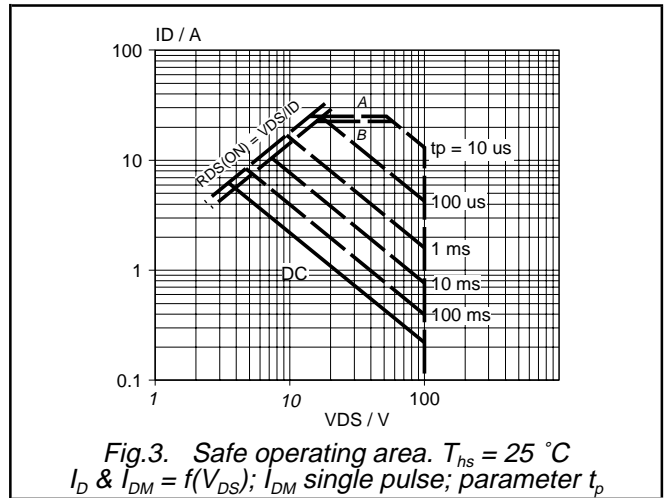
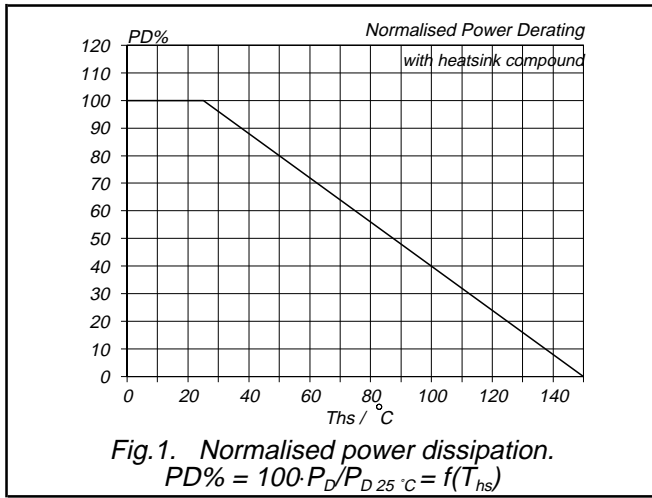
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**AVALANCHE LIMITING VALUE**

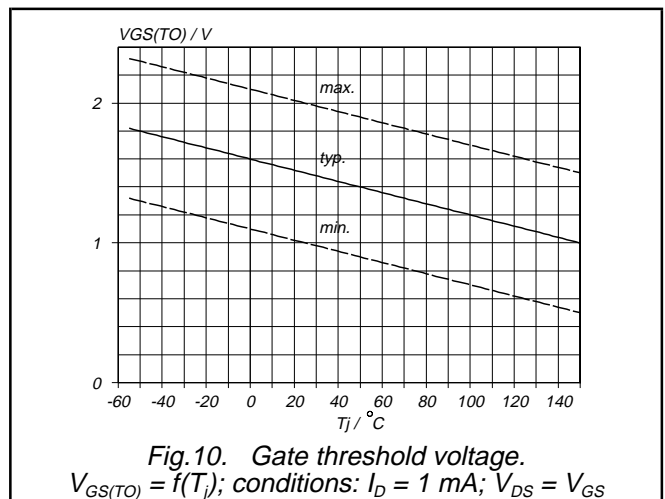
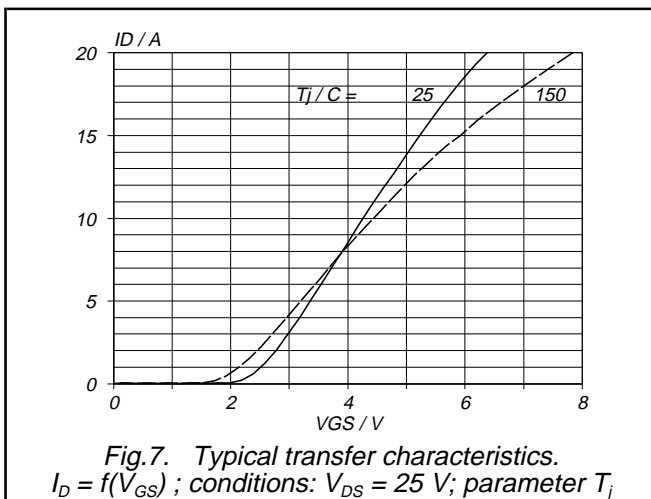
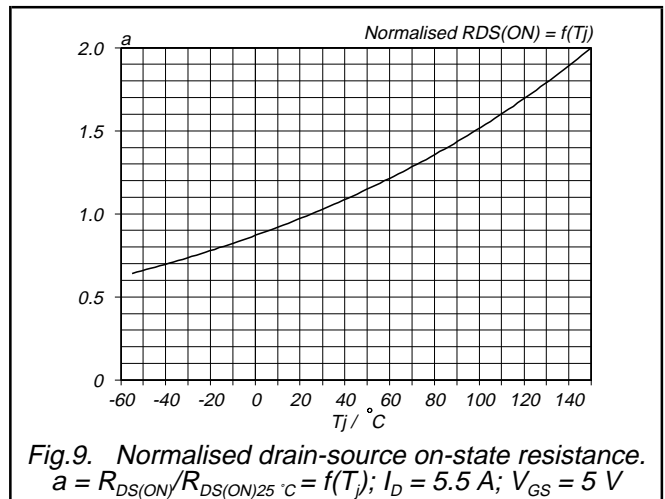
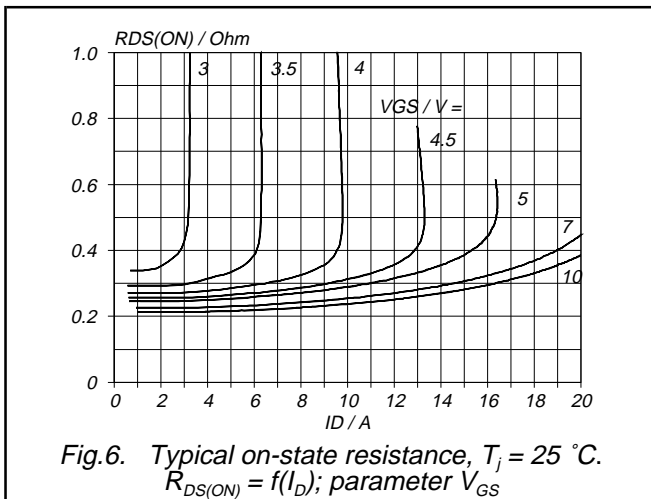
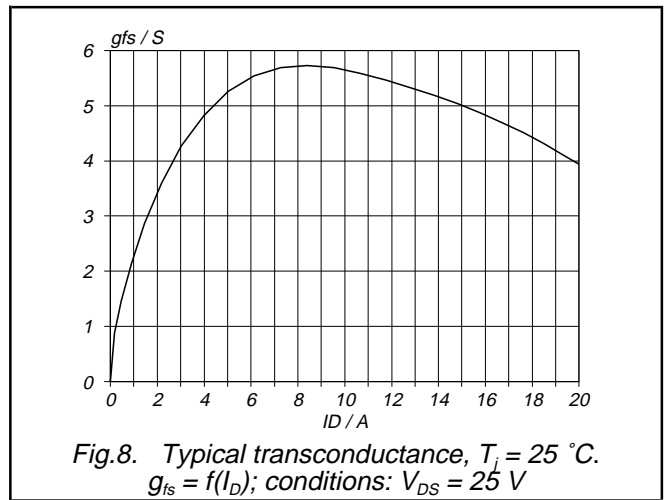
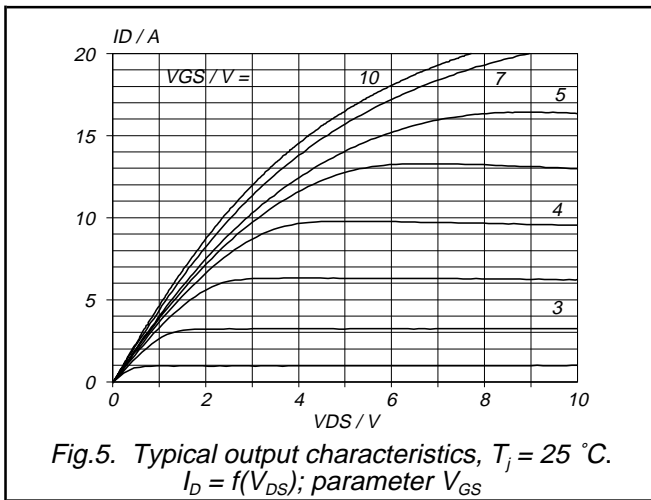
$T_{hs} = 25\text{ }^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$W_{DSS}$	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D = 10\text{ A}$ ; $V_{DD} \leq 50\text{ V}$ ; $V_{GS} = 5\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$	-	-	30	mJ



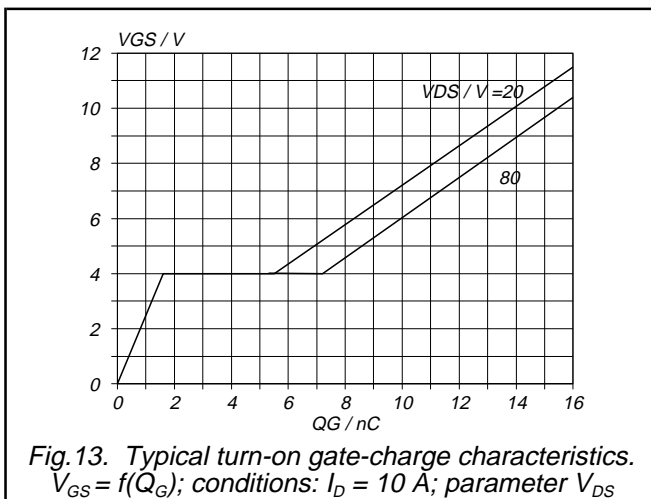
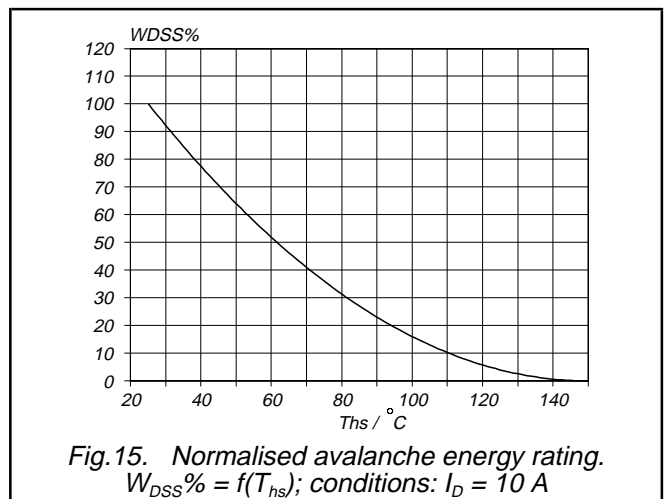
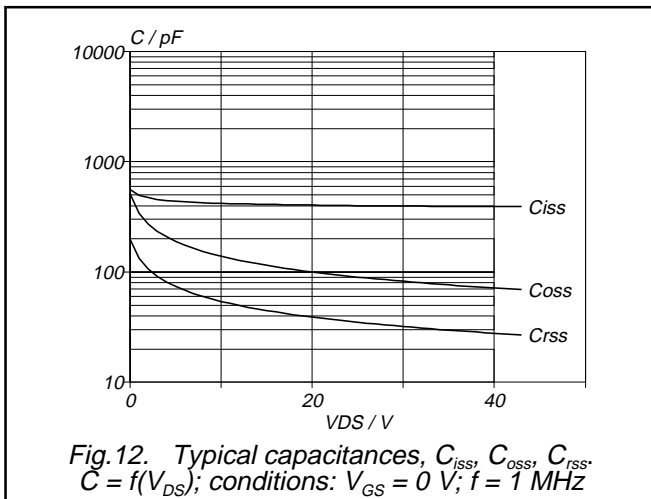
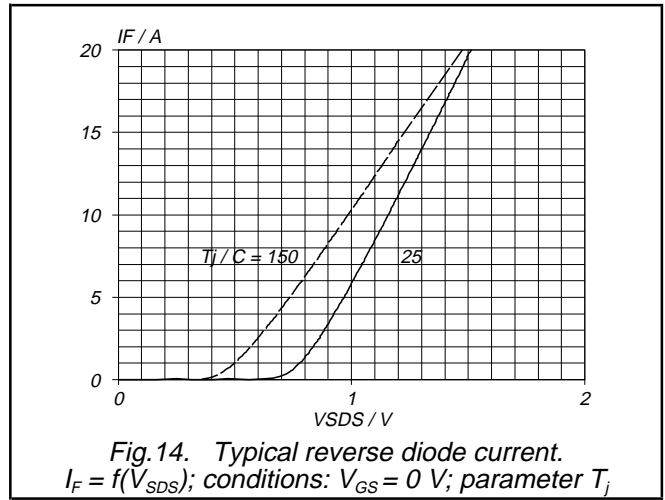
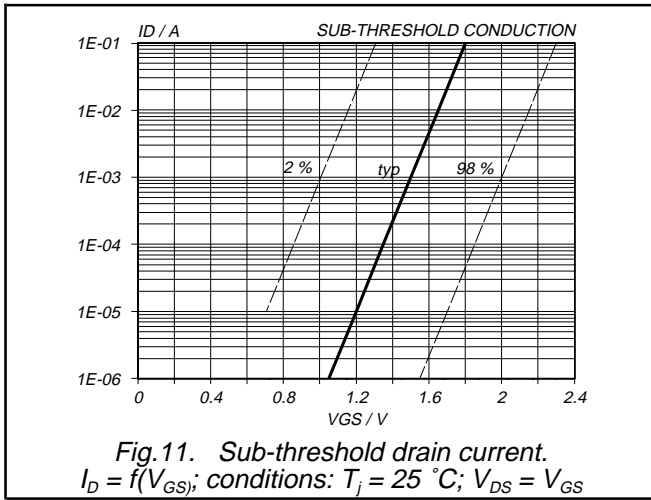
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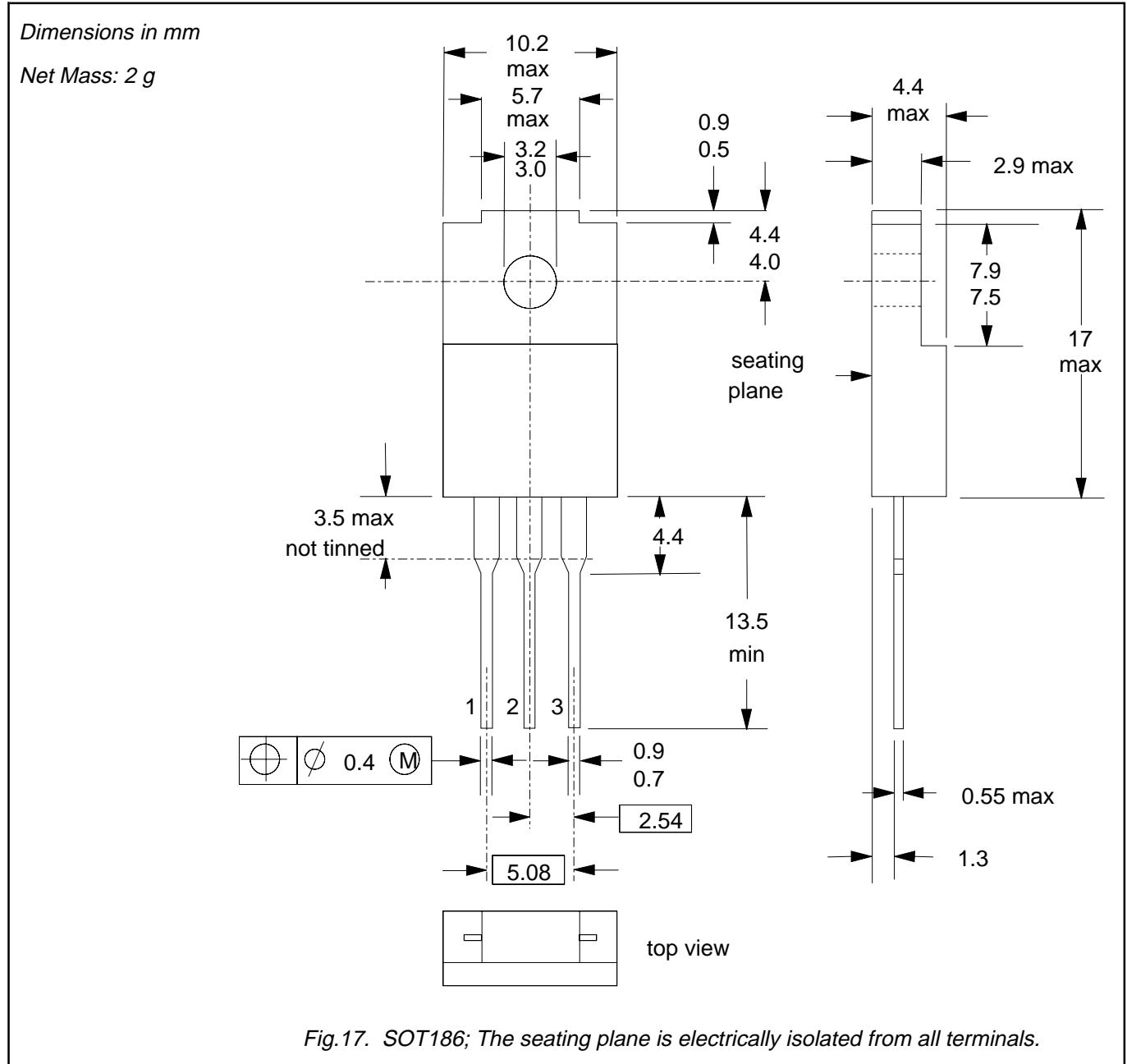
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**MECHANICAL DATA**



**Notes**

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for F-pack envelopes.
3. Epoxy meets UL94 V0 at 1/8".

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**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	
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