DATA SHEET

LVT22V10
3V high speed, universal PLD device

Product specification
Supersedes data of 1996 Mar 12
IC13 Data Handbook

1998 Feb 10

Philips
Semiconductors

PHILIPS

3V high speed, universal PLD device LVT22V10

FEATURES

- Fastest 3V PLD
- Supports 3/5V mixed systems
- Low ground bounce (<1.1V worst case)
- Live insertion/extraction permitted
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Metastable hardened device
- High output drive capability: 32mA/–16mA
- Varied product term distribution with up to 16 product terms per output for complex functions
- Programmable output polarity
- Available in 300 mil-wide 24-pin Plastic Small Outline Package
- Design support provided for third party CAD development and programming hardware

DESCRIPTION

The LVT22V10 is a versatile PAL® device fabricated on the Philips BiCMOS QUBiC process.

The QUBiC process produces very high speed 3V devices (7.5ns) which have excellent noise characteristics. Ground bounce of an output held low while the remaining 9 outputs switch from high to low is typically less than 0.7V. V_{CC} bounce of an output held high while the remaining 9 outputs switch from low to high is typically less than 1.0V.

The LVT22V10 was designed to support mixed 3/5V systems. The inputs are capable of handling 7V while the outputs can be pulled up to 7V.

The designer can interface directly from 5V outputs (CMOS full rail or totem pole) to a 3V LVT input. A 3V LVT output can drive a 5V TTL input directly, or in the case of a CMOS input, the LVT output can interface with the use of an external pull-up resistor. Finally, no external pull-up resistors are needed on unused input pins due to a bus-hold data structure designed into the LVT input.

The LVT22V10 has been designed with high drive outputs (32mA sink and 16mA source currents), which allows for direct connection to a backplane bus. This feature eliminates the need for additional, standalone bus drivers, which are traditionally required to boost the drive of a standard PLDs.

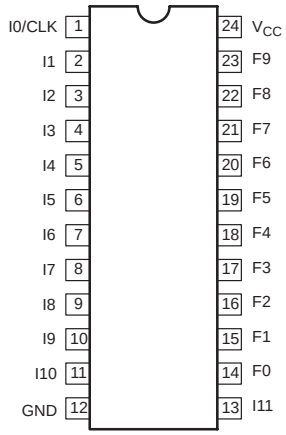
The LVT22V10 outputs are designed to support Live Insertion/Extraction into powered up systems. The output is specially designed so that during V_{CC} ramp, the output remains 3-Stated until $V_{CC} \approx 2.1V$. At that time the outputs become fully functional depending upon device inputs. (See DC Electrical Characteristics, Symbol $I_{PU/PD,}$ Page 5). In addition when an LVT22V10 output is tied to a 5V bus, no bus current is loaded.

The LVT22V10 uses the familiar AND/OR logic array structure, which allows direct implementation of sum-of-products equations.

This device has a programmable AND array which drives a fixed OR array. The OR sum of products feeds an “Output Macro Cell” (OMC) which can be individually configured as a dedicated input, a combinatorial output, or a registered output with internal feedback.

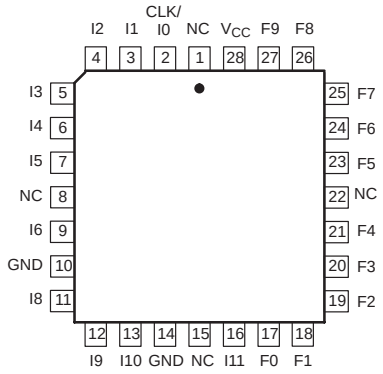
PIN CONFIGURATIONS

D and N Packages



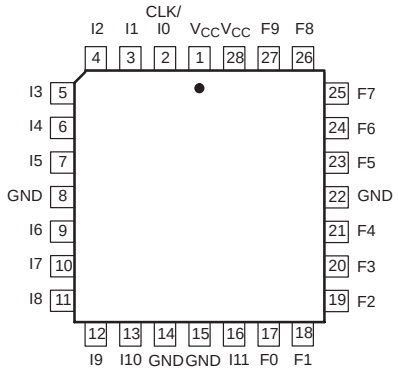
N = Plastic Dual In-Line Package (300mil-wide)
D = Plastic Small Outline Large (300mil-wide) Package

A Package (standard)



A = Plastic Leaded Chip Carrier

A Package (evolutionary)



A = Plastic Leaded Chip Carrier

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ORDERING INFORMATION

PACKAGES	ORDER CODE	DWG NUMBER
24-Pin Plastic DIP (300mil)	LVT22V10-7N (8.0ns device)	SOT222-1
28-Pin PLCC (standard pinout)	LVT22V10B7A (7.5ns device)	SOT261-3
28-Pin PLCC (evolutionary pinout)	LVT22V10-7A (7.5ns device)	SOT261-3
24-Pin Plastic SOL	LVT22V10-7D (8.0ns device)	SOT137-1

PIN LABEL DESCRIPTIONS

SYMBOL	DESCRIPTION
I1 – I11	Dedicated Input
F0 – F9	Macro Cell Input/Output
CLK/I0	Clock Input/Dedicated Input
V_{CC}	Supply Voltage
GND	Ground
NC	No Connection

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

OPERATING RANGES

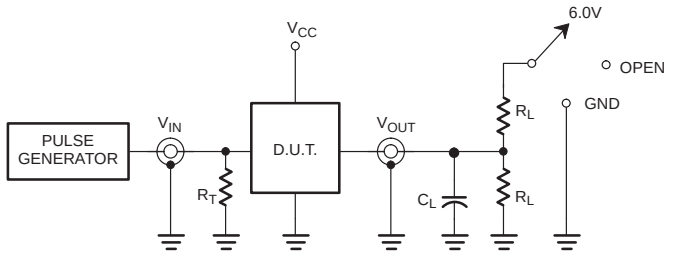
SYMBOL	PARAMETER	RATINGS		UNIT
		MIN	MAX	
V_{CC}	Supply voltage	+3.0	+3.6	V_{DC}
T_{amb}	Operating free-air temperature	0	+75	°C

ABSOLUTE MAXIMUM RATINGS[1]

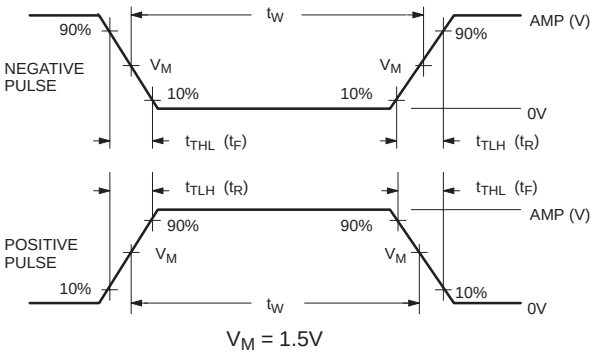
SYMBOL	PARAMETER	RATINGS		UNIT
		MIN	MAX	
V_{CC}	Supply voltage[2]	–0.5	+4.6	V_{DC}
V_{IN}	Input voltage[2]	–0.5	7	V_{DC}
V_{OUT}	Output voltage[3]	–0.5	5.5	V_{DC}
I_{IN}	Input currents	–30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{stg}	Storage temperature range	–65	+150	°C

NOTES:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.
2. Except in programming mode.
3. Outputs can be pulled up to 7V via external pull-up resistor.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
LVT	3.0V	10MHz	500ns	2.5ns	2.5ns

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DC ELECTRICAL CHARACTERISTICS

Over operating ranges.

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS MIN	LIMITS MAX	UNIT
Input voltage						
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IH}	High	V_{CC} = MAX		2.0		V
V_I	Clamp	V_{CC} = MIN, I_{IN} = –18mA			–1.2	V
Output voltage						
V_{OH}	High-level output voltage	V_{CC} = MIN to MAX, V_I = V_{IH} or V_{IL}	I_{OH} = –100 µA	V_{CC}–0.2		V
		V_{CC} = MIN, V_I = V_{IH} or V_{IL}	I_{OH} = –16mA	2.0		V
			I_{OH} = –5.5 mA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN to MAX, V_I = V_{IH} or V_{IL}	I_{OL} = 100µA		0.2	V
		V_{CC} = MIN, V_I = V_{IH} or V_{IL}	I_{OL} = 32 mA		0.5	V
			I_{OL} = 16 mA		0.4	V
Input current						
I_{IL}	Low	V_{CC} = MAX, V_{IN} = 0.0V			–10	µA
I_{IH}	High	V_{CC} = MAX, V_{IN} = V_{CC}			10	µA
I_I	Max input current	V_{CC} = MAX, V_{IN} = 5.5V			10	µA
I_I	Pin 1 (program)	V_{CC} = MAX, V_{IN} = 5.5V			20	µA
I_{BHL}	Bus hold low sustaining current[2]	V_{CC} = 3V, V_I = 0.8V		75		µA
I_{BHH}	Bus hold high sustaining current[3]	V_{CC} = 3V, V_I = 2V		–75		µA
I_{BHLO}	Bus hold low overdrive current[4, 9]	V_{CC} = 3.6V		500		µA
I_{BHHO}	Bus hold high overdrive current[5, 9]	V_{CC} = 3.6V		–500		µA
Output current						
I_{OFF}	Output off current	V_{CC} = 0V, V_I or V_O = 0 to 4.5V			±10	µA
I_{EX}	Current into an output in high state when V_O > V_{CC}	V_O = 5.5V, V_{CC} = 3.0V			±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[8]	V_{CC} <1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; OE/$\overline{OE}$ = X			100	µA
		V_{CC} = MAX				
I_{OZH}	Output leakage[6]	V_{IN} = V_{IL} or V_{IH}, V_{OUT} = 5.5V			10	µA
I_{OZL}	Output leakage[6]	V_{IN} = V_{IL} or V_{IH}, V_{OUT} =0V			–10	µA
I_{SC}	Short circuit[7]	V_{OUT} = 0.5V		–30	–220	mA
I_{CC}	V_{CC} supply current	V_{CC} = 3.6V, Outputs enabled, V_I = V_{CC} or GND; I_O = 0			170	mA
Ground/V_{CC} Bounce				**MIN**	**TYP**	**MAX** / **UNIT**
V_{OHV}	Maximum dynamic V_{OH}	V_{CC} = 3.0V, 25°C, C_L = 50pF (including jig capacitance)		2.2	2.3	V
V_{OLP}	Maximum dynamic V_{OL}	V_{CC} = 3.3V, 25°C, C_L = 50pF (including jig capacitance)	LVT22V10-7		0.7 / 1.1	V
			LVT22V10B7		1.0 / 1.1	V

NOTES:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. The bus hold circuit can sink at least the minimum low sustaining current at V_{IL} MAX. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} MAX.
3. The bus hold circuit can source at least the minimum high sustaining current at V_{IH} MIN. I_{BHL} should be measured after raising V_{IN} to V_{CC} and then lowering it to $V_{IH\ MIN.}$
4. An external driver must source at least I_{BHLO} to switch this node from low to high.
5. An external driver must sink at least I_{BHHO} to switch this node from high to low.
6. I/O pin leakage is the worst case of I_{OZX} or I_{IX} (where X = H or L).
7. No more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
8. This parameter is valid for any V_{CC} between 0V and 1.2 V with a transition time up to 10 mS. From V_{CC} = 1.2 to V_{CC} = 3.3V ±0.3V a transition time of 100 µS is permitted. X = Don't care.
9. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where input current may be affected.

AC ELECTRICAL CHARACTERISTICS

Over commercial operating temperature range.

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				MIN	TYP	MAX	
t_{PD}	Input or feedback to non-registered output[2] PLCC package	Active-LOW				7.5	ns
		Active-HIGH				7.5	ns
	Input or feedback to non-registered output[2] DIP and SOL packages	Active-LOW				8.0	ns
		Active-HIGH				8.0	ns
t_S	Setup time from input, feedback or SP to Clock			5.5			ns
t_H	Hold time			0			ns
t_{CO}	Clock to output					5.0	ns
t_{CF}	Clock to feedback[3]					3.0	ns
t_{AR}	Asynchronous Reset to registered output					12.0	ns
t_{ARW}	Asynchronous Reset width			5.0			ns
t_{ARR}	Asynchronous Reset recovery time			5.0			ns
t_{SPR}	Synchronous Preset recovery time			5.0			ns
t_{WL}	Width of Clock LOW			3.0			ns
t_{WH}	Width of Clock HIGH			3.0			ns
f_{MAX}	Maximum frequency; External feedback $1/(t_S + t_{CO})$[4]			95			MHz
	Maximum frequency; Internal feedback $1/(t_S + t_{CF})$[4]			118			MHz
t_{EA}	Input to Output Enable[5]					8.5	ns
t_{ER}	Input to Output Disable[5]					8.5	ns
Capacitance[6]							
C_{IN}	Input Capacitance (Pin 1)	V_{IN} = 2.0V	V_{CC} = 3.3V, T_{amb} = 25°C, f = 1MHz		6		pF
	Input Capacitance (Others)	V_{IN} = 2.0V			6		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V			8		pF

NOTES:

1. Test Conditions: $R_1 = 500\Omega$, $R_2 = 500\Omega$
2. t_{PD} is tested with switch S_1 open and C_L = 50pF (including jig capacitance). V_{IH} = 3V, V_{IL} = 0V, V_T = 1.5V.
3. Calculated from measured f_{MAX} internal.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
5. For 3-State output; output enable times are tested with C_L = 50pF to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.3V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.3V)$ level with S_1 closed.
6. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

PRODUCT FEATURES

Low Ground Bounce

The Philips Semiconductors BiCMOS QUBiC process results in exceptional noise immunity. Ground bounce is noise that is generated on a non-switching active low output when other outputs on the device switch from high to low. The worst case condition occurs when 9 outputs simultaneously switch from high to low and the tenth output is active low. The ground bounce on this tenth output for Philips LVT22V10 is typically less than 0.7V.

V_{CC} Bounce

V_{CC} bounce occurs on a non-switching active high output when other outputs are making a low to high transition. This specification is important to consider in 3.3V designs because of the reduced noise margin between V_{CC} and V_{OH} of only 1.3V relative to the traditional 5V system's noise margin of 3V. The Philips LVT22V10 V_{CC} bounce of an output held high while the remaining 9 outputs switch from low to high is typically less than 1.0V in magnitude.

Live Insertion/Extraction Capability

There are some inherent problems associated with inserting or extracting an unpowered module from a powered-up, active system. The LVT22V10 outputs have been designed such that any chance of bus contention, glitching or clamping is eliminated.

Detailed information on this feature is provided in an application note AN051: *Philips PLDs Support Live Insertion Applications*.

Bus Hold Input Structure

Bus Hold is a feature that maintains the input state of the device by incorporating a weak latch into the input structure. This latch maintains the input state until a minimum level of current (called the overdrive current) is supplied to change the input state. This is useful in bus applications where the bus is placed into a high impedance state. The LVT22V10's inputs, in this high impedance situation, maintain valid logic levels until the bus is actively driven to a new state.

Improved Fuse Verification Circuitry Increases Reliability

Philips has developed a new means of testing the integrity of fuses, both blown and intact fuses, which insures that all the fuses have been correctly programmed and that each and every fuse – whether "blown" or "intact" – is at the appropriate and optimal fuse resistance. This dual verify scheme represents a significant improvement over single reference voltage comparisons schemes that have been used for bipolar devices since the late 1980s. Detailed information on this feature is provided in an application note entitled *Dual Verify Technique Increases Reliability of PLDs*.

Programmable 3-stage Outputs

Each output has a 3-Stage output buffer with 3-State control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Output Polarity

The polarity of each macro cell output can be Active-HIGH or Active-LOW, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is controlled by programmable bit S_0 in the Output Macro Cell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions. If the pin definition and output equation have the same polarity, the output is programmed to be Active-HIGH (S_0 = 1).

Preset/Reset

For initialization, the LVT22V10 has additional Preset and Reset product terms. These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW, independent of the clock.

Note that Preset and Reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the LVT22V10 will depend on the programmed output polarity. The V_{CC} rise must be monotonic and the reset delay time is 1–10µs maximum.

Security Fuse

After programming and verification, LVT22V10 designs can be secured by programming the security fuse link. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is programmed.

Quality and Testability

The LVT22V10 offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies programmability and functionality of the device to provide the highest programming and post-programming functional yields.

Technology

The BiCMOS LVT22V10 is fabricated with the Philips Semiconductors process known as QUBiC. QUBiC combines an advanced, state-of-the-art 1.0µm (drawn feature size) CMOS process with an ultra fast bipolar process to achieve superior speed and drive capabilities. QUBiC incorporates three layers of Al/Cu interconnects for reduced chip size, and our proven Ti-W fuse technology ensures highest programming yields.

Programming

The LVT22V10 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Philips Semiconductors SNAP design software package. ABEL™ CUPL™ and PALASM® 90 design software packages also support the LVT22V10 architecture.

All packages allow Boolean and state equation entry formats, SNAP, ABEL and CUPL also accept, as input, schematic capture format.

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CUPL is a trademark of Logical Devices, Inc.
PALASM is a registered trademark of AMD Corp.

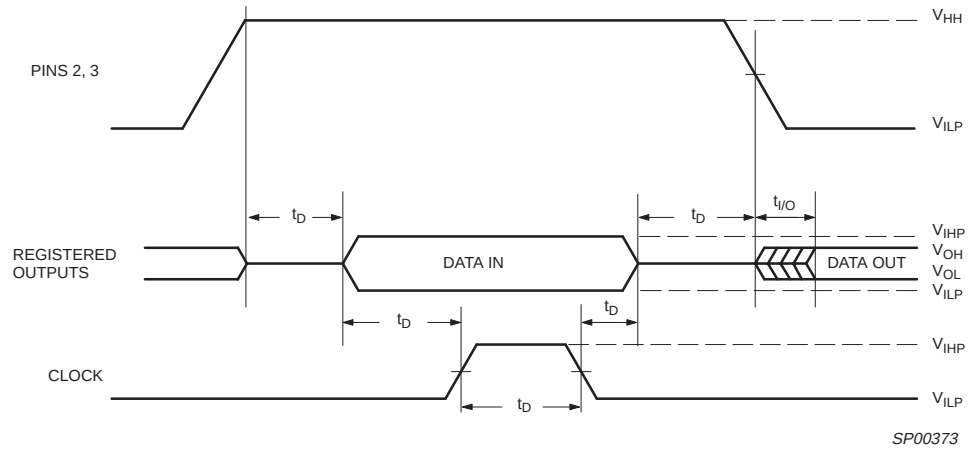
Output Register Preload

The register on the LVT22V10 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery. The procedure for preloading follows:

1. Raise V_{CC} to 3.3V ± 0.3V.
2. Set pin 2 or 3 to V_{HH} to disable outputs and enable preload.
3. Apply the desired value (V_{ILP}/V_{IHP}) to all registered output pins. Leave combinatorial output pins floating.
4. Clock Pin 1 from V_{ILP} to V_{IHP}.
5. Remove V_{ILP}/V_{IHP} from all registered output pins.
6. Lower pin 2 or 3 to V_{ILP}.
7. Enable the output registers according to the programmed pattern.
8. Verify V_{OL}/V_{OH} at all registered output pins. Note that the output pin signal will depend on the output polarity.

PRELOAD SET-UP

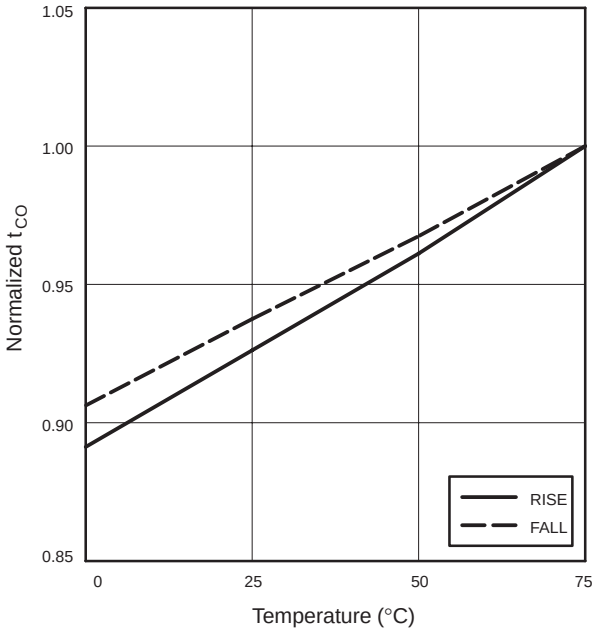
SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	REC	MAX	
V_{HH}	Super-level input voltage	9.5	9.5	10	V
V_{ILP}	Low-level input voltage	0	0	0.8	V
V_{IHP}	High-level input voltage	2.4	3.3	3.6	V
t_D	Delay time	100	200	1000	ns
$t_{I/O}$	I/O valid after Pin 2 or 3 drops from V_{HH} to V_{ILP}	100			ns



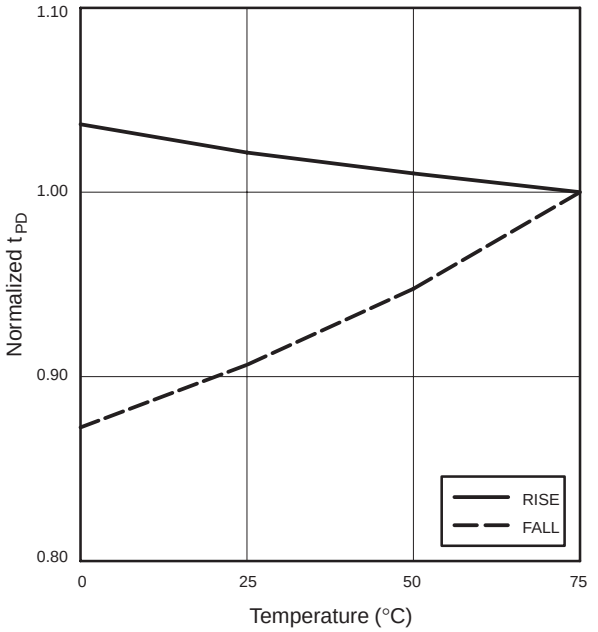
Output Register Preload Waveform

LVT22V10 TIMING CHARACTERIZATION

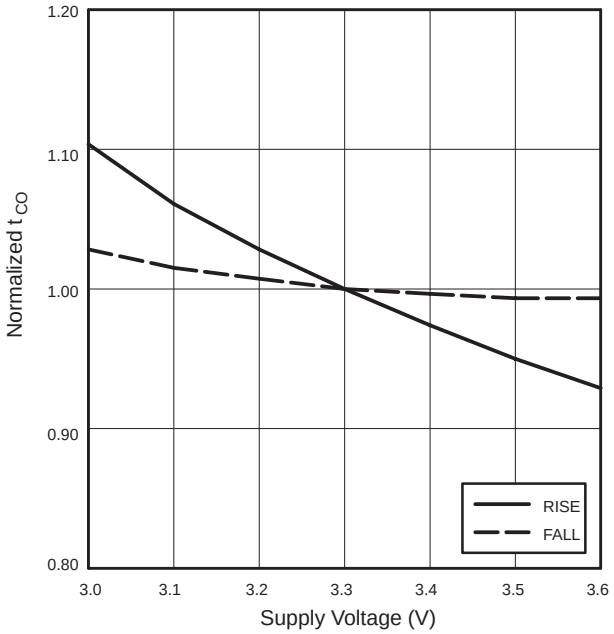
Normalized t_{CO} vs Temperature
(V_{CC} = 3.3V, output capacitance = 50pF, 5outputs switching)



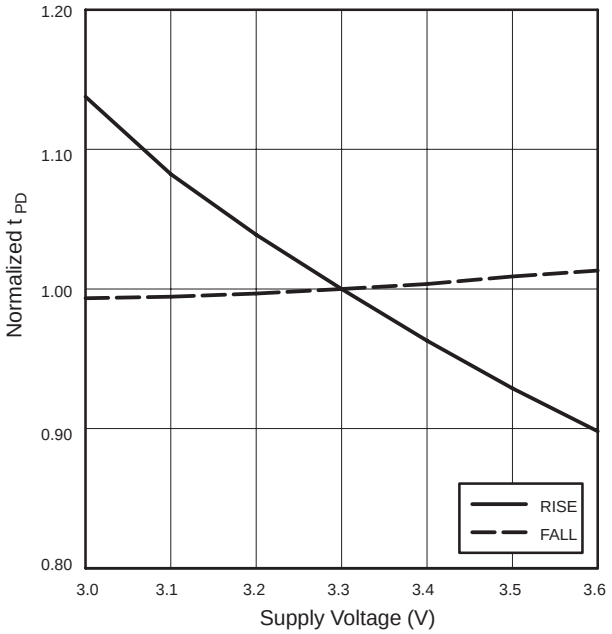
Normalized t_{PD} vs Temperature
(V_{CC} = 3.3V, output capacitance = 50pF, 5 outputs switching)



Normalized t_{CO} vs V_{CC}
(temp = 25°C, output capacitance = 50pF, 5 outputs switching)



Normalized t_{PD} vs V_{CC}
(temp = 25°C, output capacitance = 50pF, 5 outputs switching)



The timing characterization represents the average values of a representative sample for each parameter.
The data can be used to derate the MAX AC CHARACTERIZATION based upon the specific user design.
Philips guarantees the MAX AC CHARACTERIZATION specifications.

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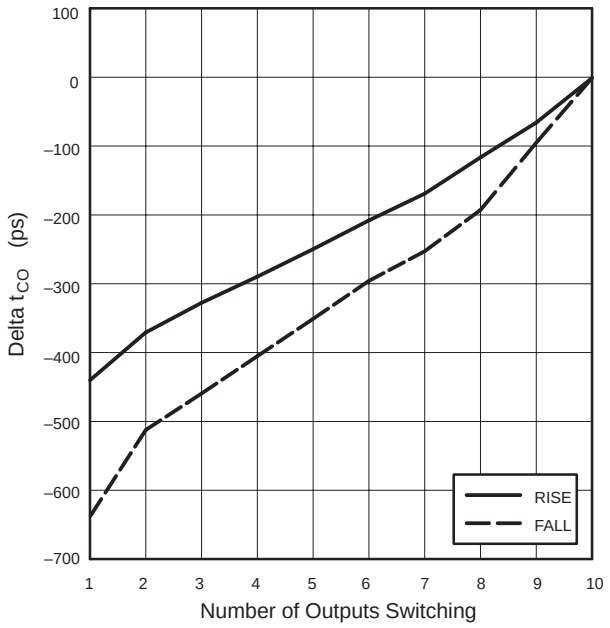
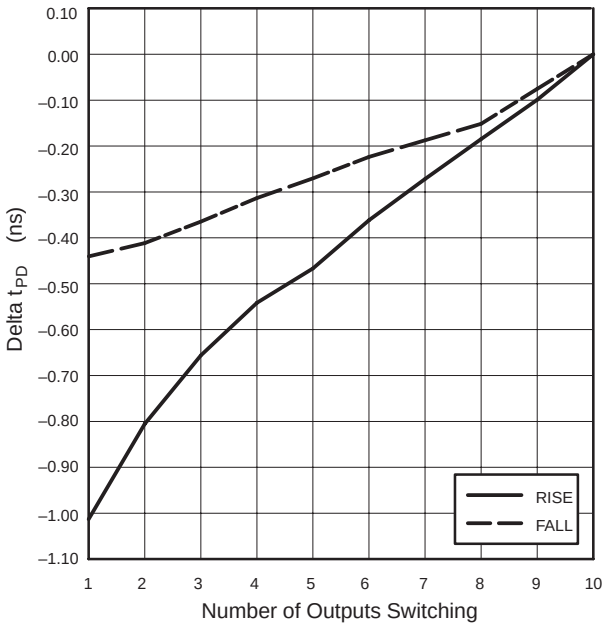
LVT22V10 TIMING CHARACTERIZATION

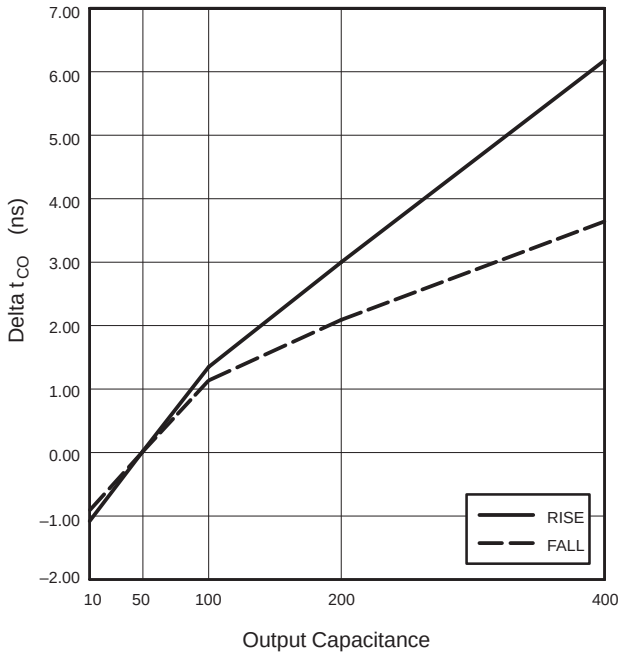
Delta t_{CO} vs Number of Outputs Switching
(V_{CC} = 3.3V, temp = 25°C, output capacitance = 50pF)



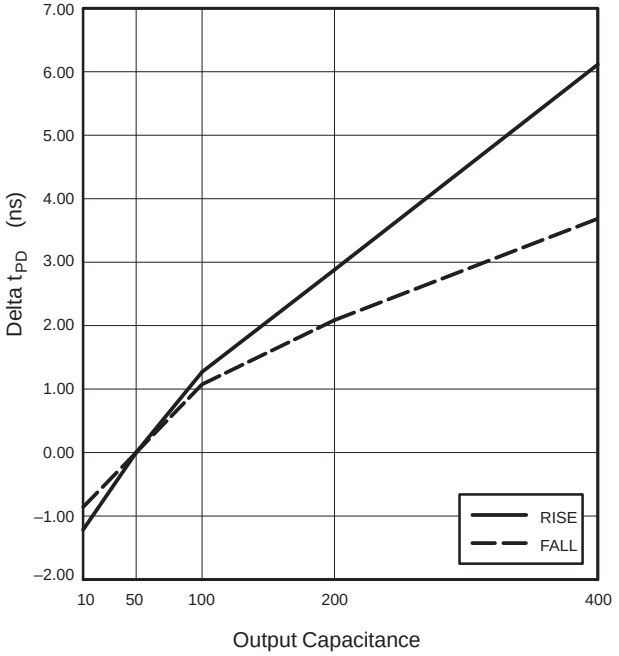
Delta t_{PD} vs Number of Outputs Switching
(V_{CC} = 3.3V, temp = 25°C, output capacitance = 50pF)



Delta t_{CO} vs Output Capacitance
(V_{CC} = 3.3V, temp = 25°C, 5 Outputs Switching)



Delta t_{PD} vs Output Capacitance
(V_{CC} = 3.3V, temp = 25°C, 5 Outputs Switching)



The timing characterization represents the average values of a representative sample for each parameter.
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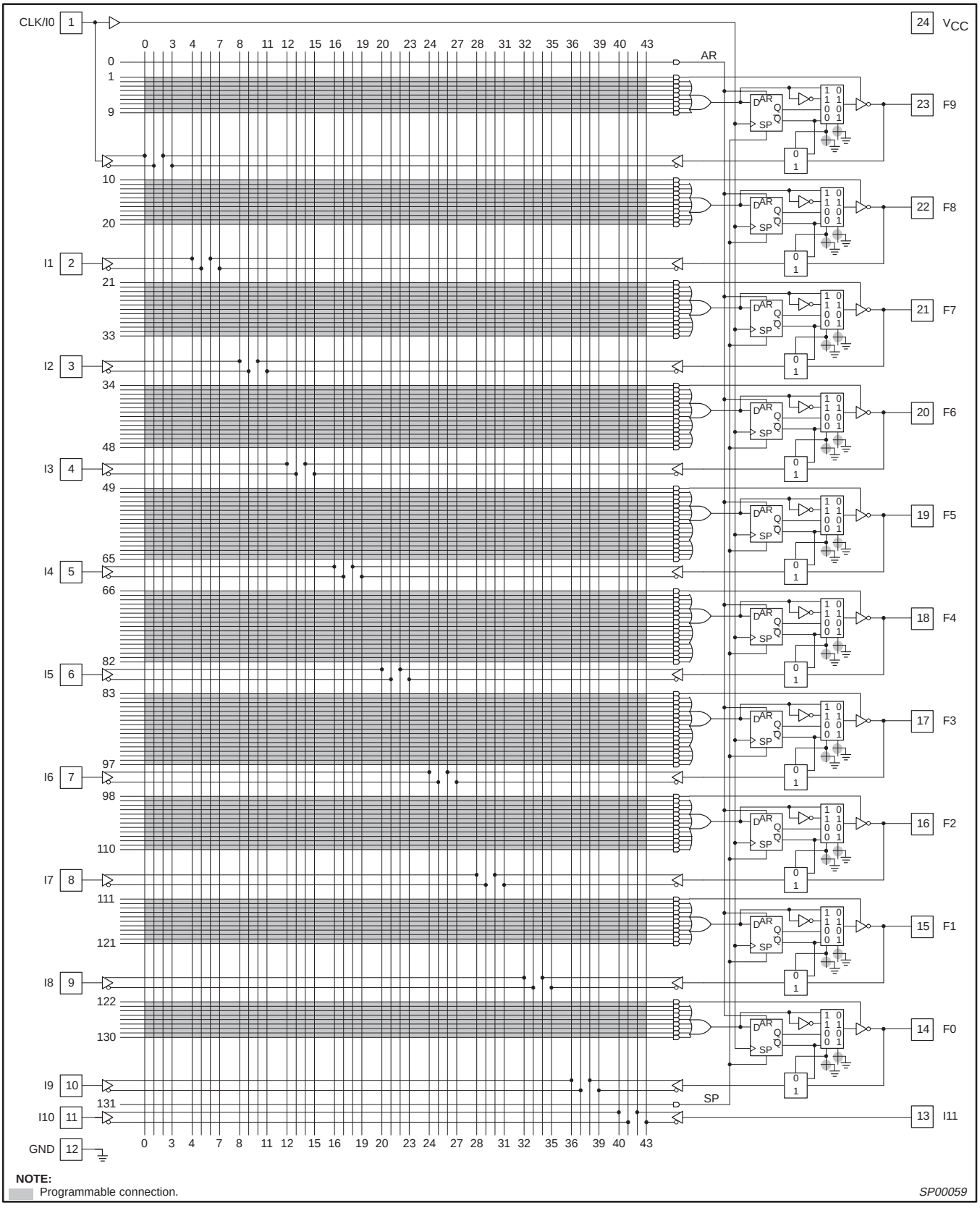
LOGIC DIAGRAM



NOTE:
Programmable connection.

SP00059

FUNCTIONAL DIAGRAM

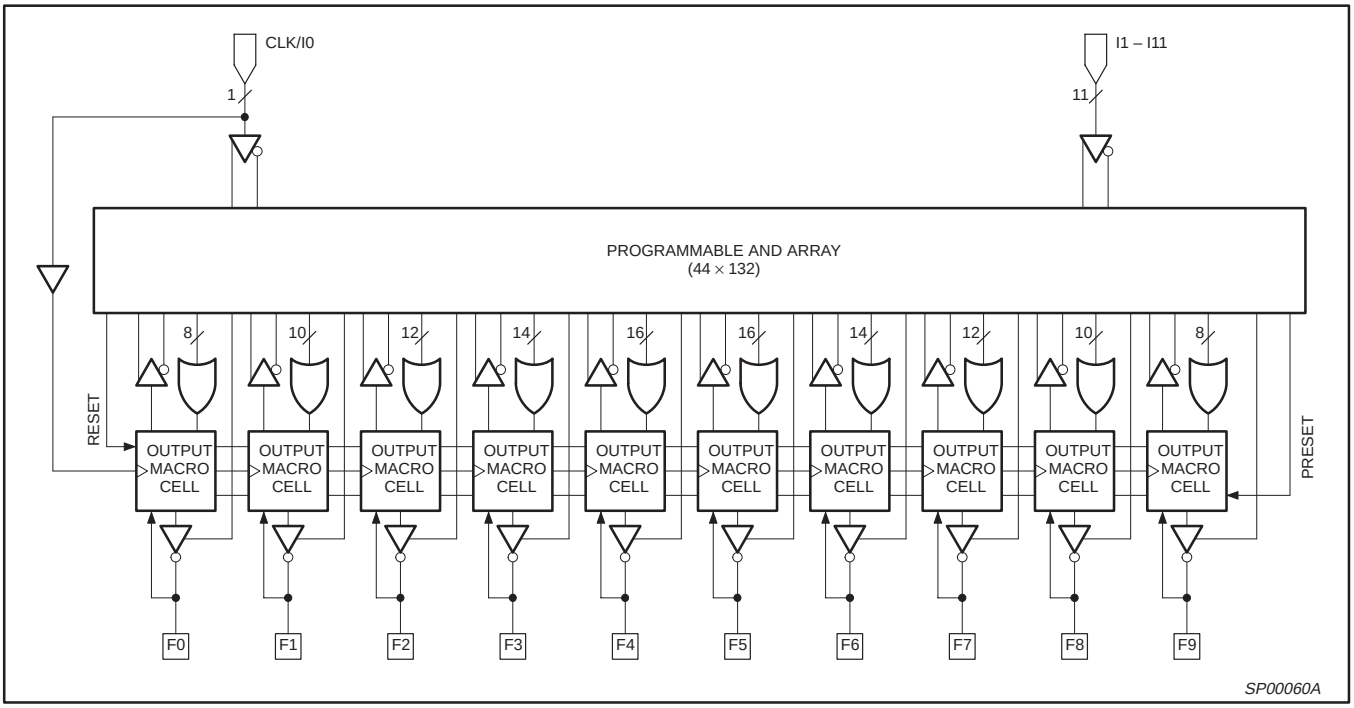


Figure 1. Functional Diagram

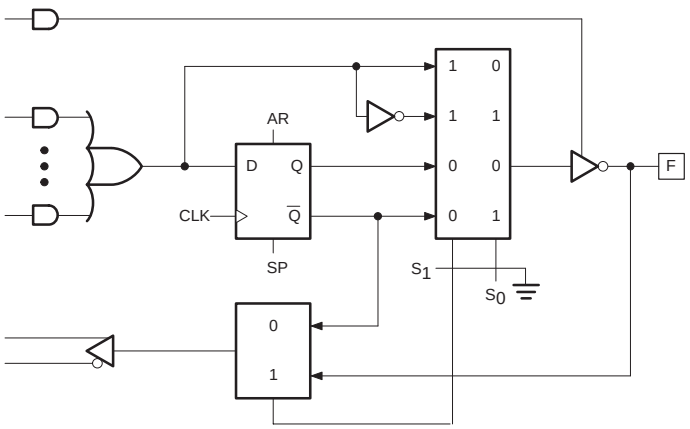
FUNCTIONAL DESCRIPTION

The LVT22V10 allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function.

Product terms with all fuses opened assume the logical HIGH state; product terms connected to both True and Complement of any single input assume the logical LOW state.

The LVT22V10 has 12 inputs and 10 I/O Macro Cells (Figure 1). The Macro Cell allows one of four potential output configurations, registered output or combinatorial I/O, Active-HIGH or Active-LOW (see Figure 2). The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits S_0 –S_1. Multiplexer controls are connected to ground (0) through a programmable fuse link, selecting the "0" path through the multiplexer. Programming the fuse disconnects the control line from GND and it floats to V_{CC} (1), selecting the "1" path.

OUTPUT MACRO CELL



S_1	S_0	OUTPUT CONFIGURATION
0	0	Registered/Active-LOW
0	1	Registered/Active-HIGH
1	0	Combinatorial/Active-LOW
1	1	Combinatorial/Active-HIGH

0 = Unprogrammed fuse
1 = Programmed fuse

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Figure 2. Output Macro Cell Logic Diagram

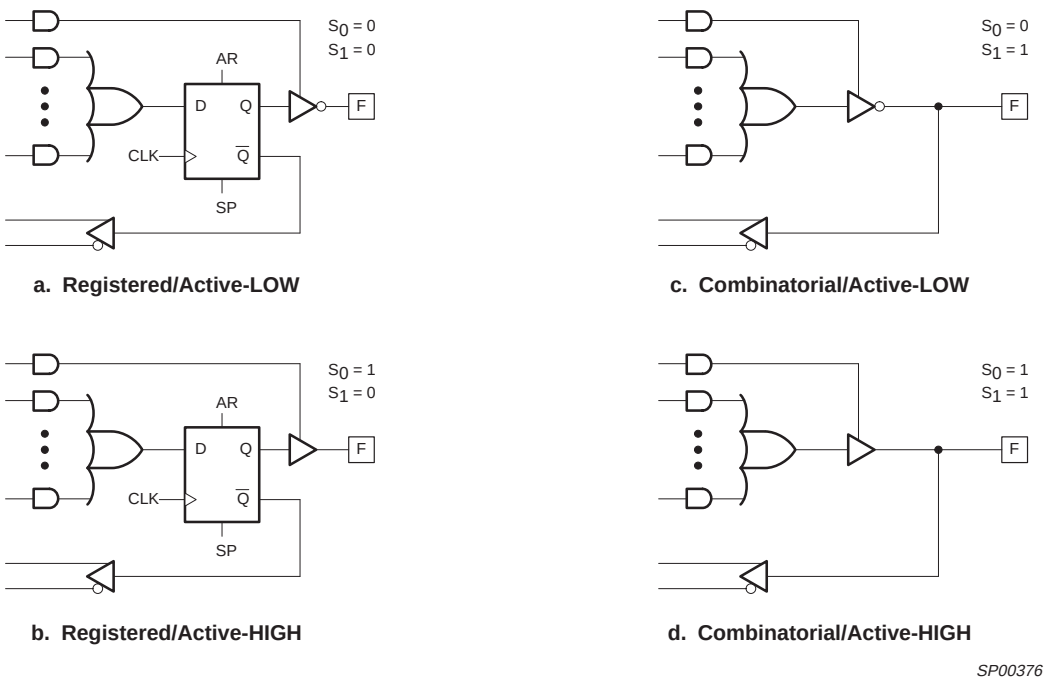

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Figure 3. Output Macro Cell Configurations

Registered Output Configuration

Each Macro Cell of the LVT22V10 includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH transition of the clock input. In the registered configuration (S_1 = 0), the array feedback is from $\overline{Q}$ of the flip-flop.

Combinatorial I/O Configuration

Any Macro Cell can be configured as combinatorial by selecting the multiplexer path that bypasses the flip-flop (S_1 = 1). In the combinatorial configuration, the feedback is from the pin.

Variable Input/Output Pin Ratio

The LVT22V10 has twelve dedicated input lines, and each Macro Cell output can be an I/O pin. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity.

INTERFACING IN MIXED 3V/5V SYSTEMS

3V Logic Driving 5V Logic

The LVT family has outputs that swing virtually between the power supply rails, thereby allowing direct interfacing with TTL switching levels.

When interfacing the outputs of any of our 3V logic ICs with standard TTL-level logic inputs (bipolar or CMOS HCT), the output levels from the 3V logic are sufficient to directly drive the 5V logic.

When driving CMOS-level devices (such as HC or AC), the output voltage from the 3V logic is insufficient to ensure reliable operation. This problem can be easily resolved by using a pull-up resistor at the interface.

5V Logic Driving 3V Logic

Since the LVT ICs do not have protection diodes between their inputs and V_{CC}, the inputs of these devices can therefore withstand higher levels than the supply voltage, and they can be directly connected to 5V CMOS logic outputs. For the LVT family, the combination of low power dissipation with the live insertion feature, bus hold and full 5V input/output capability make this logic ideal for 3.3V backplane interfacing.

INTERFACING 3 VOLT AND 5 VOLT LOGIC

	FROM	TO	METHOD
3V to 5V	LVT Output	TTL Inputs	Direct
		CMOS inputs	Pull-up
5V to 3V	CMOS Rail	LVT Input	Direct
	Totem-Pole	LVT Input	Direct
	Open Drain	LVT Input	Pull-up

LVT22V10 METASTABLE HARDENED CHARACTERISTICS

Metastable Hardened Characteristics

What is metastable hardened? Philips Semiconductors uses the term “metastable hardened” to describe a combination of two characteristic features. The first is a patented Philips circuit that prevents the outputs from glitching, oscillating, or remaining in the linear region under any circumstances, including setup and hold time violations. The second is the flip-flops’ inherent ability of resolving the metastable condition. Philips provides complete data on the LVT22V10’s metastable characteristics

With the LVT22V10, any tendency towards internal metastability is resolved by Philips Semiconductors patented circuitry. If a metastable event occurs within the flop, the only outward manifestation of the event will be an increased clock-to-Q delay. This delay is a function of the metastability characteristics of the device, defined by τ and T_O as described below. Since the outputs never glitch, oscillate, or remain in the linear region, the only metastable failure that can propagate further into the system is when the next flip-flop in the system samples the LVT22V10’s output at precisely the same time it is making a logic transition. By allowing sufficient time for any increased clock-to-Q delay, propagation of metastable failures can be avoided. The following design example illustrates this concept.

Design Example

Suppose a designer wants to use the LVT22V10 for synchronizing asynchronous data that is arriving at 2MHz (as measured by a frequency counter), in a 3.3V system that has a clock frequency of 33MHz, at an ambient temperature of 25°C. She has decided that she would like to sample the output of the LVT22V10 15ns after the clock edge to ensure that any clock-to-Q delays that were the result of the LVT22V10 internal metastability resolution circuitry have completed and the outputs have transitioned. The MTBF for this situation can be calculated by using the equation below:

$$MTBF = e(t'/\tau)/T_O F_C F_1$$

In this formula, F_C is the frequency of the clock, F_1 is the average input event frequency, and t’ is the time after the clock pulse that the output is sampled ($t' > T_{CO}$). T_O and τ are device parameters provided by the semiconductor manufacturer (refer to the following table for the LVT22V10 metastability specifications). T_O and τ are derived from tests and can be most nearly be defined as follows: τ is a function of the rate at which a latch in a metastable state resolves that condition. T_O is a function of the measurement of the propensity of a latch to enter a metastable state. T_O is also a normalization constant, which is a very strong function of the normal propagation delay of the device.

In this situation the F_1 will be twice the data frequency, or 4MHz, because input events consist of both of low and high transitions. Thus, in this case, F_C is 33MHz, F_1 is 4MHz, τ is 317ps, t’ is 15ns, and T_O is 4.27×10^{-3} seconds. Using the above formula the actual MTBF for this situation is 1.26×10^9 seconds or 39 years for the LVT22V10.

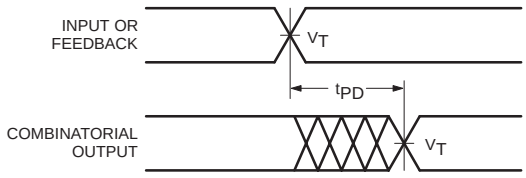
Summary

The Philips LVT22V10 has on-chip circuitry that completely eliminates any output glitches, oscillations, or other output anomalies associated with metastable conditions. For outputs that are then used to generate clocks, control signals or other asynchronous data this represents an unparalleled level of reliability in a PLD. In addition, a complete set of metastability data is provided, that allows designers the ability to design robust systems where data is synchronously pipelined.

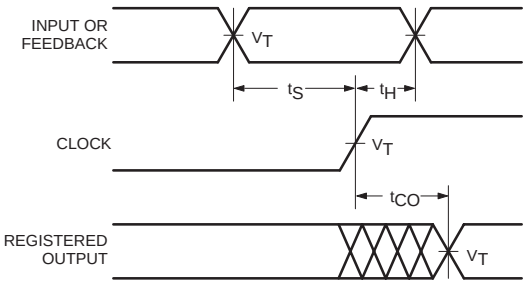
LVT22V10 VALUES FOR τ AND T_O

V_{CC}	0°C		25°C		75°C	
	τ	T_O	τ	T_O	τ	T_O
3.0V	829.00ps	1.16E–08	691.00ps	1.09E–07	429.00ps	2.27E–04
3.3V	358.00ps	2.36E–04	317.00ps	4.27E–03	329.00ps	5.75E–03
3.6V	237.00ps	2.66E–01	230.00ps	6.47E–01	250.00ps	1.13E+00

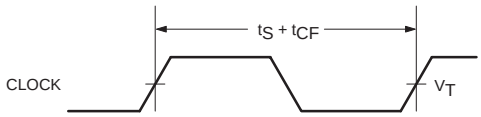
SWITCHING WAVEFORMS



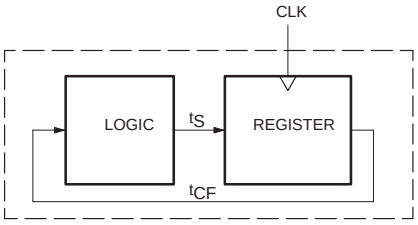
Combinatorial Output



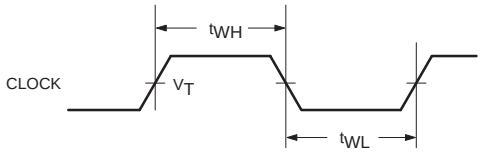
Registered Output



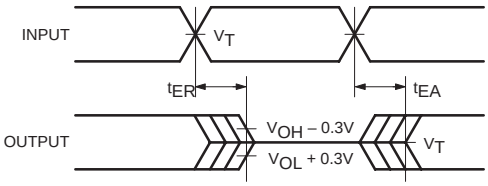
Clock to Feedback (f_{MAX} Internal)
(See Path at Right)



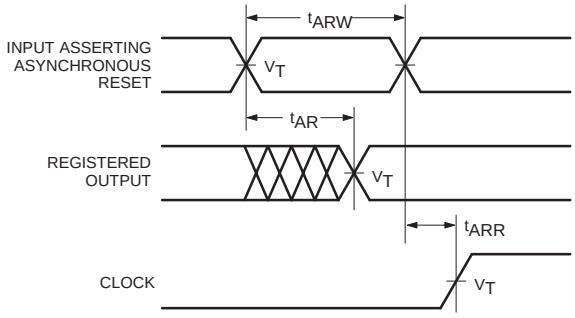
Clock to Feedback



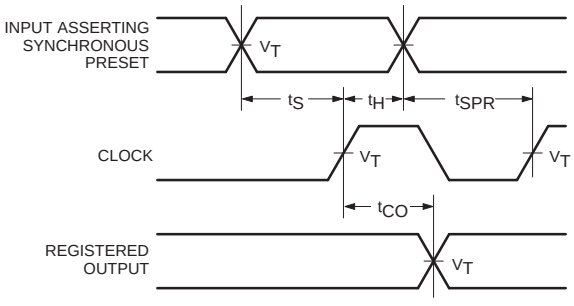
Clock Width



Input to Output Disable/Enable



Asynchronous Reset



Synchronous Preset

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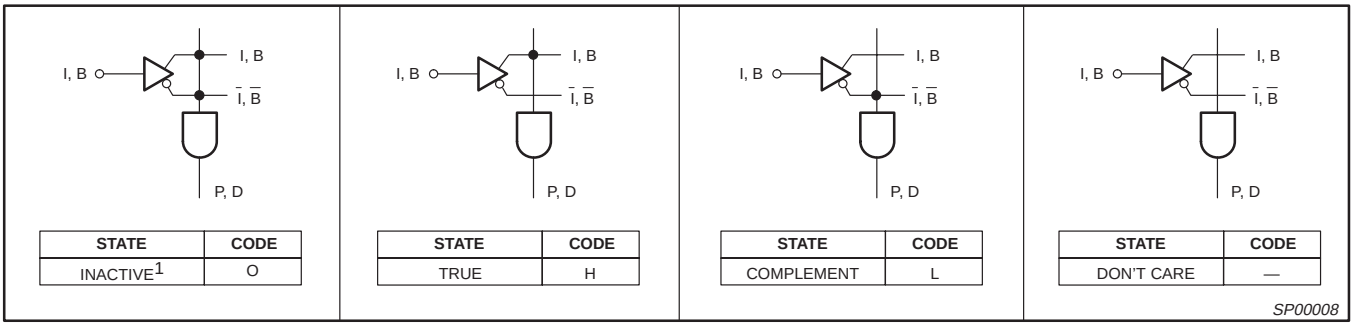
NOTES:
1. V_T = 1.5V.
2. Input pulse amplitude 0V to 3.0V.
3. Input rise and fall times 1.5ns max.

"AND" ARRAY – (I, B)

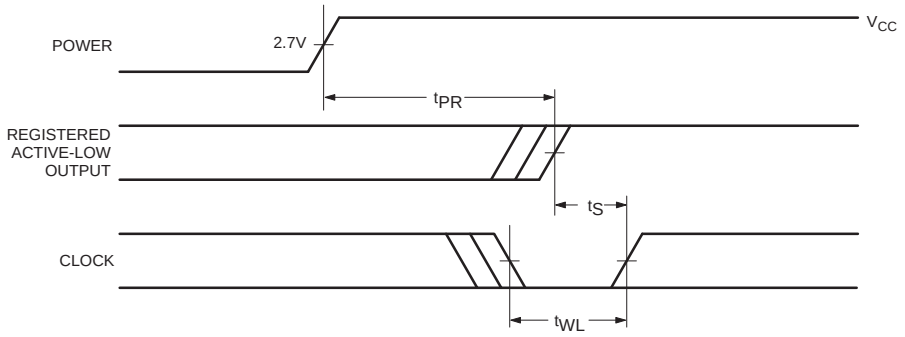


NOTE:
1. This is the initial state.

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

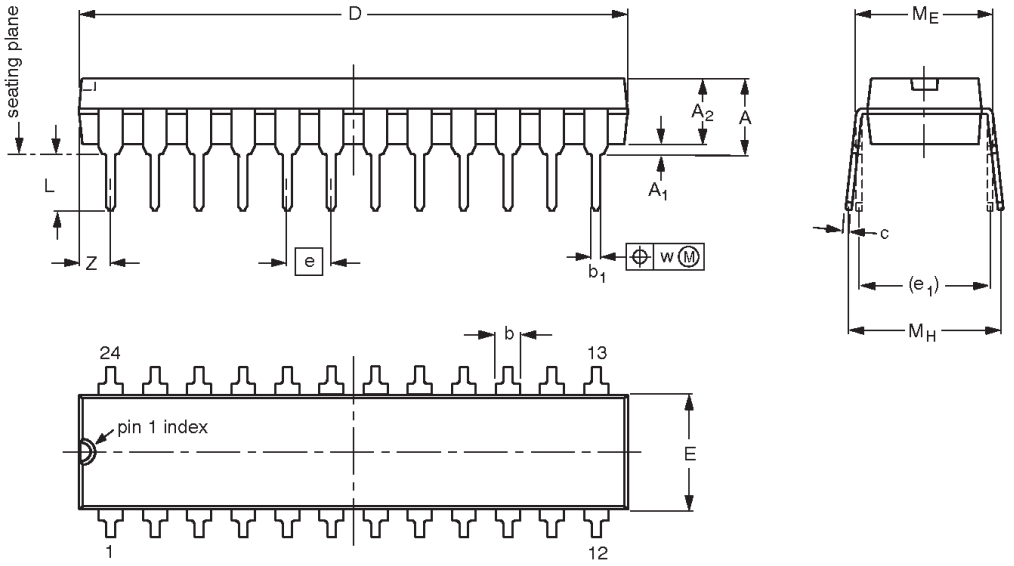


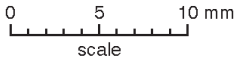
Power-Up Reset Waveform

SP00389

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
t_{PR}	Power-up Reset Time		1	µs
t_S	Input or Feedback Setup Time	See AC Electrical Characteristics		
t_{WL}	Clock Width LOW			

DIP24: plastic dual in-line package; 24 leads (300 mil) **SOT222-1**





DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

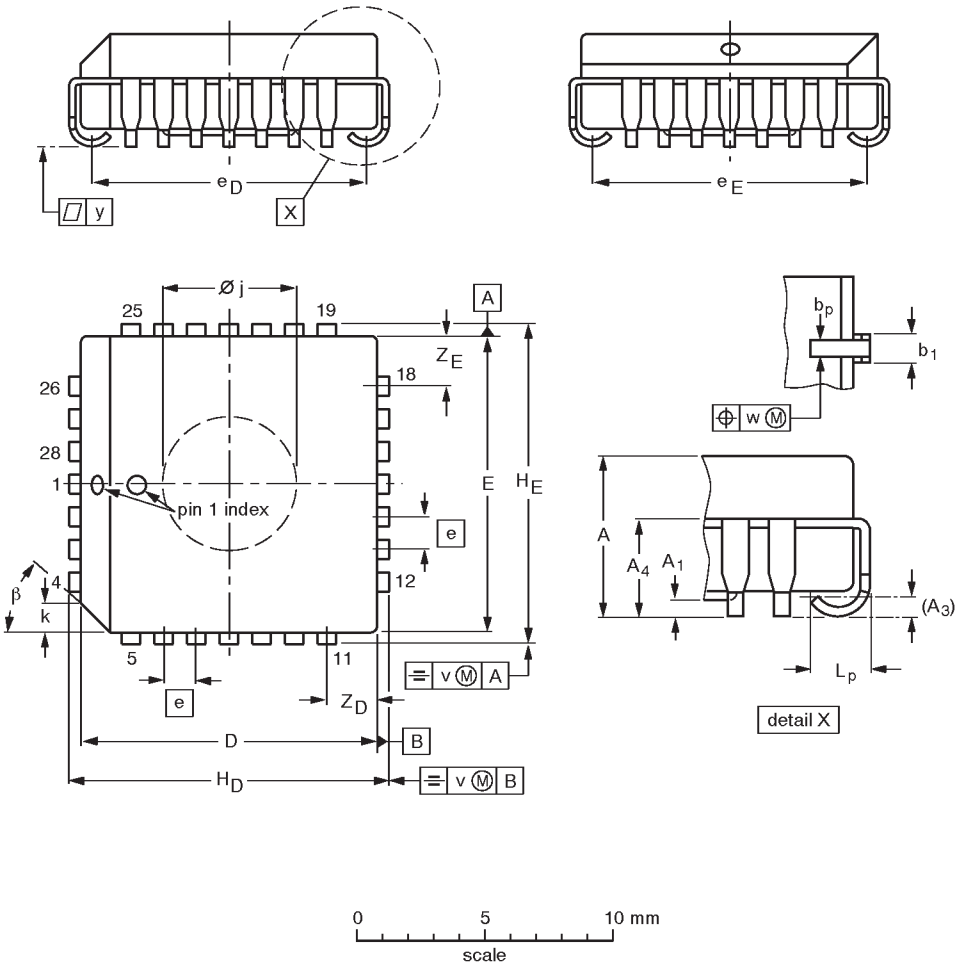
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

PLCC28: plastic leaded chip carrer; 28 leads; pedestal **SOT261-3**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

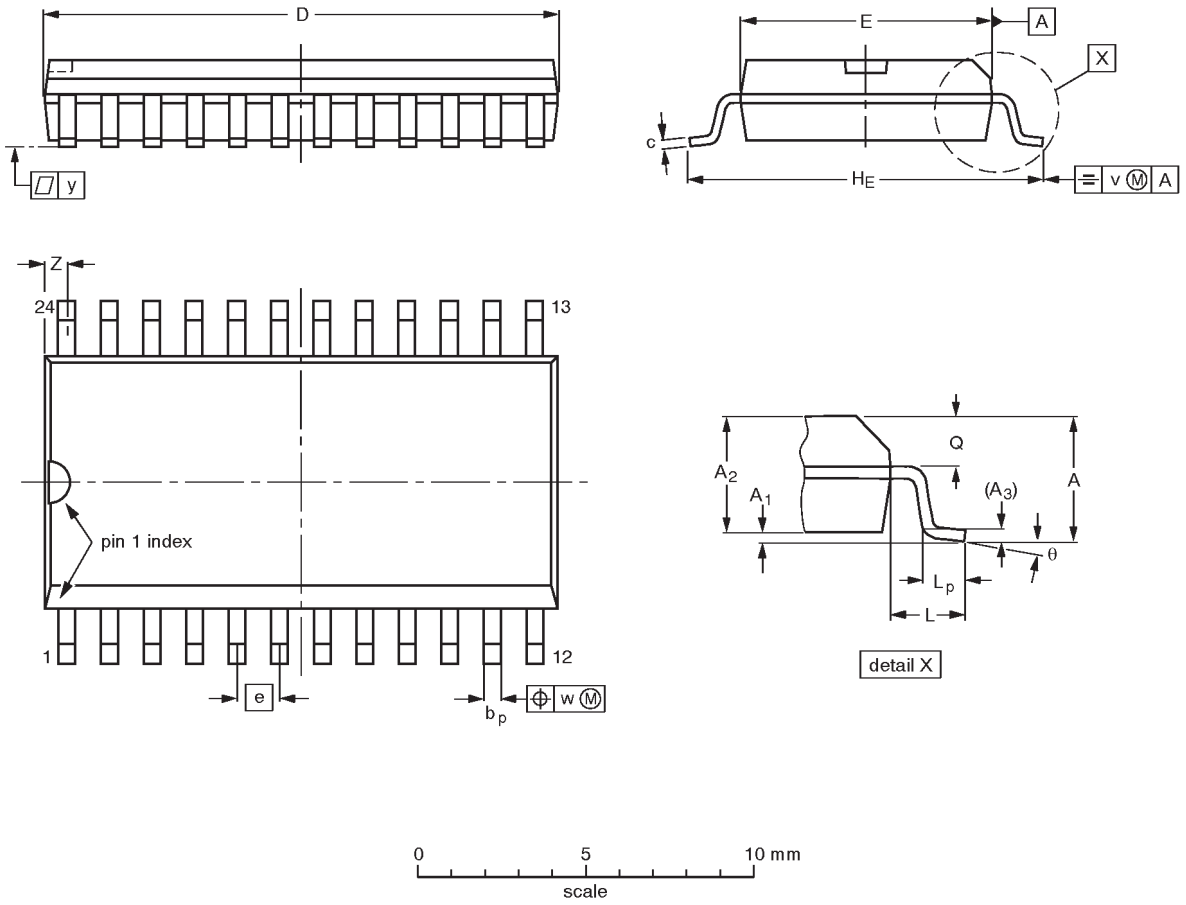
UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	$Ø_j$	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.13	0.25	3.05	0.53 0.33	0.81 0.66	11.58 11.43	11.58 11.43	1.27	10.92 9.91	10.92 9.91	12.57 12.32	12.57 12.32	1.22 1.07	5.69 5.54	1.44 1.02	0.18	0.18	0.10	2.06	2.06	45°
inches	0.180 0.165	0.005	0.01	0.12	0.021 0.013	0.032 0.026	0.456 0.450	0.456 0.450	0.05	0.430 0.390	0.430 0.390	0.495 0.485	0.495 0.485	0.048 0.042	0.224 0.218	0.057 0.040	0.007	0.007	0.004	0.081	0.081	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT261-3		MO-047AB				~~92-11-17~~ 95-02-25

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~92-11-17~~ 95-01-24

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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