TrenchMOS ${ }^{\text {TM }}$ transistor

## GENERAL DESCRIPTION

N -channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting. The device features very low on-state resistance and has integral zener diodes giving ESD protection. It is intended for use in automotive and general purpose switching applications.

PINNING - SOT223

| PIN | DESCRIPTION |
| :---: | :--- |
| 1 | gate |
| 2 | drain |
| 3 | source |
| 4 | drain (tab) |

QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | UNIT |
| :---: | :---: | :---: | :---: |
| $V_{\text {DS }}$ | Drain-source voltage | 55 | V |
| $\mathrm{I}_{\mathrm{D}}$ | Drain current | 5.5 | A |
| $\mathrm{P}_{\text {tot }}$ | Total power dissipation | 1.8 | W |
| $\mathrm{T}_{\mathrm{j}}$ | Junction temperature | 150 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ | Drain-source on-state resistance $\quad \mathrm{V}_{\mathrm{GS}}=5 \mathrm{~V}$ | 150 | $\mathrm{m} \Omega$ |

PIN CONFIGURATION


SYMBOL


## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {DS }}$ | Drain-source voltage |  |  | 55 | V |
| $\mathrm{V}_{\text {DGR }}$ | Drain-gate voltage | $\mathrm{R}_{\mathrm{GS}}=20 \mathrm{k} \Omega$ |  | 55 | V |
| $\pm \mathrm{V}_{\text {GS }}$ | Gate-source voltage |  |  | 10 | V |
| $\mathrm{I}_{\mathrm{D}}$ | Drain current (DC) | $\mathrm{T}_{\text {sp }}=25^{\circ} \mathrm{C}$ | - | 5.5 | A |
| $\mathrm{I}_{\text {D }}$ | Drain current (DC) | On PCB in Fig. 19 $\mathrm{T}_{\mathrm{amb}}=25^{\circ} \mathrm{C}$ | - | 2.6 | A |
| $\mathrm{I}_{\mathrm{D}}$ | Drain current (DC) | On PCB in Fig. 19 | - | 1.6 | A |
| $\mathrm{I}_{\mathrm{PM}}$ | Drain current (pulse peak value) | $\mathrm{T}_{\text {sp }}^{\text {amb }}=25^{\circ}{ }^{\circ} \mathrm{C}$ | - | 30 | A |
| $\mathrm{P}_{\text {tot }}$ | Total power dissipation | $\mathrm{T}_{\text {sp }}=25^{\circ} \mathrm{C}$ | - | 8.3 | W |
| $\mathrm{P}_{\text {tot }}$ | Total power dissipation | On PCB in Fig. 19 <br> $\mathrm{T}_{\text {amb }}=25^{\circ} \mathrm{C}$ | - | 1.8 | W |
| $\mathrm{T}_{\text {stg }}, \mathrm{T}_{\mathrm{j}}$ | Storage \& operating temperature | $\mathrm{a}_{\text {amb }}=25{ }^{\text {c }}$ | - 55 | 150 | c |

## ESD LIMITING VALUE

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
| :--- | :--- | :--- | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{C}}$ | Electrostatic discharge capacitor <br> voltage | Human body model <br> $(100 \mathrm{pF}, 1.5 \mathrm{k} \Omega)$ | - | 2 | kV |

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## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | TYP. | MAX. | UNIT |
| :--- | :--- | :--- | :---: | :---: | :---: |
| $R_{\text {th } j \text {-sp }}$ | From junction to solder point <br> $R_{\text {th } j \text {-amb }}$ | From junction to ambient | Mounted on any PCB | 12 | 15 |
| Mounted on PCB of Fig. 18 | - | 70 | K/W |  |  |

## STATIC CHARACTERISTICS

$\mathrm{T}_{\mathrm{j}}=25^{\circ} \mathrm{C}$ unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {(BR) }}$ ( ${ }^{\text {ds }}$ | Drain-source breakdown | $\mathrm{V}_{\mathrm{GS}}=0 \mathrm{~V} ; \mathrm{I}_{\mathrm{D}}=0.25 \mathrm{~mA}$ | 55 |  | - | V |
| $\mathrm{V}_{\text {GS (TO) }}$ | Gate threshold voltage | $\mathrm{V}_{\text {DS }}=\mathrm{V}_{G S} ; \mathrm{I}_{\mathrm{D}}=1 \mathrm{~mA} \quad \mathrm{~T}_{\mathrm{j}}=-55^{\circ} \mathrm{C}$ | 50 10 | 15 | 2.0 | V |
|  |  | $\mathrm{V}_{\mathrm{DS}}=\mathrm{V}_{\mathrm{GS}} ; \mathrm{l}_{\mathrm{D}}=1 \mathrm{~mA}$ | 0.6 | 1.5 | 2.0 | V |
|  |  | $\mathrm{V}_{\text {DS }}=55 \mathrm{~V} \cdot \mathrm{~V}_{\text {GS }}=0 \mathrm{~V} \cdot \quad \mathrm{~T}_{\mathrm{j}}=-55^{\circ} \mathrm{C}$ | - | 0.05 | 2.3 | $\checkmark$ |
| $\mathrm{I}_{\text {DSs }}$ | Zero gate voltage drain current | $\mathrm{V}_{\mathrm{DS}}=55 \mathrm{~V} ; \mathrm{V}_{\mathrm{GS}}=0 \mathrm{~V}$; | - | 0.05 | 10 | $\mu \mathrm{A}$ |
| $\mathrm{I}_{\text {GSS }}$ | Gate source leakage current | $\mathrm{V}_{\mathrm{GS}}= \pm 5 \mathrm{~V}$ | - | 0.02 | 100 1 | $\mu \mathrm{A}$ |
|  |  | $\mathrm{T}_{\mathrm{j}}=150^{\circ} \mathrm{C}$ | - | - | 5 | $\mu \mathrm{A}$ |
| $\begin{array}{\|l}  \pm \mathrm{V}_{\text {(BR)GSS }} \\ \mathrm{R}_{\mathrm{DS}(\mathrm{ON})} \end{array}$ | Gate source breakdown voltage | $\mathrm{V}_{\text {GS }}= \pm 1 \mathrm{~mA}$ | 10 | 120 | 150 | V |
|  | Drain-source on-state resistance | $\mathrm{V}_{\mathrm{GS}}=5 \mathrm{~V} ; \mathrm{I}_{\mathrm{D}}=5 \mathrm{~A} \quad \mathrm{~T}_{\mathrm{j}}=150^{\circ} \mathrm{C}$ | - | 120 | 150 277 | $\mathrm{m} \Omega$ $\mathrm{m} \Omega$ |

## DYNAMIC CHARACTERISTICS

$\mathrm{T}_{\mathrm{mb}}=25^{\circ} \mathrm{C}$ unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| :--- | :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{g}_{\mathrm{is}}$ | Forward transconductance | $\mathrm{V}_{\mathrm{DS}}=25 \mathrm{~V} ; \mathrm{I}_{\mathrm{D}}=5 \mathrm{~A} ; \mathrm{T}_{\mathrm{j}}=25^{\circ} \mathrm{C}$ | 3 | 5 | - | S |
| $\mathrm{C}_{\text {iss }}$ | Input capacitance | $\mathrm{V}_{\mathrm{GS}}=0 \mathrm{~V} ; \mathrm{V}_{\mathrm{DS}}=25 \mathrm{~V} ; \mathrm{f}=1 \mathrm{MHz}$ | - | 250 | 330 | pF |
| $\mathrm{C}_{\text {ons }}$ | Output capacitance |  | - | 65 | 80 | pF |
| $\mathrm{C}_{\text {Iss }}$ | Feedback capacitance |  | - | 35 | 50 | pF |
| $\mathrm{t}_{\text {don }}$ | Turn-on delay time | $\mathrm{V}_{\mathrm{DD}}=30 \mathrm{~V} ; \mathrm{I}_{\mathrm{D}}=5 \mathrm{~A} ;$ | - | 11 | 17 | ns |
| $\mathrm{t}_{\mathrm{f}}$ | Turn-on rise time | $\mathrm{V}_{\mathrm{GS}}=5 \mathrm{~V} ; \mathrm{R}_{\mathrm{G}}=10 \Omega ;$ | - | 38 | 60 | ns |
| $\mathrm{t}_{\text {doff }}$ | Turn-off delay time | Turn-off fall time | $\mathrm{T}_{\mathrm{j}}=25^{\circ} \mathrm{C}$ | - | 25 | 38 |
| $\mathrm{t}_{\mathrm{f}}$ | ns |  |  |  |  |  |

## REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

$T_{j}=-55$ to $175^{\circ} \mathrm{C}$ unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| :--- | :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\mathrm{DR}}$ | Continuous reverse drain | $\mathrm{T}_{\mathrm{sp}}=25^{\circ} \mathrm{C}$ | - | - | 5.5 | A |
| $\mathrm{I}_{\mathrm{DRM}}$ | current | Pulsed reverse drain current | $\mathrm{T}_{\text {sp }}=25^{\circ} \mathrm{C}$ | - | - | 30 |
| $\mathrm{~V}_{\mathrm{SD}}$ | Diode forward voltage | $\mathrm{I}_{\mathrm{F}}=2 \mathrm{~A} ; \mathrm{V}_{\mathrm{GS}}=0 \mathrm{~V}$ | A |  |  |  |
| $\mathrm{t}_{\mathrm{r}}$ | Reverse recovery time | $\mathrm{I}_{\mathrm{F}}=2 \mathrm{~A} ;-\mathrm{dl} \mathrm{I}_{\mathrm{F}} / \mathrm{dt}=100 \mathrm{~A} / \mu \mathrm{s} ;$ | - | 43 | - | ns |
| $\mathrm{Q}_{\mathrm{rr}}$ | Reverse recovery charge | $\mathrm{V}_{\mathrm{GS}}=-10 \mathrm{~V} ; \mathrm{V}_{\mathrm{R}}=30 \mathrm{~V}$ | - | 0.85 | 1.1 | V |

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## AVALANCHE LIMITING VALUE

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| :--- | :--- | :--- | :---: | :---: | :---: | :---: |
| W $_{\text {DSS }}$ | Drain-source non-repetitive <br> unclamped inductive turn-off <br> energy | $\mathrm{I}_{\mathrm{D}}=1.9 \mathrm{~A} ; \mathrm{V}_{\mathrm{DD}} \leq 25 \mathrm{~V} ;$ <br> $\mathrm{V}_{\mathrm{GS}}=5 \mathrm{~V} ; \mathrm{R}_{\mathrm{GS}}=50 \Omega ; \mathrm{T}_{\mathrm{sp}}=25^{\circ} \mathrm{C}$ | - | - | 15 | mJ |



Fig.1. Normalised power dissipation. $P D \%=100 \cdot P_{D} / P_{D 25{ }^{\circ} \mathrm{C}}=f\left(T_{\text {sp }}\right)$


Fig.2. Normalised continuous drain current. $I D \%=100 \cdot I_{D} / I_{D 25{ }^{\circ} \mathrm{C}}=f\left(T_{s p}\right)$; conditions: $V_{G S} \geq 5 \mathrm{~V}$


Fig.3. Safe operating area. $T_{s p}=25^{\circ} \mathrm{C}$ $I_{D} \& I_{D M}=f\left(V_{D S}\right) ; I_{D M}$ single pulse; parameter $t_{p}$


Fig.4. Transient thermal impedance.
$Z_{t h j-s p}=f(t) ;$ parameter $D=t_{p} / T$

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Fig.5. Typical output characteristics, $T_{j}=25^{\circ} \mathrm{C}$. $I_{D}=f\left(V_{D S}\right)$; parameter $V_{G S}$


Fig.6. Typical on-state resistance, $T_{j}=25^{\circ} \mathrm{C}$. $R_{D S(O N)}=f\left(I_{D}\right)$; parameter $V_{G S}$


Fig.7. Typical transfer characteristics. $I_{D}=f\left(V_{G S}\right)$; conditions: $V_{D S}=25 \mathrm{~V}$; parameter $T_{j}$


Fig.8. Typical transconductance, $T_{j}=25{ }^{\circ} \mathrm{C}$. $g_{t s}=f\left(I_{D}\right)$; conditions: $V_{D S}=25 \mathrm{~V}$


Fig.9. Normalised drain-source on-state resistance. $a=R_{D S(O N)} / R_{D S(O N) 25{ }^{\circ} \mathrm{C}}=f\left(T_{j}\right) ; I_{D}=5 \mathrm{~A} ; V_{G S}=5 \mathrm{~V}$


Fig.10. Gate threshold voltage.
$V_{G S(T O)}=f\left(T_{j}\right) ;$ conditions: $I_{D}=1 \mathrm{~mA} ; V_{D S}=V_{G S}$

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Fig.11. Sub-threshold drain current.
$I_{D}=f\left(V_{G S}\right)$; conditions: $T_{j}=25^{\circ} \mathrm{C} ; V_{D S}=V_{G S}$


Fig.12. Typical capacitances, $C_{i s s}, C_{\text {oss }}, C_{\text {rss }}$. $C=f\left(V_{D S}\right)$; conditions: $V_{G S}=0 \quad V ; f=1 \mathrm{MHz}$


Fig.13. Typical turn-on gate-charge characteristics. $V_{G S}=f\left(Q_{G}\right)$; conditions: $I_{D}=5$ A; parameter $V_{D S}$


Fig.14. Typical reverse diode current.
$I_{F}=f\left(V_{S D S}\right)$; conditions: $V_{G S}=0 \quad \mathrm{~V}$; parameter $T_{j}$


Fig.15. Normalised avalanche energy rating.

$$
W_{\text {DSs }} \%=f\left(T_{s p}\right) ; \text { conditions: } I_{D}=1.9 \mathrm{~A}
$$

Fig.16. Avalanche energy test circuit.

$$
W_{D S S}=0.5 \cdot L I_{D}^{2} \cdot B V_{D S S} /\left(B V_{D S S}-V_{D D}\right)
$$

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Fig.17. Switching test circuit.

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PRINTED CIRCUIT BOARD


Fig.18. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 $\mu \mathrm{m}$ thick).

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## MECHANICAL DATA



Fig. 19. SOT223 surface mounting package.

## Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to surface mounting instructions for SOT223 envelope.
3. Epoxy meets UL94 V0 at 1/8".

## TrenchMOS ${ }^{\text {TM }}$ transistor Logic level FET

 BUK98150-55
## DEFINITIONS

| Data sheet status |  |
| :--- | :--- |
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one <br> or more of the limiting values may cause permanent damage to the device. These are stress ratings only and <br> operation of the device at these or at any other conditions above those given in the Characteristics sections of <br> this specification is not implied. Exposure to limiting values for extended periods may affect device reliability. |
| Application information |  |
| Where application information is given, it is advisory and does not form part of the specification. |  |
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