NEC

TFT COLOR LCD MODULE

NL10276AC28-01

36 cm (14.1 type), 1024 × 788 pixels, FULL-COLOR, MULTI-SCAN FUNCTION INCORPORATED BACKLIGHT WITH INVERTER

DESCRIPTION

NL10276AC28-01 is a TFT (thin film transistor) active matrix color liquid crystal display (LCD) comprising amorphous silicon TFT attached to each signal electrode, a driving circuit and a backlight. NL10276AC28-01 has a built-in backlight with inverter.

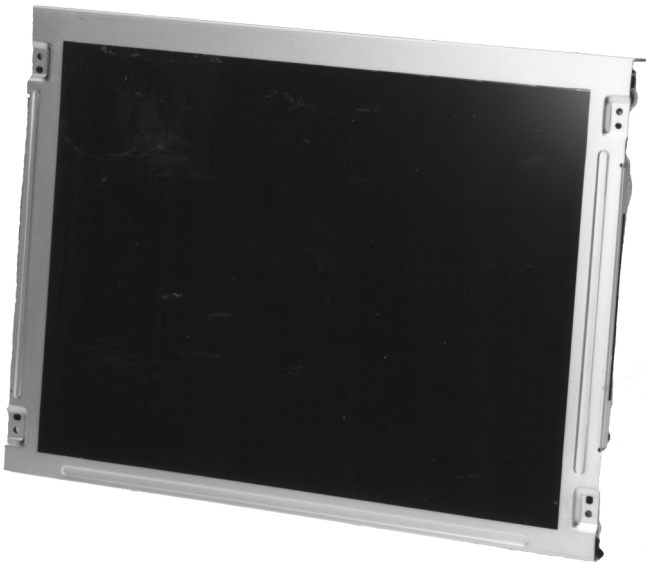
The 36cm diagonal display area contains 1024 × 768 pixels and can display full-color (more than 16 million colors simultaneously).

FEATURES

- High luminance and Low reflection
- Analog RGB signals
- Multi-scan function: e.g., XGA, SVGA, VGA, VGA-TEXT, PC-9801, MAC
- Incorporated edge-light type backlight with inverter (Two lamps)

APPLICATIONS

- Engineering workstation(EWS), Desk-top type of PC
- Display terminals for control system
- Monitors for process controller



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STRUCTURE AND FUNCTIONS

A color TFT (thin film transistor) LCD module is comprised of a TFT liquid crystal panel structure, LSIs for driving the TFT array, and a backlight assembly. The TFT panel structure is created by sandwiching liquid crystal material in the narrow gap between a TFT array glass substrate and a color filter glass substrate. After the driver LSIs are connected to the panel, the backlight assembly is attached to the backside of the panel.

RGB (red, green, blue) data signals from a source system is modulated into a form suitable for active matrix addressing by the onboard signal processor and sent to the driver LSIs which in turn addresses the individual TFT cells.

Acting as an electro-optical switch, each TFT cell regulates light transmission from the backlight assembly when activated by the data source. By regulating the amount of light passing through the array of red, green, and blue dots, color images are created with clarity.

OUTLINE OF CHARACTERISTICS (at room temperature)

Display area	285.696 (H) × 214.272 (V) mm
Drive system	a-Si TFT active matrix
Display colors	Full-color
Number of pixels	1024 × 768
Pixel arrangement	RGB vertical stripe
Pixel pitch	0.279 (H) × 0.279 (V) mm
Module size	330.0 (H) × 255.0 (V) × 19.0 typ. (D) mm
Weight	1220 g (typ.)
Contrast ratio	150:1 (typ.)

Viewing angle (more than the contrast ratio of 10:1)

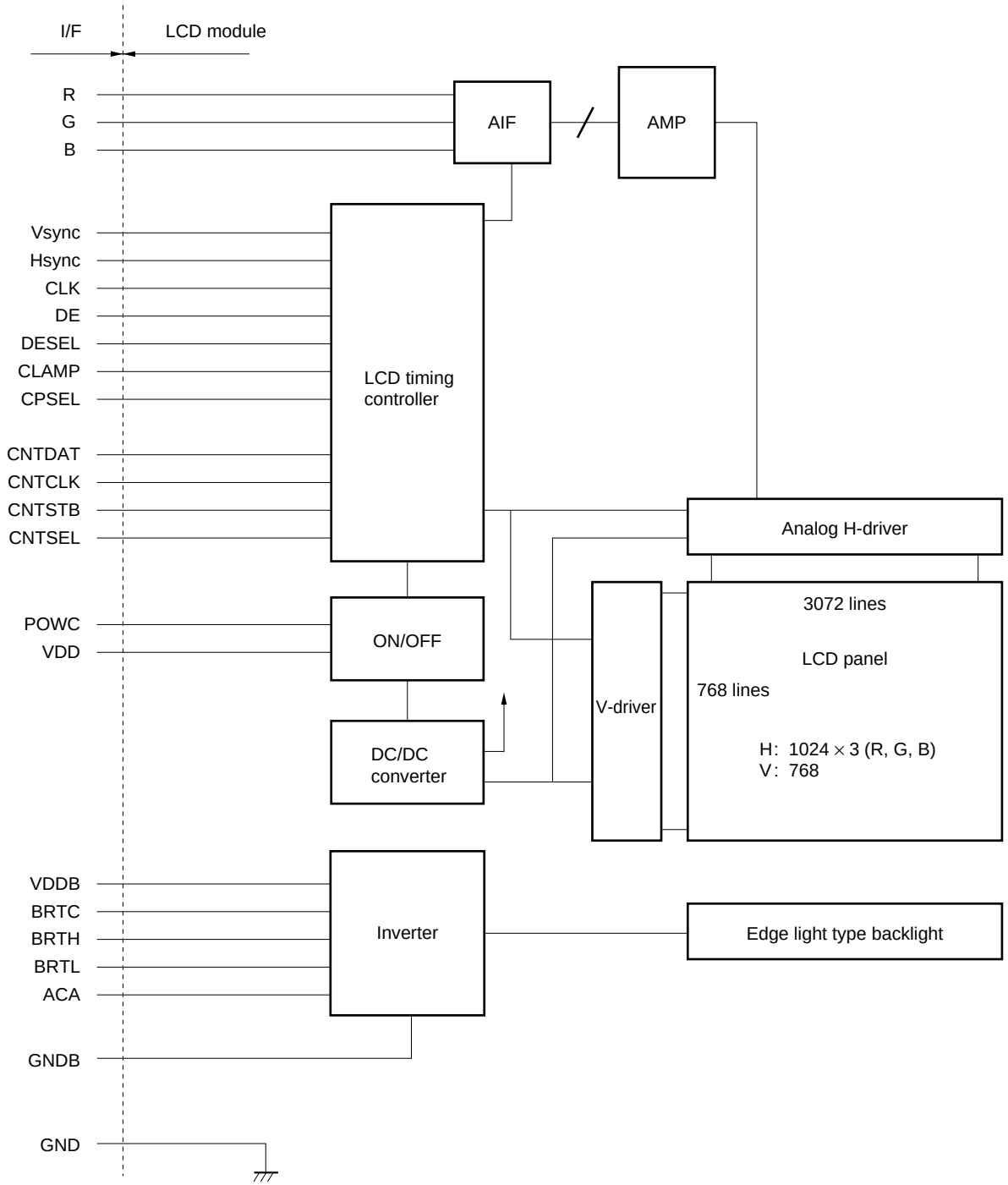
- Horizontal : 50° (typ., left side, right side)
- Vertical : 15° (typ., up side), 30° (typ., down side)

Designed viewing direction

- Wider viewing angle with contrast ratio : down side (6 o'clock)
- Wider viewing angle without image reversal : up side (12 o'clock)
- Optimum grayscale (γ= 2.2) : –5° (typ.)

Color gamut	35 % (min. At center, To NTSC)
Response time	40 ms (max.), "white" to "black"
Luminance	200 cd/m^2 (typ.)
Signal system	Analog RGB signals, Synchronous signals (Hsync, Vsync), Dot clock (CLK)
Supply voltage	12 V, 12 V (Logic/LCD driving, Backlight)
Backlight	Edge light type: Two cold cathode fluorescent lamps with inverter
Power consumption	15.0 W (typ.)

BLOCK DIAGRAM



Note Frame is not connected to GND and GNDB.

SPECIFICATIONS

GENERAL SPECIFICATIONS

Item	Contents	Unit
Module size	330.0 ± 0.5 (H) × 255.0 ± 0.5 (V) × 20.0 (max.) (D)	mm
Display area	285.696 (H) × 214.272 (V)	mm
Number of dots	1024 × 3 (H) × 768 (V)	dots
Pixel pitch	0.279 (H) × 0.279 (V)	mm
Dot pitch	0.093 (H) × 0.279 (V)	mm
Pixel arrangement	RGB (Red, Green, Blue) vertical stripe	—
Display colors	full-color	color
Weight	1250 (max.)	g

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit	Remarks
Supply voltage	VDDB	–0.3 to +14	V	Ta = 25 °C
	VDD	–0.3 to +14	V	
Logic input voltage	Vin1	–0.3 to +5.5	V	Ta = 25 °C VDD = 12 V
R, G, B input voltage	Vin2	–6.0 to +6.0	V	
CLK input voltage	Vin3	–7.0 to +7.0	V	
BRTL input voltage	Vin4	–0.3 to +1.5	V	
Storage temp.	Tst	–20 to +60	°C	—
Operating temp.	Top	0 to +50	°C	Module surface[Note]
Humidity (no condensation)	≦ 95 % relative humidity			Ta ≦ 40 °C
	≦ 85 % relative humidity			40 < Ta ≦ 50 °C
	Absolute humidity shall not exceed Ta = 50 °C, 85 % relative humidity level.			Ta > 50 °C

Note Measured at the LCD panel

ELECTRICAL CHARACTERISTICS

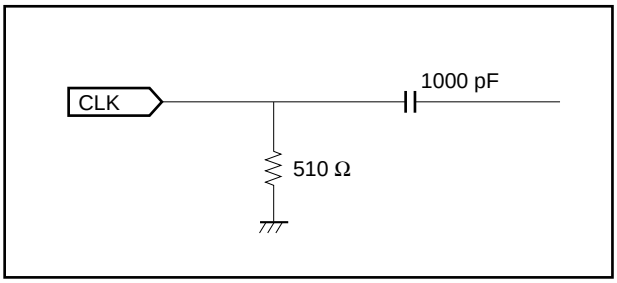
(1) Logic, LCD driving, Backlight

(Ta = 25 °C)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	VDDB	11.4	12.0	12.6	V	for backlight
	VDD	11.4	12.0	12.6	V	for Logic and LCD driving
Logic input “L” voltage	ViL	0	—	0.8	V	TTL level
Logic input “H” voltage	ViH	2.2	—	5.25	V	
CLK input voltage	ViCLK	0.6	—	1.0	Vp-p	for CLK
CLK DC input level	ViDCCLK	–4.5	—	+4.5	V	
Logic input “L” current 1	IiL1	–1080	—	—	μA	for CNTSEL and CPSEL for POWC
Logic input “H” current 1	IiH1	—	—	10	μA	
Logic input “L” current 2	IiL2	–260	—	—	μA	for BRTC
Logic input “H” current 2	IiH2	—	—	820	μA	
Logic input “L” current 3	IiL3	–500	—	—	μA	for ACA
Logic input “H” current 3	IiH3	—	—	340	μA	
Logic input “L” current 4	IiL4	–10	—	—	μA	for except above terminals
Logic input “H” current 4	IiH4	—	—	130	μA	
Supply current[Note]	IDDB	—	710	900	mA	VDDB = 12.0 V (Max. luminance)
	IDD	—	530	800	mA	VDD = 12.0 V

Note Dot- checkered pattern

(2) CLK input equivalent circuit

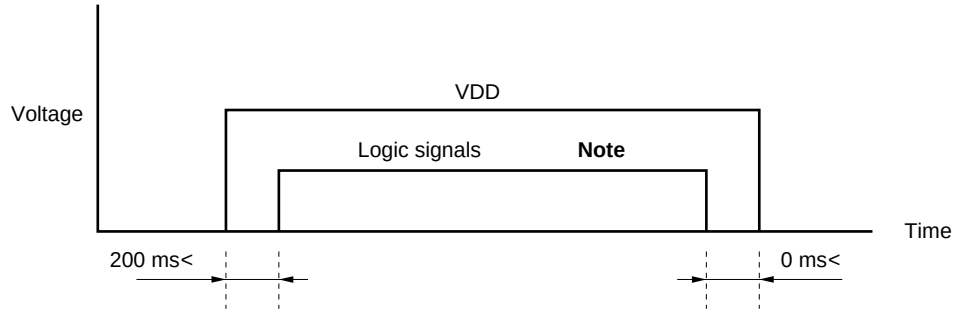


(3) Video signal (R, G, B) input

(Ta = 25 °C)

Item	Min.	Typ.	Max.	Unit	Remarks
Maximum amplitude (white - black)	0 (black)	—	0.7 (white)	Vp-p	—
DC input level (black)	–3.5	—	+3.5	V	—

SUPPLY VOLTAGE SEQUENCE



Note Synchronous signal, Control signals

CAUTION
Wrong power sequence may damage to the module.

(1) Logic signals (synchronous signals and control signals) should be "0" voltage (V), when VDD is not input. If higher than 0.3 V is input to signal lines, the internal circuit will be damaged.
(2) LCD module will shut down the power supply of driving voltage to LCD panel internally, when one of CLK, Hsync, Vsync, DE (at DE mode) is not input more than 90 ms typically. As the display data are unstable in this period, the display is disordered. But the backlight works correctly event this period. So the backlight ON/OFF should be controlled by BRTC signal.
(3) The ON/OFF switching of backlight while logic signals are supplied. The backlight power supply (VDDB) is not related to the power supply sequence. However, unstable data will be displayed when the backlight power is turned ON/OFF with no logic signals.
(4) Keep POWC signal "L" more than 200 ms after the power supply (VDD) is input, if POWC signal is controlled.
(5) Analog RGB input are independent from this power supply sequence.

INTERFACE PIN CONNECTION

(1) CN1

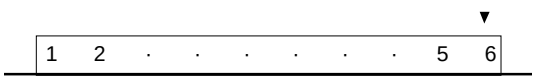
Part No. : MRF03-6R-SMT
Adaptable socket : MRF03-2 × 6P-1.27 (For cable type) or MRF03-6PR-SMT (For board to board type)
Supplier : HIROSE ELECTRIC CO.,LTD. (coaxial type)

Coaxial cable : UL20537PF75VLAS
Supplier : HITACHI CO., LTD.

Note A coaxial cable shield should be connected with GND.

Pin No.	Symbol	Pin No.	Symbol
1	B	4	Vsync
2	G	5	Hsync
3	R	6 ▼	CLK

Figure from socket view



(2) CN2

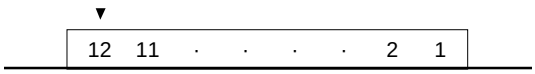
Part No. : IL-Z-12PL1-SMTY

Adaptable socket : IL-Z-12S-S125C3

Supplier : Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	VDD	7	N.C.
2	VDD	8	N.C.
3	GND	9	DESEL
4	GND	10	GND
5	POWC	11	GND
6	GND	12 ▼	DE

Figure from socket view



(3) CN3

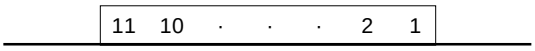
Part No. : IL-Z-11PL1-SMTY

Adaptable socket : IL-Z-11S-S125C3

Supplier : Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	VDDB	7	ACA
2	VDDB	8	BRTC
3	VDDB	9	BRTH
4	GNDB	10	BRTL
5	GNDB	11 ▼	N.C.
6	GNDB		

Figure from socket view



Note N.C. (No connection) should be open.

(4) CN4

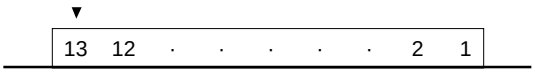
Part No. : IL-Z-13PL1-SMTY

Adaptable socket : IL-Z-13S-S125C3

Supplier : Japan Aviation Electronics Industry Limited (JAE)

Pin No.	Symbol	Pin No.	Symbol
1	GND	8	CLAMP
2	CNTSEL	9	GND
3	CNTDAT	10	N.C.
4	CNTSTB	11	GND
5	GND	12	N.C.
6	CNTCLK	13 ▼	GND
7	CPSEL		

Figure from socket view



Note N.C. (No connection) should be open.

(5) CN5

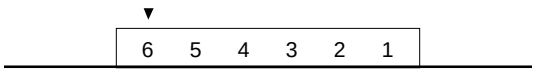
Part No. : IL-Z-6PL-SMTY

Adaptable socket : IL-Z-6S-S125C3

Supplier : Japan Aviation Electronics Industry Limited (JAE)

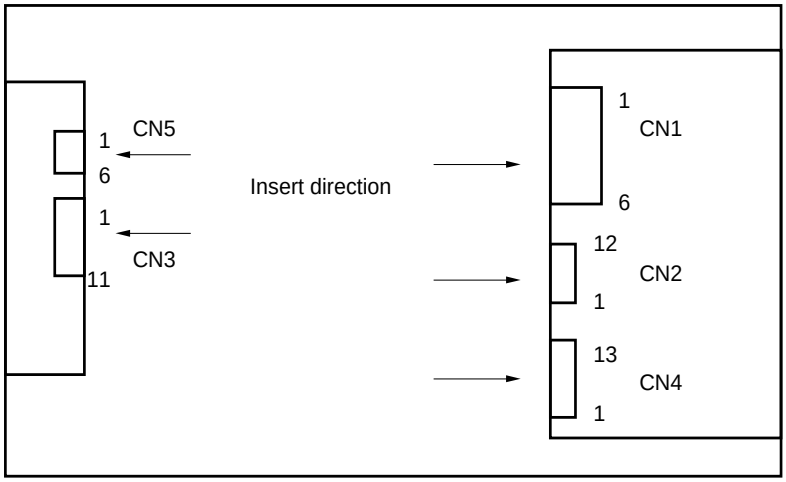
Pin No.	Symbol	Pin No.	Symbol
1	GNDB	4	BRTC
2	GNDB	5	BRTH
3	ACA	6 ▼	BRTL

Figure from socket view



Note CN5 should be open in case of CN3 is used.

Rear view

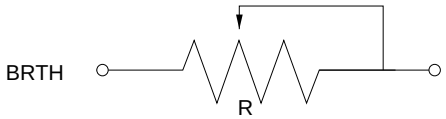


PIN FUNCTION

Symbol	I/O	Logic	Description
CLK	Input	Negative	Dot clock input. (ECL level) This timing-signal is for display data.
Hsync	Input	Negative	Horizontal synchronous signal input (TTL level)
Vsync	Input	Negative	Vertical synchronous signal input (TTL level)
R	Input	—	Red video signal input (0.7 Vp-p, 75 Ω)
G	Input	—	Green video signal input (0.7 Vp-p, 75 Ω)
B	Input	—	Blue video signal input (0.7 Vp-p, 75 Ω)
POWC	Input	Positive	Power control signal (TTL level) "H" or "Open" : Logic and LCD power are on. "L" : Logic and LCD power are off. When POWC is "L" , serial communication data is clear. Please set again. **Note 1**
DESEL	Input	Positive	DE function select signal (TTL level) "H": DE mode, "L" or "Open": Fixed mode
DE	Input	Positive	Data enable signal input (TTL level) 1. Back-porch becomes free, when DESEL is "H". 2. Back-porch becomes fix, when DESEL is "L". Then DE should be fixed "H" or "L".
CNTSEL	Input	—	Display control signal in case of serial communications. (TTL level) "H" or "Open": Default , "L": External control Serial communications set external control up.
CNTDAT	Input	Positive	Display control data (TTL level) Detail of CNTDAT is mentioned in **FUNCTIONS**.
CNTCLK	Input	Positive	CLK for display control data (TTL level) Detail of CNTDAT is mentioned in **FUNCTIONS**.
CNTSTB	Input	Positive	Latch pulse for display control data (TTL level) Detail of CNTDAT is mentioned in **FUNCTIONS**.
CPSEL	Input	—	Clamp signal function select signal (TTL level) "H" or "Open": Default, "L": CLAMP signal is possible.
CLAMP	Input	Negative	Clamp timing signal of black level (TTL level) This mode works in CPSEL = "L".
ACA	Input	Positive	Luminance control signal (TTL level) "H" or "Open": Normal luminance "L" : Low luminance (1/2 of normal luminance)
BRTC	Input	Positive	Backlight ON/OFF control signal (TTL level) "H" or "Open": Backlight ON, "L": Backlight OFF
BRTH	Input	—	Variable resistor control (**Note 2**) or Voltage control (**Note 3**)
BRTL			
VDD	—	—	Power supply for Logic and LCD driving +12 V (±5 %)
VDDB	—	—	Power supply for backlight. +12 V (±5 %)
GND	—	—	Signal ground for Logic and LCD driving (Connect to a system ground)
GNDB	—	—	Ground for backlight. GNDB is not connected to the flame ground of LCD module.

Notes 1. When POWC is "L" logic input signal is all "0 V". If input more than "0.3 V", inside circuits of the LCD module may be broken.

2. The variable resistor for luminance control should be 10 kΩ type, and zero point of the resistor correspond to the minimum of luminance.



Maximum luminance (100 %) : R = 10 kΩ
Minimum luminance (50 %) : R = 0 Ω

Mating variable resistor: 10 kΩ ±5 %, B curve

3. If luminance is controlled by BRTH/BRTL input voltage, at first BRTH is "0 V", and BRTL input voltage controls brightness. When BRTL input voltage is "1 V" the luminance become maximum, and when BRTL input voltage is "0 V", the luminance becomes minimum.

FUNCTIONS

This LCD module has following functions by serial data input (table 1)

(1) Expansion mode : See table 2 and **EXPANSION FUNCTION**
(2) Display position control (VERTICAL) : See table 3
(3) Display position control(HORIZONTAL): See table 6
(4) CLK delay control : See table 4
(5) CLK fall/rise synchronous change : See table 5

Set up the following items to work the above functions

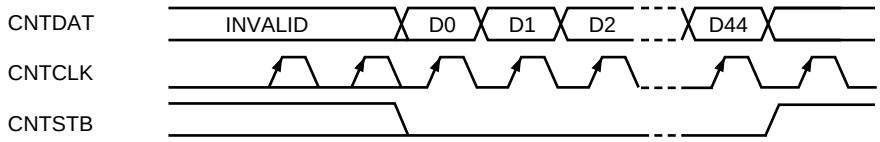
(A) CLK counts of horizontal period : See table 7
(B) CLK frequency range : See table 8

HOW TO USE THE ABOVE FUNCTIONS

If CNTSEL is “L”, the above functions are valid. (CNTSEL is “H” or open, default values are valid.) After serial data are transferred, the data is latched by CNTSTB. Once, the data is latched, the above functions are effective. Please keep CNTSTB to be “L” during transferring data. Input data can be changed during power on, but LCD display may be disturbed. When the serial data are changed, we recommend that the backlight power is off using BRTC function.

SERIAL COMMUNICATION TIMING AND WAVEFORM

SERIAL COMMUNICATION TIMING



Parameter	Symbol	Min.	Max.	Unit	Remark
CLK pulse-width	Twck	50	—	ns	CNTCLK
CLK frequency	Fclk	—	5	MHz	
DATA set-up-time	Tdst	50	—	ns	CNTDAT
DATA hold-time	Tdhl	50	—	ns	
Latch pulse-width	Twlp	50	—	ns	CNTSTB
Latch set-up-time	T1st	50	—	ns	
Rise/fall time	Tr, Tf	—	50	ns	CNT xxx

SERIAL COMMUNICATION WAVEFORM

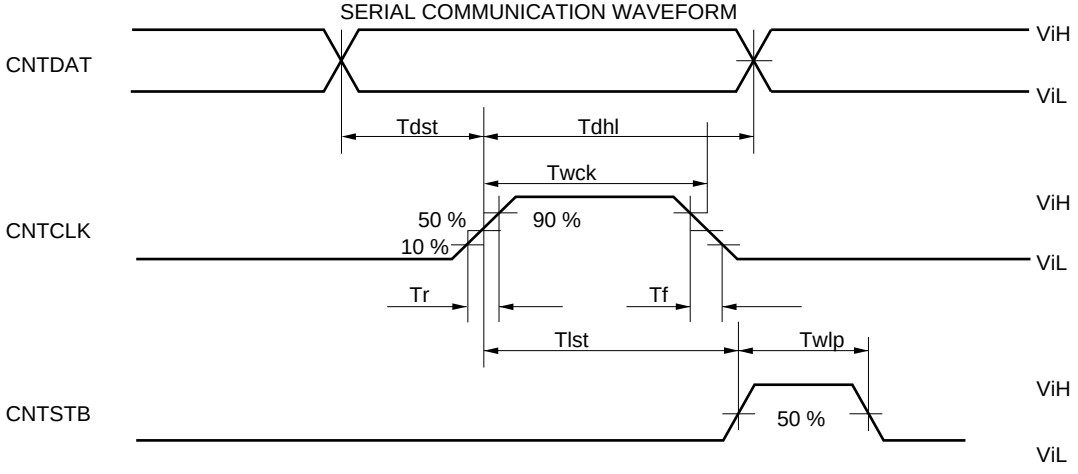


Table 1. CNTDAT Composition

DATA	DATA name	Function	
D0	VEX3	Expansion mode	See table 2
D1	VEX2	Expansion mode	
D2	VEX1	Expansion mode	
D3	VEX0	Expansion mode	
D4	VD10	Vertical display position (MSB)	See table 3
D5	VD9	Vertical display position	
D6	VD8	Vertical display position	
D7	VD7	Vertical display position	
D8	VD6	Vertical display position	
D9	VD5	Vertical display position	
D10	VD4	Vertical display position	
D11	VD3	Vertical display position	
D12	VD2	Vertical display position	
D13	VD1	Vertical display position	
D14	VD0	Vertical display position (LSB)	
D15	DELAY6	CLK delay (MSB)	See table 4
D16	DELAY5	CLK delay	
D17	DELAY4	CLK delay	
D18	DELAY3	CLK delay	
D19 20	DELAY2- ELAY1	LK delay	
21	ELAY0	LK delay (LSB)	
22	KS	LK reverse signal	ee table 5
23	D8	orizontal display position (MSB)	ee table 6
24	D7	orizontal display position	
25	D6	orizontal display position	
26	D5	orizontal display position	
27	D4	orizontal display position	
28	D3	orizontal display position	
29	D2	orizontal display position	
30	D1	orizontal display position	
31	D0	orizontal display position (LSB)	
32	SE10	LK count of horizontal period (MSB)	ee table 7
33	SE9	LK count of horizontal period	
34	SE8	LK count of horizontal period	
35	SE7	LK count of horizontal period	
36	SE6	LK count of horizontal period	
37	SE5	LK count of horizontal period	
38	SE4	LK count of horizontal period	
39	SE3	LK count of horizontal period	
40	SE2	LK count of horizontal period	
41	SE1	LK count of horizontal period	
42	SE0	LK count of horizontal period (LSB)	
43	OD1	LK frequency select	ee table 8
44	OD0	LK frequency select	

Table 2. Display Mode (VEX3 to VEX0: 4 bit)

VEX3	VEX2	VEX1	VEX0	Vertical magnification	Display mode	Display image
0	0	0	0	1	XGA	Standard **Note**
0	0	0	1	1.25	SVGA	See **DISPLAY IMAGE**
0	0	1	0	1.6	TEXT	
0	0	1	1	—	Prohibit	
0	1	0	1	—	Prohibit	
0	1	1	0	—	Prohibit	
0	1	1	1	—	Prohibit	
1	0	0	0	—	Prohibit	
1	0	0	1	1.2	Prohibit	
1	0	1	0	—	832 × 624 (MAC)	
1	0	1	1	—	Prohibit	
1	1	0	0	—	Prohibit	
1	1	0	1	—	Prohibit	
1	1	1	0	—	Prohibit	
1	1	1	1	—	Prohibit	
					Prohibit	

Note When CNTSEL is “H” or “Open”, display mode is XGA.

Table 3. Vertical Position (VD10 to VD0: 11 bit)

VD10	VD9	VD8	VD7	VD6	VD5	VD4	VD3	VD2	VD1	VD0	Vertical position [H] **Note 1**
0	0	0	0	0	0	0	0	0	0	0	Prohibit
0	0	0	0	0	0	0	0	0	0	1	Prohibit
0	0	0	0	0	0	0	0	0	1	0	Prohibit
0	0	0	0	0	0	0	0	0	1	1	Prohibit
0	0	0	0	0	0	0	0	1	0	0	4
0	0	0	0	0	0	0	0	1	0	1	5
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	0	1	2045
1	1	1	1	1	1	1	1	1	1	0	2046
1	1	1	1	1	1	1	1	1	1	1	2047 **Note 2**

Notes 1. This is horizontal line number for effective VIDEO signal from Vsync-fall.

2. The maximum vertical position is Vsync total.

3. When CNTSEL is “H” or “Open”, vertical position is fixed at 35 [H].

Table 4. CLK Delay (DELAY6 to DELAY0: 7 bit)

DELAY[6..0]	Delay	Unit
00H	7.0	ns
01H	7.6	ns
02H	8.2	ns
03H	8.8	ns
04H	9.4	ns
05H	10.0	ns
06H	10.5	ns
07H	11.2	ns
08H	11.8	ns
09H	12.4	ns
0AH	13.0	ns
0BH	13.7	ns
0CH	14.2	ns
0DH	14.8	ns
0EH	15.3	ns
0FH	15.9	ns
10H	16.6	ns
11H	17.2	ns
12H	17.8	ns
13H	18.4	ns
14H	18.9	ns
15H	19.5	ns
16H	20.1	ns
17H	20.7	ns
18H	21.4	ns
19H	22.0	ns
1AH	22.6	ns
1BH	23.2	ns
1CH	23.8	ns
1DH	24.4	ns
1EH	24.9	ns
1FH	25.6	ns
20H	26.3	ns
21H	26.9	ns
22H	27.4	ns
23H	28.1	ns
24H	28.5	ns
25H	29.1	ns
26H	29.7	ns
27H	30.3	ns
28H	31.0	ns
29H	31.6	ns
2AH	32.2	ns
2BH	32.8	ns
2CH	33.3	ns
2DH	33.9	ns
2EH	33.4	ns
2FH	35.1	ns

DELAY[6..0]	Delay	Unit
30H	35.6	ns
31H	36.1	ns
32H	36.8	ns
33H	37.5	ns
34H	37.9	ns
35H	38.5	ns
36H	39.1	ns
37H	39.7	ns
38H	40.4	ns
39H	41.0	ns
3AH	41.5	ns
3BH	42.1	ns
3CH	42.6	ns
3DH	43.2	ns
3EH	43.8	ns
3FH	44.4	ns
40H	45.0	ns
41H	45.6	ns
42H	46.2	ns
43H	46.8	ns
44H	47.3	ns
45H	47.8	ns
46H	48.4	ns
47H	49.0	ns
48H	49.6	ns
49H	50.2	ns
4AH	50.8	ns
4BH	51.4	ns
4CH	51.9	ns
4DH	52.6	ns
4EH	53.1	ns
4FH	53.7	ns
50H	54.5	ns
51H	55.0	ns
52H	55.6	ns
53H	56.3	ns
54H	56.8	ns
55H	57.4	ns
56H	57.9	ns
57H	58.5	ns
58H	59.2	ns
59H	59.8	ns
5AH	60.4	ns
5BH	61.1	ns
5CH	61.6	ns
5DH	62.2	ns
5EH	62.7	ns
5FH	63.3	ns

DELAY[6..0]	Delay	Unit
60H	64.0	ns
61H	64.7	ns
62H	65.3	ns
63H	66.0	ns
64H	66.5	ns
65H	67.1	ns
66H	67.7	ns
67H	68.3	ns
68H	68.9	ns
69H	69.5	ns
6AH	70.1	ns
6BH	70.7	ns
6CH	71.2	ns
6DH	71.9	ns
6EH	72.4	ns
6FH	73.1	ns
70H	73.6	ns
71H	74.2	ns
72H	74.8	ns
73H	75.4	ns
74H	75.9	ns
75H	76.5	ns
76H	77.0	ns
77H	77.7	ns
78H	78.3	ns
79H	79.0	ns
7AH	79.6	ns
7BH	80.2	ns
7CH	80.8	ns
7DH	81.4	ns
7EH	81.9	ns
7FH	82.5	ns

Notes 1. When CNTSEL is “H” or “Open”, DELAY[6..0] is fixed at 00H.

2. This delay value is typical value at Ta = 25 °C. By changing ambient temperature and power supply, the delay will be changed.

Please set up a preferable display position. See the following references.

<1> Variation of CLK delay by temperature drift. (as reference) The temperature constant of CLK delay is 0.2 %/°C.

Calculated example:

In case of delay time is 20 ns at Ta = 25 °C;

(a) In case Ta rising to 50 °C.

Increase of delay time → (50 °C – 25 °C) × 0.002 × 20 ns = +1 ns

So, the total delay time is 21 ns at Ta = 50 °C.

(b) In case Ta falling to 0 °C.

Decrease of delay time → (0 °C – 25 °C) × 0.002 × 20 ns = –1 ns

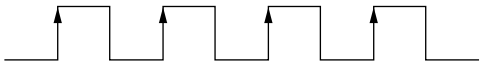
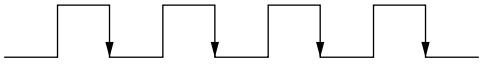
So, the total delay time is 19 ns at Ta = 0 °C.

<2> Variation of CLK delay time against each LCD module. (as reference)

–10.5 % to +14.4 %

	MOD setting			
	0, 0	0, 1	1, 0	1, 1
The upper limit of CLK delay; DELAY[6..0]	Prohibit	59H	6BH	7FH

Table 5. CLK Reverse Signal

CKS	FUNCTION
0	DATA is sampled on rising edge of CLK 
1	DATA is sampled on falling edge of CLK 

Note When CNTSEL is “H” or “Open”, CKS is “0”.

Table 6. Display Horizontal Position (HD8 to HD0: 9 bit)

HD8	HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0	Horizontal position [CLK] **Note 1**
0	0	0	0	0	0	0	0	0	Prohibit
0	0	0	0	0	0	0	0	1	Prohibit
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
0	0	1	1	1	1	1	1	1	Prohibit
0	1	0	0	0	0	0	0	0	64
0	1	0	0	0	0	0	0	1	65
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	0	1	509
1	1	1	1	1	1	1	1	0	510
1	1	1	1	1	1	1	1	1	511

Notes 1. This is CLK number from Hsync-fall to effecting VIDEO signal.

2. When CNTSEL is “H” or “Open”, Horizontal position is set at 296 [CLK].

Table 7. CLK Count of Horizontal Period (HSE10 to HSE0: 11 bit)

HSE10	HSE9	HSE8	HSE7	HSE6	HSE5	HSE4	HSE3	HSE2	HSE1	HSE0	CLK count **Note 1**
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	0	1	2045
1	1	1	1	1	1	1	1	1	1	0	2046
1	1	1	1	1	1	1	1	1	1	1	2047

Notes 1. This is CLK number from Hsync to next Hsync.
2. When CNTSEL is “H” or “Open”, CLK count is set at 1344 [CLK].
3. This CLK count must be equal to CLK count of input signal.

Table 8. CLK Frequency Select (MOD1 to MOD0: 2 bit)

MOD1	MOD0	CLK frequency [MHz]
0	0	Prohibit
0	1	65 to 79
1	0	50 to 65
1	1	20 to 50

Notes 1. Set up the MOD1 and MOD0 complying with input CLK frequency.
2. When CNTSEL is “H” or “Open”, CLK frequency is set 65 to 79 MHz.

EXPANSION FUNCTION

HOW TO USE EXPANSION MODE

Expansion mode is a function to expand screen. For example, VGA signal has 640 × 480 pixels. But, if the display data can expanded to 1.6 times vertically and horizontally, VGA screen image can be displayed fully on the screen of XGA resolution.

This LCD module has the function of expanding vertical direction as shown in Table 1. And expanding horizontal direction is possible by setting input CLK frequency which is equivalent to the magnification. It is necessary to make this CLK outside of this LCD module.

The below image is display example, when DE function is default and HD and VD is set to most suitable frequency. And when DE function is used, HD and VD become default. Adjustment the display to the best position by DE signal. Please adopt this mode after evaluating display quality, because the appearance of expansion mode is happened to become bad some cases.

The followings show display magnifications for each mode.

Input display	Number of pixels	Magnification	
		Vertical	Horizontal **Note**
XGA	1024 × 768	1	1
SVGA	800 × 600	1.25	1.25
VGA	640 × 480	1.6	1.6
VGA text	720 × 400	1.6	1.4
PC9801	640 × 400	1.6	1.6
MAC	832 × 624	1.2	1.2

Note The horizontal magnification multiples the input clock (CLK).
Input CLK = system CLK × horizontal magnification

Example In case of XGA and VGA, CLK frequency can be decided as follows.
XGA: (system CLK (65 MHz)) × 1.0 = 65 MHz
VGA: (system CLK (25.175 MHz)) × 1.6 = 40.28 MHz

SETTING SERIAL DATA

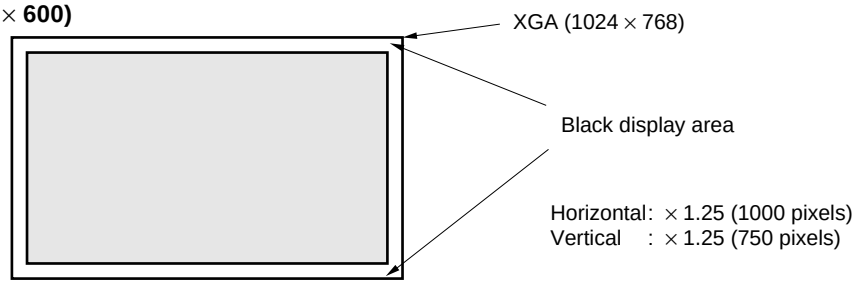
Input signal								Module serial data setting		
Mode	System CLK [MHz]	Hsync [kHz]	Vsync [Hz]	Horizontal		Vertical		HSE	HD	VD
				Count number [CLK]	DSP* [CLK]	Count number [H]	DSP* [H]	Calculation formula		
				(A)	(B)	—	(C)	(A) × Ver. mag.	(B) × Hor. mag.	= (C)
XGA (1024 × 768)	65 75 78.75	48.363 56.476 60.023	60.004 70.069 75.029	1344 1328 1312	296 280 272	806 806 800	35 35 31	(A) × 1	(B) × 1	= (C)
MAC (832 × 624)	57.283	49.725	74.5	1152	288	667	42	(A) × 1.2	(B) × 1.2	
SVGA (800 × 600)	36* 40* 50* 49.5*	35.156 37.879 48.077 46.875	56.25 60.317 72.188 75	1024 1056 1040 1056	200 216 184 240	625 628 666 666	24 27 29 24	(A) × 1.25	(B) × 1.25	
VGA (640 × 480)	25.175* 31.5* 31.5* 30.24*	31.469 37.861 37.5 35.0	59.94 72.809 75 66.667	800 832 840 864	144 168 184 160	525 520 500 525	35 31 19 42	(A) × 1.6	(B) × 1.6	
VGA text (720 × 400)	28.322* 31.5*	31.469 37.927	70.087 85.04	900 936	153 180	449 446	37 45	(A) × 1.4	(B) × 1.4	
PC9801 (640 × 400)	21.053*	24.827	56.432	848	144	440	33	(A) × 1.6	(B) × 1.6	443

***** DSP = Display Start Period. DSP is total of “pulse-width” and “back-porch”.

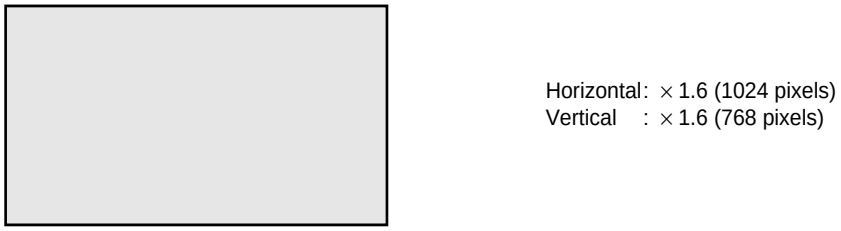
Notes 1. HD and VD are approximate value. Set HD and VD in case of adjusting display to the screen center.
2. The pulse-width of Hsync, Vsync and back-porch are the same as XGA-mode. (Standard-mode).
3. HSE see CLK number of table 7.
4. HD see horizontal position of table 6.
5. VD see vertical position of table 3.

DISPLAY IMAGE

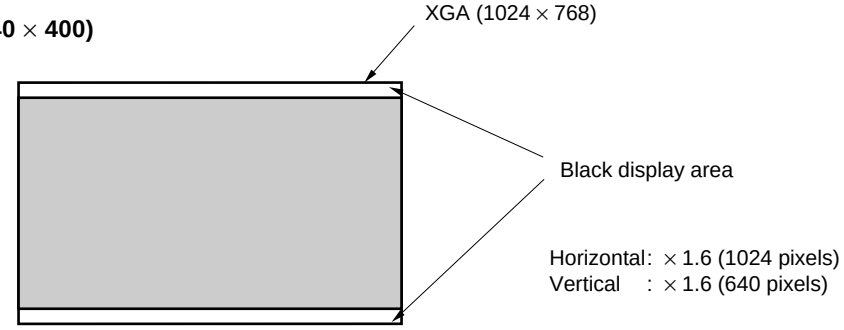
1) SVGA mode (800 × 600)



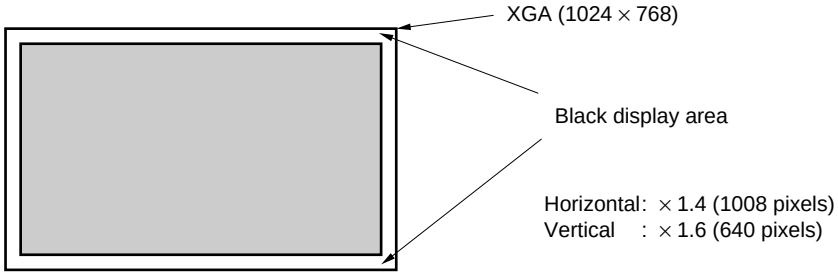
2) VGA mode (640 × 480)



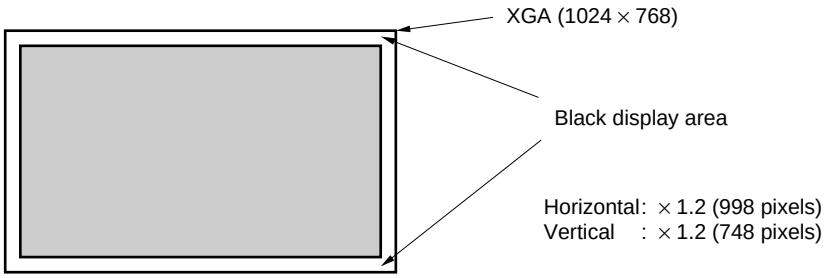
3) PC9801 mode (640 × 400)



4) VGA text mode (720 × 400)



5) 832 × 624 MAC mode (832 × 624)

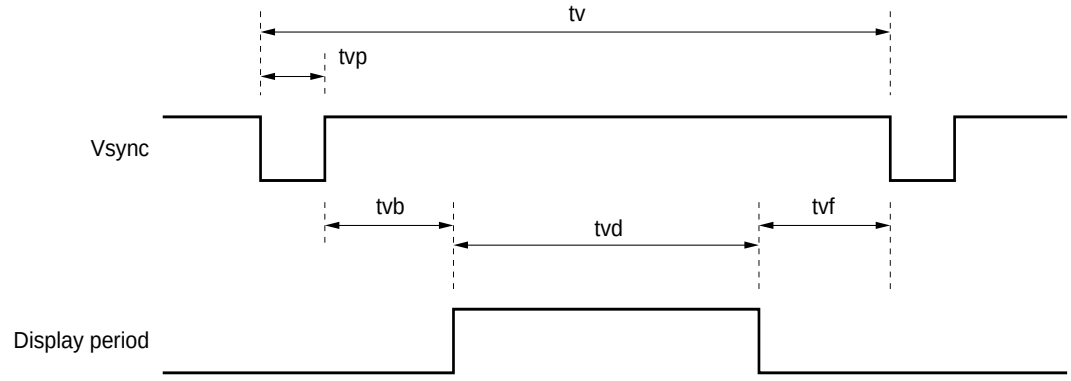


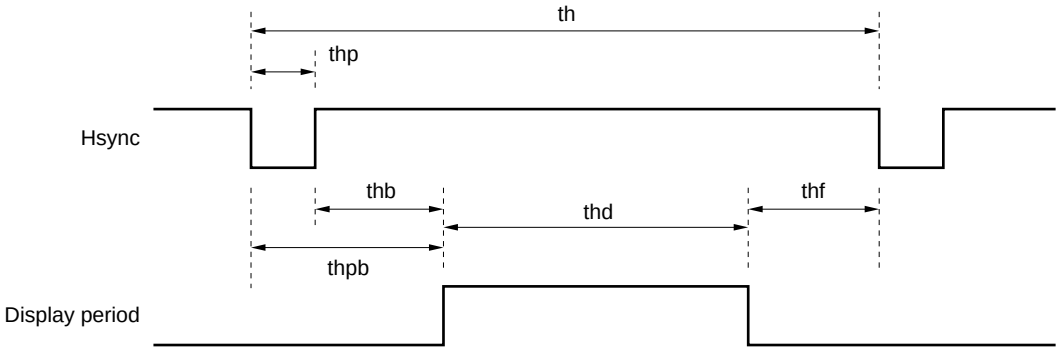
INPUT SIRIAL TIMING

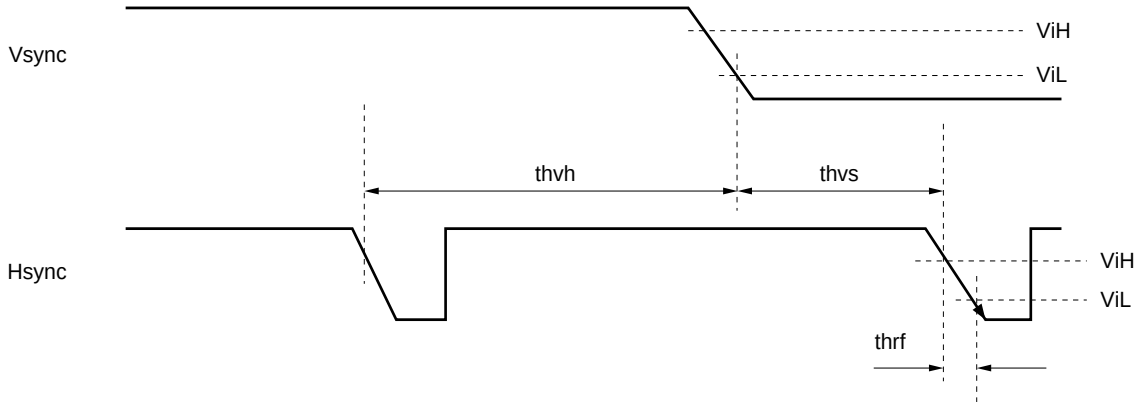
XGA MODE (STANDARD)

	Name	Symbol	Min.	Typ.	Max.	Unit	Remark
CLK	Frequency	1/tc	52.0 —	65.0 15.385	79.0 —	MHz ns	XGA standard
	Rise / Fall	tcrf	—	—	10	ns	—
	Pulse-width	tcl/tc	0.4	0.5	0.6	—	—
Hsync	Period	th	16.0 —	20.677 1344	22.7 —	μs CLK	48.363 kHz (typ.)
	Display	thd	— —	15.754 1024	— —	μs CLK	—
	Front-porch	thf	— 10	0.369 24	— —	μs CLK	—
	Pulse-width	thp	— 16	2.092 136	— —	μs CLK	—
	Back-porch	thb	1.0 44	2.462 160	— —	μs CLK	**Note**
	Pulse-width + Back-porch	thpb	1.8	—	—	μs	—
	Vsync – Hsync timing	thvh	4	—	—	ns	—
		thvs	1	—	—	CLK	—
	Rise / Fall	thrf	—	—	10	ns	—
Vsync	Period	tv	13.3 —	16.665 806	18.5 —	ms H	60.004 Hz (typ.)
	Display	tvd	— —	15.880 768	— —	μs H	—
	Front-porch	tvf	— 1	62.031 3	— —	μs H	—
	Pulse-width	tvp	— 2	124.06 6	— —	μs H	—
	Back-porch	tvb	— 5	599.63 29	— —	μs H	—
DE	Set-up time	tds	2	—	—	ns	—
	Hold time	tdh	4	—	—	ns	—
	Rise / Fall	tdrf	—	—	10.0	ns	—
Analog R, G, B	—	tda	4	—	—	ns	—

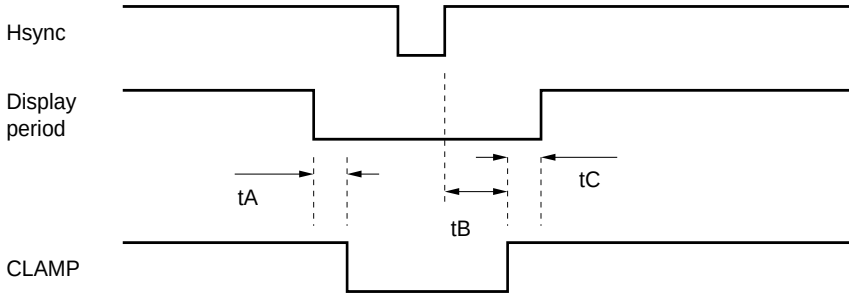
Note Minimum values of Back-porch (thb) must be satisfied with both 1.0 μs and 44 CLK.


tv
tvp
Vsync
tvb
tvd
tvf
Display period


th
thp
Hsync
thb
thd
thf
thpb
Display period


Vsync
ViH
ViL
thvh
thvs
Hsync
ViH
ViL
thrf

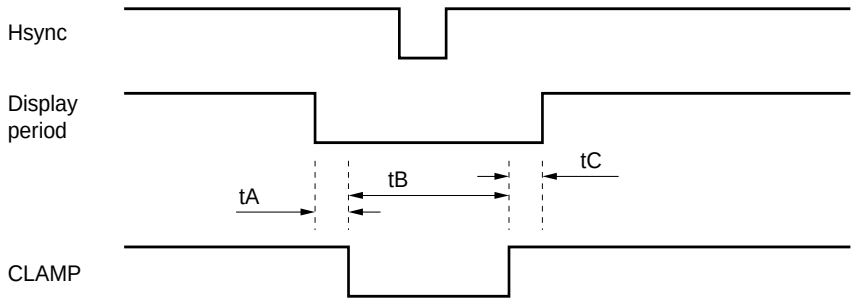
TIMING FOR GENERATING CLAMP SIGNAL INTERNALLY



MOD1	MOD2	tA [CLK]	tB [CLK]	tC [ns]
0	0	Prohibit		
0	1	44	32	200 minimum
1	0	34	22	
1	1	28	18	

Note Exclude noises on analog R, G, B signal, because analog R, G, B signals are the black level reference during CLAMP = "L". If noises are on the analog signals, luminance level of display is changed and the display becomes bad.

TIMING FOR INPUTING CLAMP SIGNAL FROM OUTSIDE



Item	Min.	Typ.	Max.	Unit	Remarks
tA	0.1	—	—	μs	—
tB	0.3	—	—	μs	—
tC	0.2	—	—	μs	—

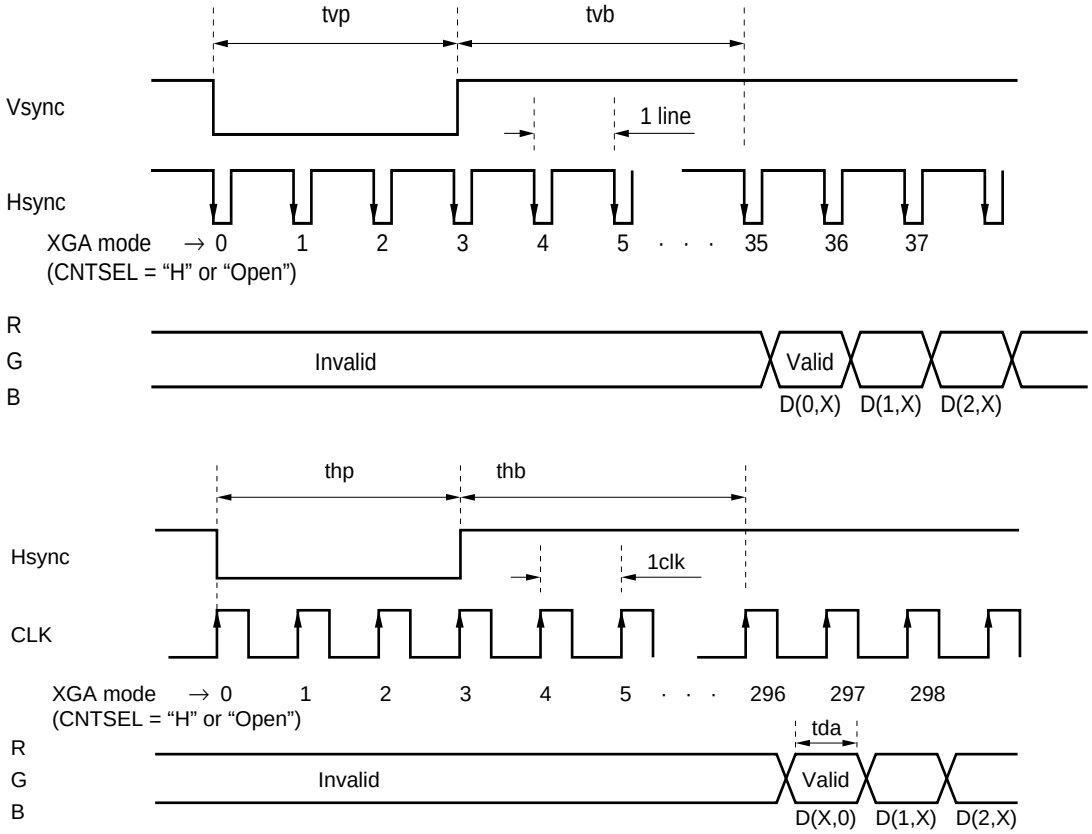
Note Exclude noises on analog R, G, B signal, because analog R, G, B signals are the black level reference during CLAMP = "L". If noises are on the analog signals, luminance level of display is changed and the display becomes bad.

INPUT SIGNAL AND DISPLAY POSITION

FOR DESEL = “L” (XGA standard timing)

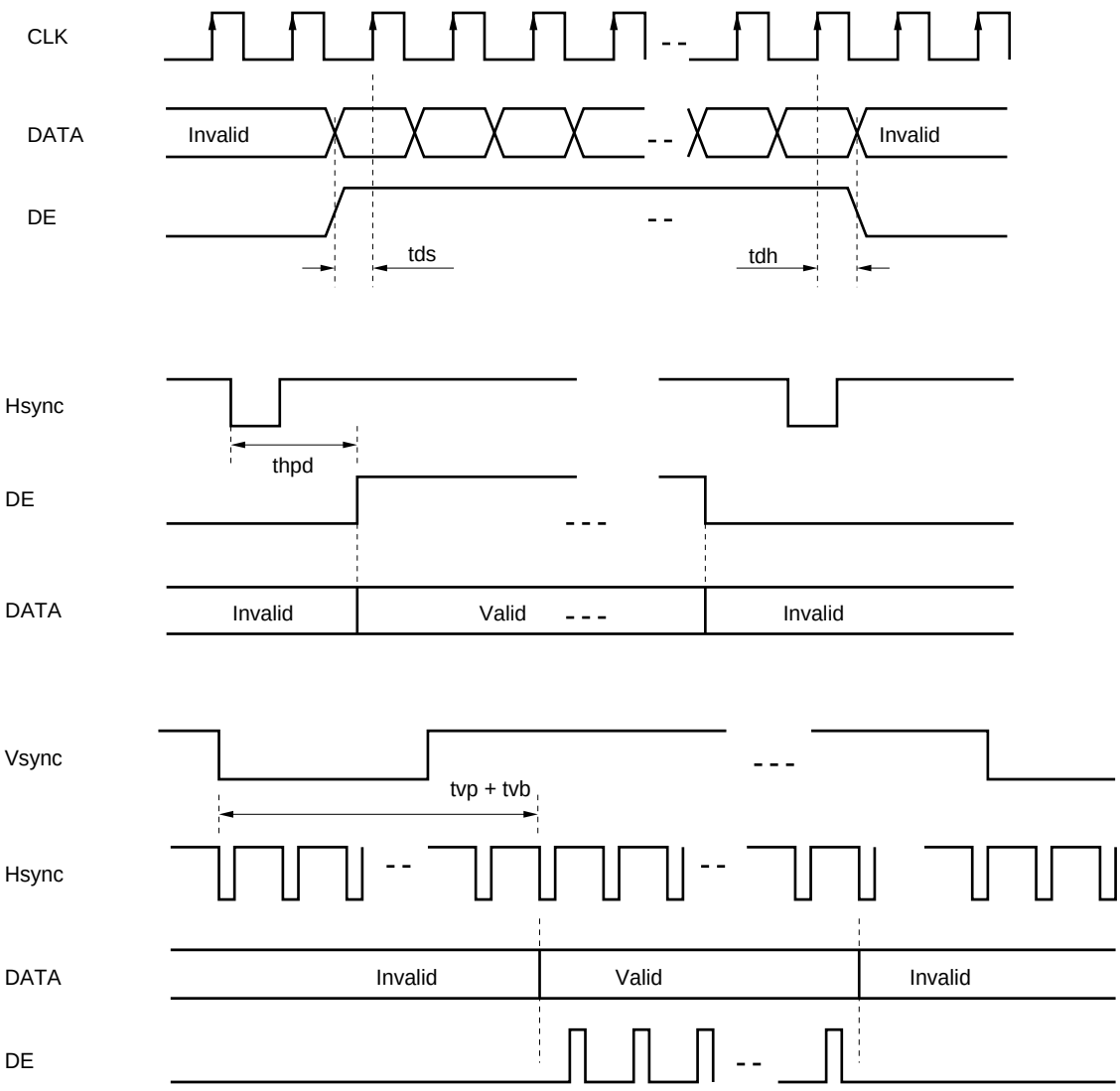
Pixels

D(0,0)	D(0,1)	D(0,2)	· · · · · ·	D(0,1023)
D(1,0)	D(1,1)	D(1,2)	· · · · · ·	D(1,1023)
D(2,0)	D(2,1)	D(2,2)	· · · · · ·	D(2,1023)
. . . .	. . . .	. . . .		. . . .
D(767,0)	D(767,1)	D(767,2)	· · · · · ·	D(767,1023)



Note tda should be minimum 4ns

FOR DESEL= “H”


CLK
DATA
Invalid
Invalid
DE
tds
tdh
Hsync
thpd
DE
DATA
Invalid
Valid
Invalid
Vsync
tvp + tvb
Hsync
DATA
Invalid
Valid
Invalid
DE

OPTICAL CHARACTERISTICS

(Ta = 25 °C, VDD = 12 V, VDDB = 12 V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Contrast ratio	CR	Best contrast angle θR = 0°, θL = 0°, θU = 7°, White/Black	—	300	—	—	**Note 1**
		γ = 2.2 viewing angle θR = 0°, θL = 0°, θD = 5°, White/Black	80	150	—	—	
Luminance	Lvmax	White	150	200	—	cd/m^2	**Note 2**
Luminance uniformity	—	White	—	—	1.30	—	**Note 3**
Color gamut	C	θR = 0°, θL = 0°, θU = 0°, θD = 0°, At center, to NTSC	35	—	—	%	—
Response time	tpd	White to black	—	—	40	ms	**Note 4**

Reference data

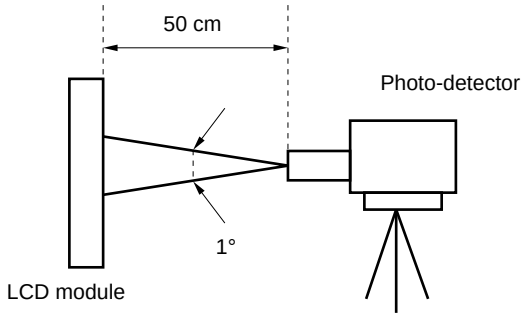
(Ta = 25 °C, VDD = 12 V, VDDB = 12 V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Viewing angle range	θ R	CR > 10, θU = 0°, θD = 0°		40	50	—	deg.
	θ L			40	50	—	deg.
	θ U	CR > 10, θR = 0°, θL = 0°		10	15	—	deg.
	θ D			25	30	—	deg.
Luminance control range by BRTH/BRTL	—	Maximum luminance: 100 %	ACA = H	—	20 to 100	—	%
			ACA = L	—	40 to 100	—	

Notes 1. The contrast ratio is calculated by using the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance with all pixels in “white”}}{\text{Luminance with all pixels in “black”}}$$

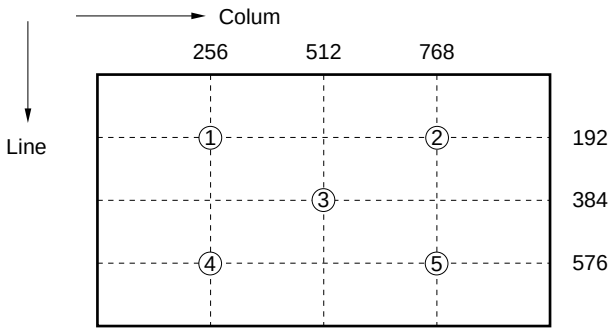
2. The luminance is measured after 20 minutes from the module works, with all pixels in “white”. The typical value is measured after luminance saturation.



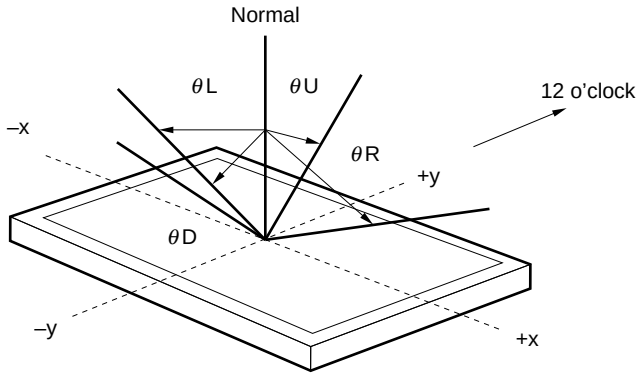
3. Luminance uniformity is calculated by using the following formula.

$$\text{Luminance uniformity} = \frac{\text{Maximum luminance}}{\text{Minimum luminance}}$$

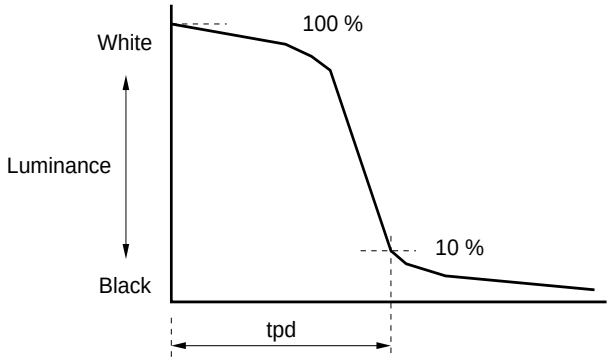
The luminance is measured at near the five points shown below.



Notes 4. Definitions of viewing angle are as follows.



5. Definitions of response time is as follows.
Photo-detector out put signal is measured when the luminance changes “white” to “black”. Response time is the time between 10 % and 100 % of the photo-detector output amplitude.



Next figures and sentence are very important. Please understand these, then read the text of a book.

CAUTION	This figure is a mark that you will get hurt and/or the module will have damages when you make a mistake to operate.

	This figure is a mark that you will get an electric shock when you make a mistake to operate.
	This figure is a mark that the LCD module will give out smoke or catch fire when you make a mistake to operate.
	This figure is a mark that you will get hurt when you make a mistake to operate.

 **CAUTION**

Do not touch an inverter --on which is stuck a caution label-- while the LCD module is under the operation, because of dangerous high voltage.

(1) Caution when taking out the module
   <1> Pick the pouch only, in taking out module from a carrier box.

(2) Caution for handling the module
   <1> As the electrostatic discharges may break the LCD module, handle the LCD module with care against electrostatic discharges.
   <2>  As the LCD panel and backlight element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
   <3> As the surface of polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
   <4> Do not pull the interface connectors in or out while the LCD module is operating.
   <5> Put the module display side down on a flat horizontal plane.
   <6> Handle connectors and cables with care.
   <7> When the module is operating, do not lose CLK, Hsync, or Vsync signal. If any one of these signals is lost, the LCD panel would be damaged.
   <8> The torque of mounting screw should be 0.392 N·m (4 Kgf·cm) less.

(3) Caution for the atmosphere
   <1> Dew drop atmosphere should be avoided.
   <2> Do not store and/or operate the LCD module in a high temperature and/or high humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

<3> This module uses cold cathode fluorescent lamps. Therefore, the life time of lamps becomes short conspicuously at low temperature.

<4>  Do not operate the LCD module in a high magnetic field.

(4) Caution for the module characteristics

<1> Do not apply fixed pattern data signal to the LCD module at product aging. Applying fixed pattern for a long time may cause image sticking.

(5) Other cautions

<1> Do not disassemble and/or reassemble LCD module.

<2> Do not readjust variable resistor or switch etc.

<3> When returning the module for repair or etc., please pack the module not to be broken. We recommend to the original shipping packages.

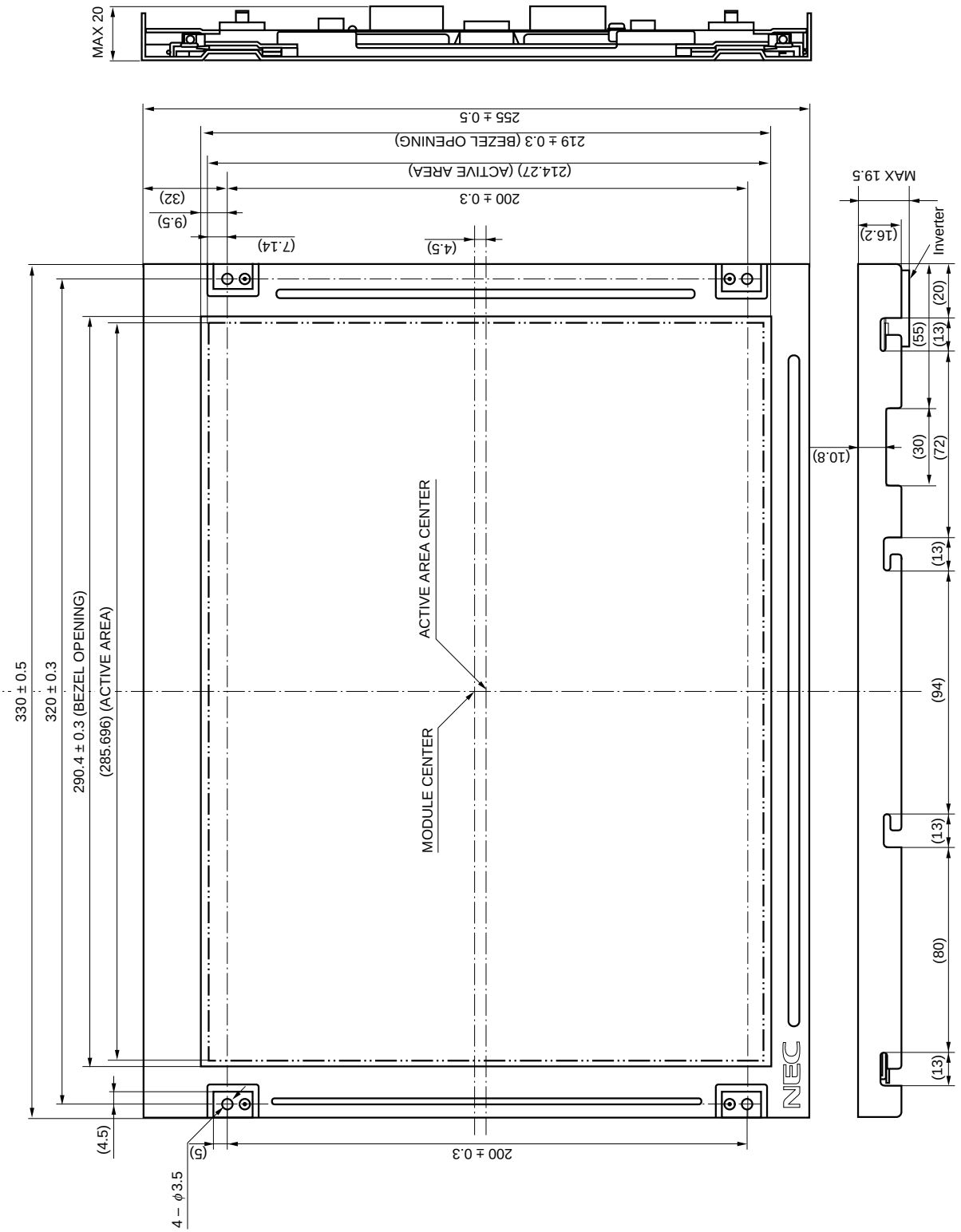
Liquid Crystal Display has the following specific characteristics. There are not defects or malfunctions.

The display condition of LCD module may be affected by the ambient temperature.
The LCD module uses cold cathode tube for backlight. Optical characteristics, like luminance or uniformity, will change during time.

Uneven brightness and/or small spots may be noticed depending on different display patterns.

OUTLINE DRAWING (Unit in mm)

FRONT VIEW

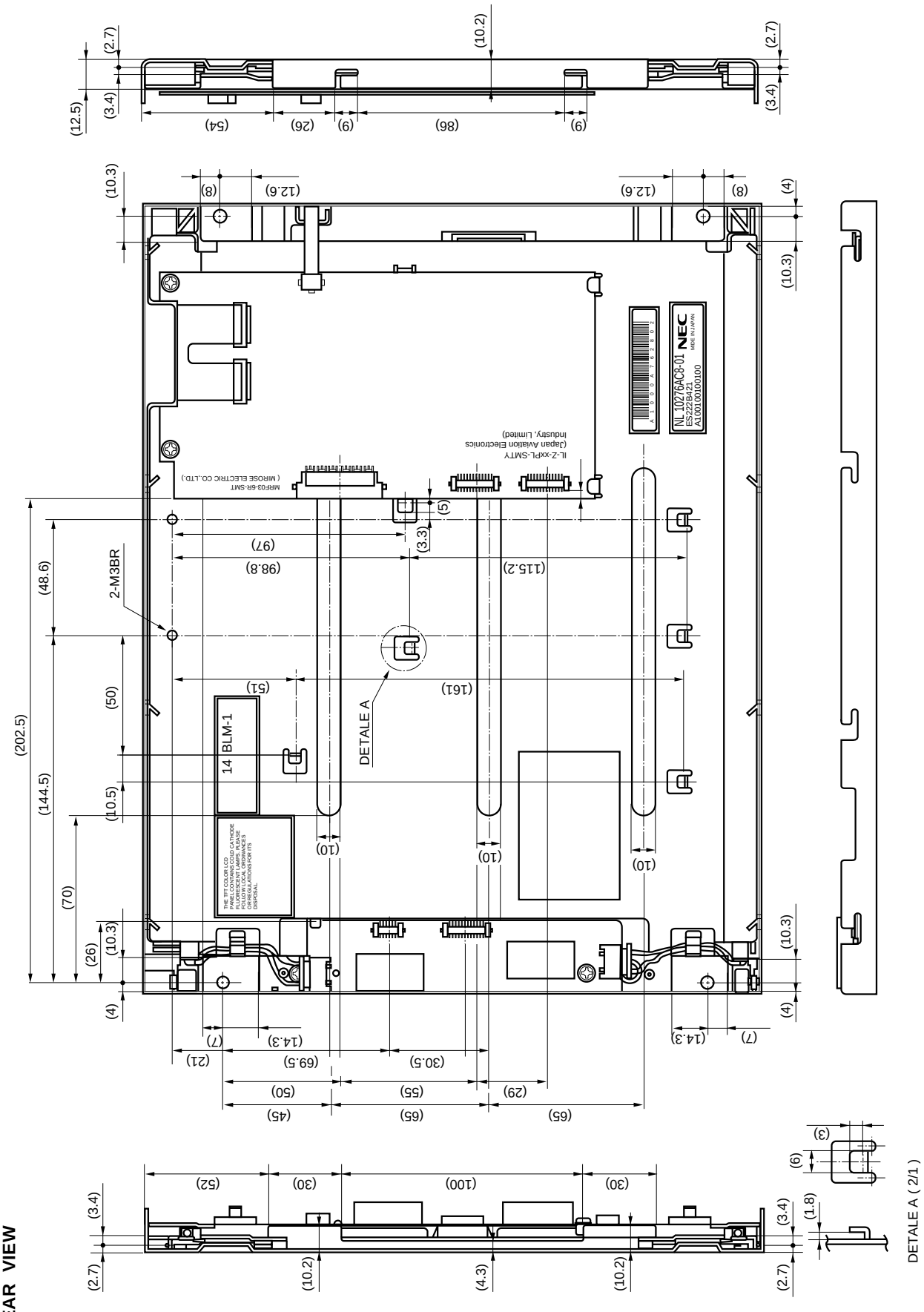


Notes 1. The value in parentheses are for reference.

2. The torque to mounting screw should never exceed 0.392 N·m (4 Kgf·cm).

OUTLINE DRAWING (Unit in mm)

REAR VIEW



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