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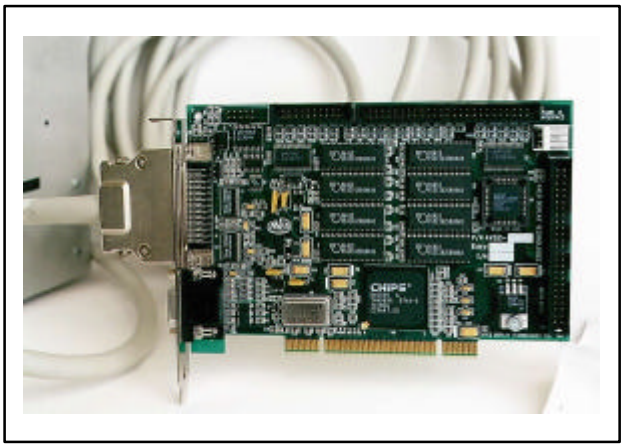
AV555-PCI-LVDS High Performance Flat Panel/CRT Video Sub-System Controller



- **Flat Panel Sub-System Controller for Industrial and LCD Monitor Applications. Single Cable Remote System up to 15M distance.**
- **4MB Memory for XGA and SXGA True Color.**
- **LVDS Interface now supports all DSTN, TFT, and Plasma Panels. 24Bit Data at single pixel per clock up to XGA. 18Bit Dual pixel per clock up to UXGA resolutions.**
- **Enhanced power distribution for Large Format and High-Bright LCD Monitors and Sub-Systems that require 30W of Power or more. Uses internal PC Power supply directly.**
- **RS-232, I2C, General Purpose, and User Programmable I/O.**

Desktop Graphics Performance for LCD's

- 64-Bit Graphics Engine and Memory Interface
- 4MB 40nS EDO Memory
- Windows Acceleration Hardware BITBLT, Line Draw, Cursor, ICONS, Raster OP's.

Multi-Media Accelerator

- Hardware Color Space Conversion, Video Capture, and Scaling. Zoom up to 8x.
- Live Video Windowing and MPEG playback through PCI bus or Multi-media connector.
- Multi-media Connector supports Zoomed Video Input (YUV) or AVED NTSC/PAL Input Daughter card.

Low EMI Design for FCC-B and CE

- LVDS and Double-Shielded SCSI-II interface for minimized radiation and maximum immunity.
- Extensive signal and power filtering.

Flat Panel Sub-System Controller

- RS-232 pass-through and I2C communications for system controls.
- All system power and software controlled sequencing with routing options for local LCD Monitors or Long Distance remote sub-systems.
- User Programmable and General Purpose I/O's. Headers for Stereo Audio or remote PS-2 Keyboard/Mouse functions.
- Interfaces to AVED LVDS-RCVR controller family.

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Robust Digital CMOS Interface

- Switchable 3.3V or 5.0V CMOS 24 and 36 Bit Panel Interfaces.
- Fully EMI filtered. Balanced 24mA drive.
- Additional Sequenced Power on Internal IDC for Direct drive of Large format Panels.

Display Enhancement Hardware

- Extended Color Modulation for 24Bit Color on 18Bit TFT Panels.
- Horizontal and Vertical Stretching so Text and Graphic sub-modes fill entire panel.
- Enhanced Temporal Modulation algorithm (TMED) for True Color on DSTN Panels.

CRT Interface

- Up to UXGA resolutions.
- Plug and Play compatible (DDC1/2B).
- Simultaneous CRT/Flat Panel operation.

Highest Quality Standards

- Manufactured to IPC-610-A.

Specifications

Interface Summary
J1 - 15 Pin CRT Output
J2 - 50 Pin Digital Multi-Media Interface
J3 - 24 Bit Digital CMOS Panel Interface
J4 - 50 Pin External System / LVDS Interface
J5 - 4 Pin Speaker / User Defined I / O
J6 - 10 Pin RS-232 Pass-Through / I2C
J7 - 4 Pin Auxiliary PC Power Input
J8 - 3 Pin General Purpose I / O
J9 - 3 Pin LVDS GPIOTX18 / 19 / 20
J10 - 20 Pin Auxiliary CMOS Panel Interface for 36 Bit Panels

CRT Interface
Analog RGB, .7Vptp into 75 Ohms, Nom.

DDC Interface
DDC 1 / 2B compliant on CRT and External Flat Panel Interface. Upgradable to 2B+ for Plug and Display protocol.

Digital Video Panel Interfaces and Data Bandwidth
24 Bit Digital TTL Panel Interface
36 Bit Dual Pixel Digital TTL Interface
24 Bit LVDS Single Pixel Per Clock
36 Bit LVDS Dual Pixel Per Clock
Max Transmission Clock 68MHz. (135MHz Bandwidth for Dual Pixel Panels Only).
Digital TTL Panel Interface voltages selectable – 3.3V or 5.0V.

Interface Power/Fuse Limits

Fixed +5V	5A
Fixed +12V	3A
Fixed -12V	100mA
Switched +3.3V	1.2A (VDD)
Switched +5V	3A (VDD)
Switched +12V	3A

Note1: Auxiliary PC Power Connector must be connected for Sub-System Power Requirements over 8W.
Note2: Power protected by resettable fuses. If a short condition occurs, wait 5 minutes for fuses to reset.

Video Memory
4MB 40nS EDO, 64 Bit Memory Bus

Video Modes (CRT and TFT LCD)

640x480x16M	75Hz
800x600x16M	75Hz
1024x768x16M	70Hz
1280x1024x16M	60Hz
1600x1200x256	60Hz

Up to 135MHz Pixel Clock Rate.
Up to 55MHz Memory Clock Rate.

Control IC's
Chips and Technology F65555
National DS90C363 / TI SN75LVDS84

Environmental Characteristics
- Backed up with 1 year limited warranty.
- ISO9000 Certification in process.

Humidity: 5% to 95%, Non-condensing.
Ambient Temperature: 0 to 70 C. Operating. -20 to 100 Non-Operating.

EMI
FCC Class B and CE for CRT Interface
External Digital Sub-System Tests performed by OEM for System Result. Preliminary Scans pass to FCC-B / CE levels.
Internal Ribbon Cable Interface Fully EMI Filtered.

Power Consumption
2.8 W (Board Only)

Mechanical Dimensions
Standard 32Bit PCI Short Card Form Factor (106Hx156Lmm)

Software Drivers
Win3.1, Win95, Win98, NT4.0, OS / 2.
Available at www.chips.com.

User Interfaces and Configuration

Jumper Settings
W6 Panel / VDDSAFE Voltage Select
1-2 +5VOLTS
2-3 +3.3VOLTS
W7 Panel Logic Interface Levels
1-2 +5VOLTS
2-3 +3.3VOLTS

Power Distribution Options For External Interface
Default configuration distributes Fixed and Sequenced voltages evenly. To support sub-systems with power consumption above 25W alternate configurations have been designed in.
Optionally the External Power Conductors can be routed to be all Switched Power (for short cables or direct panel interfacing) or all Fixed Power (for Long Distance Remote Systems that must re-regulate and sequence power).

I2C Interface Control
I2C Interface implemented with programmed I / O and transmitted externally over twisted pair and internally on J6. End user must develop communication program. Test Software and Sample Code available from AVED.

General Purpose and Programmed I/O
RS-232 Pass-Through for Host System connection to Remote System.
GPIO1 / 2 - Hardwire or Logic Controlled. GPIO1 I / O Mapped Control: Config Write 3D0H=0CH, 3D0H=02H. Config Read 3D0H=0CH, 3D1H=03H. Operate. Write 3D6=63, Read / Modify Write 3D7[1]. GPIO2 is BKLTENABL.
SPKR+ / -, SPKL+ / - Hardwired Audio or General Purpose I / O twisted pairs.

Ordering Information
Part Number: AV555-LVDS. Must Specify any special requirements and Flat Panel vendor and part number.

Direct Sales
AVED Display Technologies, 14192 Chambers Road, Tustin, CA 92780
Internet: sales@aveddisplay.com Web Site: www.aveddisplay.com **See Web Site for Worldwide Distribution and Sales Representatives**.

U.S. Distribution Sales

All American	800-573-2727
Reptron	800- 800-5441
Wyle	800-283-9953

Technical Support
Visit our Technical Support Center at **www.aveddisplay.com** for detailed installation guides and manuals.

Warranty
AVED Display Technologies (AVED) warrants these products to be free from defects in workmanship and materials under normal use and service and in its original, unmodified condition, for a period of one year from the time of purchase. **All warranties are void if the board is reconfigured or modified without factory authorization**. If the product is found to be defective within the terms of this warranty, AVED's sole responsibility shall be to repair, or at AVED's sole option, to replace the defective product. The product must be returned by the original customer, insured, and shipped prepaid to AVED. **An RMA Number must be obtained from AVED before they will be accepted.** All replaced products become the sole property of AVED Display Technologies.

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**“First in Technology,
First with Products”**

AV555-PCI-LVDS Controller Pin Definitions and I/O Descriptions

Internal 50 Pin IDC Panel Connector (J3)

Description: The Internal 24-Bit Digital CMOS Panel Interface. LC filters on clocks and syncs. Ferrites on all data. Mating connector: 50 pin Dual Row .1" IDC. Logic Levels and VDDSAFE are jumper configurable for either 3.3V or 5.0V operation.

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VDDSAFE	11	FLM (VS)	21	P4	31	P11	41	GND
2	+12VSAFE	12	GND	22	P5	32	GND	42	P18
3	+12VSAFE	13	SHFCLK	23	GND	33	P12	43	P19
4	VDDSAFE	14	GND	24	P6	34	P13	44	GND
5	VDDSAFE	15	P0	25	P7	35	GND	45	P20
6	+12VFUSED	16	P1	26	GND	36	P14	46	P21
7	GND	17	GND	27	P8	37	P15	47	GND
8	M (DE)	18	P2	28	P9	38	GND	48	P22
9	GND	19	P3	29	GND	39	P16	49	P23
10	LP (HS)	20	GND	30	P10	40	P17	50	GND

Auxiliary Internal 20 Pin IDC Panel Connector (J10)

Description: Auxiliary Color Bits for 36-Bit Digital CMOS Interface. Mating Connector: 20 Pin Dual Row .1" IDC.

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	6	P27	11	P30	16	GND
2	P24	7	GND	12	P31	17	P34
3	P25	8	P28	13	GND	18	P35
4	GND	9	P29	14	P32	19	GND
5	P26	10	GND	15	P33	20	GND

External 50 Pin Flat Panel/Sub-System Interface (J3)

Description: The External 50 Pin interface for LVDS Signals and Panel Powers. Designed for use with SCSI-II type connector with Double-Shielded Twisted Pair cable. Bracketed items indicate alternate multiplexed pin operation – allow customer specific changes. Compatibility Note: This interface and connector remain backward compatible with the AVED LVDS Receiver boards in addition to Dual 18 Bit TFT's that have LVDS integrated into them. Mating Connector: Male 50 Pin SCSI-II. Board Mount Connector - Amp P/N:**AMP 787395-5.**

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	11	+5VFUSED	21	I2C_SCL (DTR)	31	TXOUT20+	41	VDDSAFE
2	TXOUT10-	12	+12VFUSED	22	GPIO1 (PROGIO1)	32	TXOUT21+	42	GND
3	TXOUT11-	13	GND	23	+5VFUSED	33	TXOUT22+	43	SDA_RTN/GND (DSR)
4	TXOUT12-	14	+12VSAFE	24	SPKR+	34	TXCLKOUT2+	44	RTS
5	TXCLKOUT1-	15	VDDSAFE	25	SPKL+	35	GND	45	CTS
6	TXOUT20-	16	-12VOLTS	26	GND	36	+12VFUSED	46	SCL_RTN/GND (RI)
7	TXOUT21-	17	+12VFUSED	27	TXOUT10+	37	+12VFUSED	47	GPIO2 (ENABKL)
8	TXOUT22-	18	I2C_SDA (DCD)	28	TXOUT11+	38	GND	48	+5VFUSED
9	TXCLKOUT2-	19	RXD	29	TXOUT12+	39	+12VSAFE	49	SPKR-
10	GND	20	TXD	30	TXCLKOUT1+	40	VDDSAFE	50	SPKL-

Internal 50 Pin IDC Multi-Media Interface Connector (J2)

Description: Multi-Media Interface Connector for video capture port/daughter card. 16Bit YUV (ZV Video) or RGB Data In. Interface Logic Level are 3.3V with 5.0V Tolerant I/O.

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	11	VCLK	21	GND	31	SCL	41	GND
2	+5VFUSED	12	UV6 (R3)	22	UV1 (G4)	32	Y4 (B4)	42	GND
3	GND	13	HREF	23	+12VFUSED	33	GND	43	VREF
4	+5VFUSED	14	UV5 (R2)	24	UV0 (G3)	34	Y3 (B3)	44	GND
5	GND	15	GND	25	+12VFUSED	35	-12VOLTS	45	GND
6	+3.3VOLTS	16	UV4 (R1)	26	Y7 (G2)	36	Y2 (B2)	46	VRDY
7	GND	17	GND	27	GND	37	-12VOLTS	47	GND
8	+3.3VOLTS	18	UV3 (R0)	28	Y6 (G1)	38	Y1 (B1)	48	GND
9	GND	19	GND	29	SDA	39	GND	49	GND
10	UV7 (R4)	20	UV2 (G5)	30	Y5 (G0)	40	Y0 (B0)	50	GND

AV555-PCI-LVDS Controller Pin Definitions and I/O Descriptions (cont.)

10 Pin RS-232 (J6)

Description: The 10 Pin RS-232 Pass-Through connector. Standard PC "AT" connector arrangement and definitions. Note that the default configuration uses DCD, DSR, DTR, RI for I2C interface to external I/O (J4) and must be left disconnected when resistors () are installed. Note: Typical Serial Communications devices such as a mouse or touch-screen controller only require RXD, TXD, RTS, CTS. . Routed to J3 External Interface.

Pin	Signal
1	DCD (I2C_SDA)(R11)
2	DSR (SDA_RTN)(R12)
3	RXD
4	RTS
5	TXD
6	CTS
7	DTR (I2C_SCL) (R13)
8	RI (SCL_RTN) (R14)
9	GND
10	NC

4 Pin Speaker/User Defined I/O Twisted Pair (J5)

Description: Hardwired General purpose I/O suitable for High Level Audio, PS-2 Keyboard/Mouse, power, or whatever. SPKR+/- and SPKL+/- are run as twisted pairs over the external interface. Routed to J3 External Interface. Mating connector: 4 pin Single .1" IDC.

Pin	Signal
1	SPKR+
2	SPKR-
3	SPKL-
4	SPKL+

3 Pin General Purpose I/O (J8)

Description: Hardwired General purpose I/O limited to 5V max. External logic to over-drive 4.7K pull-up. Logic Controlled I/O are also connected: 1. GPIO1 connects to user I/O programmable signal (see above section for programming), GPIO2 connect to ENABKL which is active high Backlight Enable signal. . Routed to J3 External Interface.

Pin	Signal
1	GPIO1
2	GPIO2
3	GND

Auxiliary Power Input Connector (J7)

Description: Power Input from Standard PC Power Supply. Always connect when using Flat Panel or Sub-Systems that consume more than 8 Watts.

Pin	Signal
1	+5VOLTS
2	GND
3	GND
4	+12VOLTS

Key Improvements for AV-555-PCI-LVDS over the AV-550-PCI-LVDS

1. 4MB Memory translates to XGA and SXGA True Color. The 64 Bit HiQVideo Hardware Graphics Controller along with a 64 Bit Memory Bus make this the highest performance AVED Video Controller.

2. LVDS Interface now supports all DSTN and TFT Panel Interfaces. 24 Bit Data at single pixel per clock is now supported up to XGA resolutions. Dual pixel per clock supported up to UXGA resolutions.

3. Enhanced power distribution for Large Format and High-Bright LCD Monitors and Sub-Systems that require 30W of power or more. Can use internal PC Power supply directly. Board power routing options for local LCD Monitors or Long Distance remote sub-systems.

4. Fully Buffered and EMI filtered Digital CMOS Interfaces. For "Internal" ribbon cable connections up to 36 bits wide. High (24mA) Drive allow direct "External" Digital Interfaces as well. In fact, internal CMOS, external LVDS, and CRT interfaces can all be run simultaneously assuming the same panel type.

5. All fixed and programmable powers supplies protected by automatically resettable fuses. Avoids field failures when a momentary short occurs. System will resume once cause of continuous over-current condition is resolved.

6. User programmable I2C capability added to External Interface. OEM application and control software can communicate with external sub-system.

7. Setting for LVDS Panel Types DSTN or TFT as well as clock polarity are controlled by the software video BIOS. A minimum of user configurable jumpers.

AV555-PCI-LVDS Internal Digital CMOS Panel Interface Definition

Description: Selectable 3.3V or 5.0V logic levels. Fully EMI Filtered. Compatibility Note: Internal 50 Pin IDC (J3) is backwards compatible with all other AVED products. Additional 20 Pin IDC (J10) is a new definition and is required for Dual Pixel Per Clock Panel Interfaces. All cable lengths should be kept to a minimum and the maximum amount of grounds from the board carried across to the panel should always be used.

Signal Name	AV555 Internal 50 Pin IDC - J3	AV555 Internal 20 Pin IDC, J10	24 Bit TFT Single Pixel/ Clock	36 bit TFT Dual Pixel/ Clock	12 Bit TFT Dual Pixel/ Clock	24 Bit Color DSTN	16 Bit Color DSTN
+5VOLT FUSED	NC						
VDDSAFE	1,4,5						
+12VSAFE	2,3						
+12 V FUSED	6						
M (DE)	8						
LP (HS)	10						
FLM (VS)	11						
SHFCLK	13						
P0	15		B0	FB0	FB0	UR0	UR0
P1	16		B1	FB1	FB1	UG0	UG0
P2	18		B2	FB2	FB2	UB0	UB0
P3	19		B3	FB3	FB3	LR0	UR1
P4	21		B4	FB4	SB0	LG0	LR0
P5	22		B5	FB5	SB1	LB0	LG0
P6	24		B6	SB0	SB2	UR1	LB0
P7	25		B7	SB1	SB3	UG1	LR1
P8	27		G0	SB2	FG0	UB1	UG1
P9	28		G1	SB3	FG1	LR1	UB1
P10	30		G2	SB4	FG2	LG1	UR2
P11	31		G3	SB5	FG3	LB1	UG2
P12	33		G4	FG0	SGO	UR2	LG1
P13	34		G5	FG1	SG1	UG2	LB1
P14	36		G6	FG2	SG2	UB2	LR2
P15	37		G7	FG3	SG3	LR2	LG2
P16	39		R0	FG4	FR0	LG2	
P17	40		R1	FG5	FR1	LB2	
P18	42		R2	SG0	FR2	UR3	
P19	43		R3	SG1	FR3	UG3	
P20	45		R4	SG2	SR0	UB3	
P21	46		R5	SG3	SR1	LR3	
P22	48		R6	SG4	SR2	LG3	
P23	49		R7	SG5	SR3	LB3	
P24		2		FR0			
P25		3		FR1			
P26		5		FR2			
P27		6		FR3			
P28		8		FR4			
P29		9		FR5			
P30		11		SR0			
P31		12		SR1			
P32		14		SR2			
P33		15		SR3			
P34		17		SR4			
P35		18		SR5			
GND	7,9,12,14,17,20, 23,26,29,32,35,3 8,41,44,47, 50	1,4,7,10,13,16,19 ,20					

AV555-PCI-LVDS LVDS Signal Mapping

Description: The following table describes the mapping between the LVDS Transmission Lines and the organization of interface signal that drive the LVDS IC's before they are combined into serial transmission line data. Two discrete 18 Bit LVDS IC's are used to support all panel interface types. The most common supported panel interfaces are: Dual Pixel / Clock 18 Bit TFT, Single Pixel / Clock 24 Bit TFT, 24 Bit Color DSTN, 18 Bit Color DSTN.

	36 Bit Dual-Pixel/Clock (Industry Standard for XGA and SXGA TFT LVDS Interfaces)	**24 Bit Single Pixel/Clock**	**24 Bit Color DSTN**	**18 Bit Color DSTN**
TXOUT1X Definitions				
TXIN0	First RED 0	-	-	-
TXIN1	First RED 1	Blue 0	UR0	UR0
TXIN2	First RED 2	-	-	-
TXIN3	First RED 3	-	-	-
TXIN4	First RED 4	-	-	-
TXIN5	First RED 5	-	-	-
TXIN6	First Green 0	Green 4	UR2	LG1
TXIN7	First Green 1	Green 5	UG2	LB1
TXIN8	First Green 2	Green 6	UB2	LR2
TXIN9	First Green 3	Green 7	LR2	LG2
TXIN10	First Green 4	Red 0	LG2	-
TXIN11	First Green 5	Red 1	LB2	-
TXIN12	First Blue 0	NC (Blue 0) Don't Use	-	-
TXIN13	First Blue 1	Blue 1	UG0	UG0
TXIN14	First Blue 2	Blue 2	UB0	UB0
TXIN15	First Blue 3	Blue 3	LR0	UR1
TXIN16	First Blue 4	Blue 4	LG0	LR0
TXIN17	First Blue 5	Blue 5	LB0	LG0
TXIN18	HSYNC	HSYNC	LP	LP
TXIN19	VSYNC	VSYNC	FLM	FLM
TXIN20	DE	DE	M	M
TXCLKIN	SHFCLK (Pixel Clock / 2)	SHFCLK (Pixel Clock)	Pixel Clock	Pixel Clock
TXOUT2X Definitions				
TXIN0	Second RED 0	-	Panel Data Clock	Panel Data Clock
TXIN1	Second RED 1	-	-	-
TXIN2	Second RED 2	-	-	-
TXIN3	Second RED 3	-	-	-
TXIN4	Second RED 4	-	-	-
TXIN5	Second RED 5	-	-	-
TXIN6	Second Green 0	Red 2	UR3	-
TXIN7	Second Green 1	Red 3	UG3	-
TXIN8	Second Green 2	Red 4	UB3	-
TXIN9	Second Green 3	Red 5	LR3	-
TXIN10	Second Green 4	Red 6	LG3	-
TXIN11	Second Green 5	Red 7	LB3	-
TXIN12	Second Blue 0	Blue 6	UR1	LB0
TXIN13	Second Blue 1	Blue 7	UG1	LR1
TXIN14	Second Blue 2	Green 0	UB1	UG1
TXIN15	Second Blue 3	Green 1	LR1	UB1
TXIN16	Second Blue 4	Green 2	LG1	UR2
TXIN17	Second Blue 5	Green 3	LB1	UG2
TXIN18	Pull Down / J9-1 GPIO / ENABKL	Same	Same	Same
TXIN19	Pull Down / J9-2 GPIO / GPIO1	Same	Same	Same
TXIN20	Pull Down / J9-3 GPIO	Same	Same	Same
TXCLKIN	SHFCLK (Pixel Clock / 2)	SHFCLK (Pixel Clock)	Pixel Clock	Pixel Clock