UNIVERSAL SYNC GENERATOR

GENERAL DESCRIPTION

The SAA1043 generates the synchronizing waveforms required in all types of video source equipment (video cameras, film-scanners, video games, computer displays and similar applications). The device is programmable to suit standards SECAM1, SECAM2, PAL/CCIR, NTSC1, NTSC2 and PAL-M; the video game 624 and 524-line standards; and can be synchronized to an external sync signal. Inputs and outputs are CMOS compatible.

Features

- Programmable to eight standards
- Horizontal frequency manipulation for application in non-standard systems
- Oscillator functions with LC or crystal elements
- Additional outputs to simplify camera signal processing
- Can be synchronized to an external sync signal
- Vertical reset for fast vertical lock
- Subcarrier lock in combination with subcarrier coupler SAA1044
- Very low power consumption

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range (pin 28)	V_{DD}	5.7	–	7.5	V
Supply current range (quiescent)	I_{DD}	–	–	10	μA
Oscillator frequency	f_{OSC}	–	–	5.1	MHz
Operating ambient temperature range	T_{amb}	−25	–	+ 70	°C

PACKAGE OUTLINES

SAA1043 : 28-lead DIL; plastic (SOT117).
SAA1043T: 28-lead mini-pack; plastic (SO28; SOT136A).

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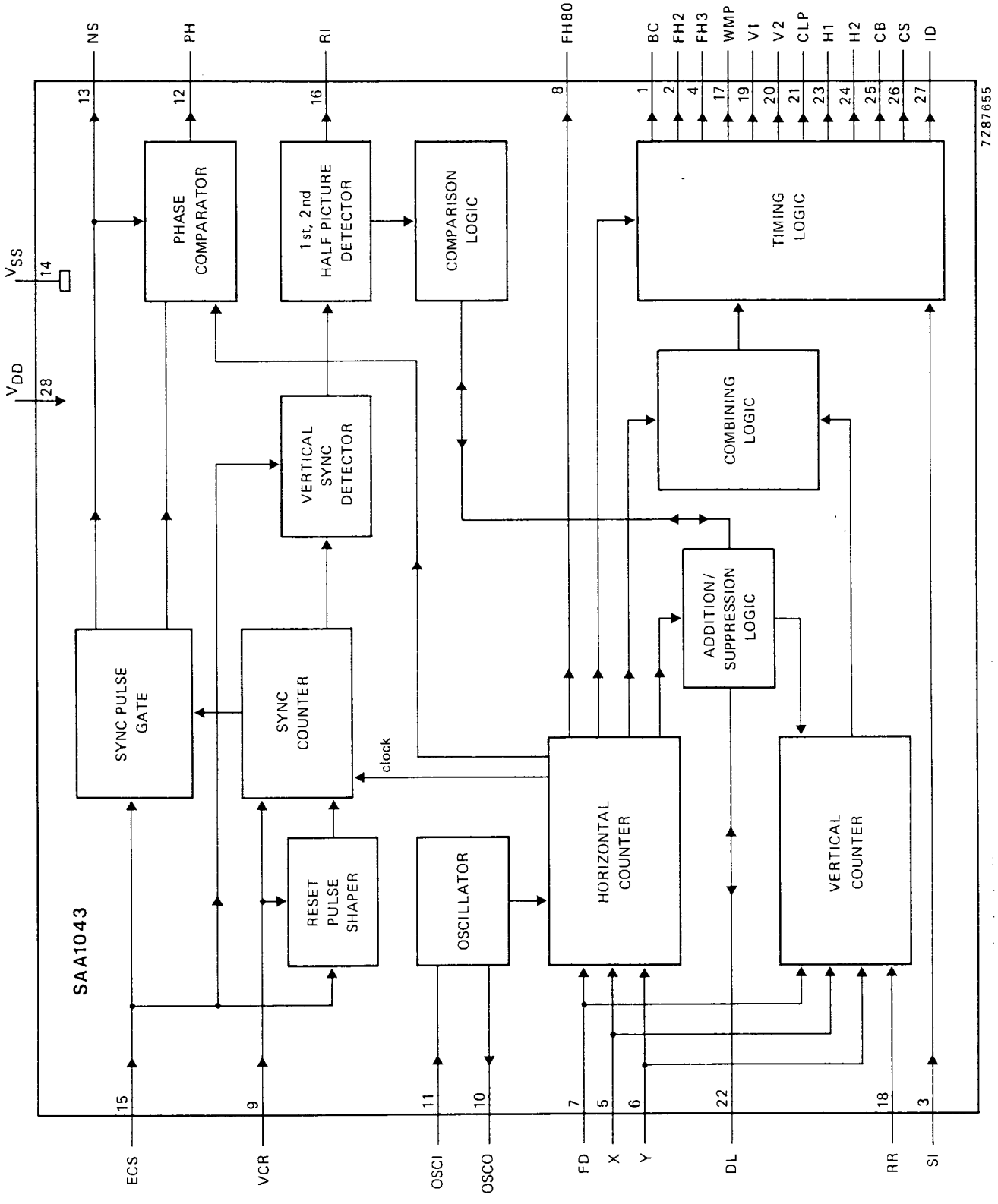


Fig. 1 Block diagram.

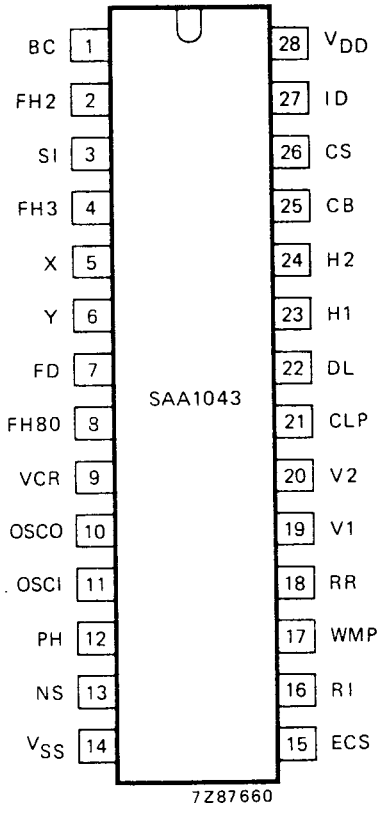


Fig. 2 Pinning diagram.

PINNING

1	BC	burst flag/chrominance blanking (SECAM) output
2	FH2	PAL identification output
3	SI	set identification input (SECAM, PAL, PAL-M)
4	FH3	400 Hz (PAL); 360 HZ (NTSC, PAL-M) and $f_H/3$ (SECAM)
5	X	standard programming input
6	Y	standard programming input
7	FD	standard programming input
8	FH80	80 x f_H output (1.25 MHz)
9	VCR	VCR standard input
10	OSCO	oscillator output
11	OSCI	oscillator input
12	PH	phase detector output
13	NS	no-sync detector output
14	V_{SS}	negative supply voltage (ground)
15	ECS	external composite sync input
16	RI	vertical identification output
17	WMP	white measurement pulse output
18	RR	vertical reset input
19	V1	vertical drive output
20	V2	vertical drive output
21	CLP	clamp pulse output
22	DL	2 x f_H input/output
23	H1	horizontal drive output
24	H2	horizontal drive output
25	CB	composite blanking output
26	CS	composite sync output
27	ID	SECAM identification output
28	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

Sync pulse generation

Programming of operating standard

The standard required for operation is programmed using the inputs X, Y and FD as shown in Table 1. The FD input selects 525 or 625-line working of the vertical counter (524 or 624-lines for video game standards) and also influences the choice of oscillator frequency as shown in Table 2.

Table 1 Programming of operating standard

standard	FD	X	Y
SECAM 1	0	0	0
SECAM 2	0	0	1
624	0	1	0
PAL/CCIR	0	1	1
NTSC 1	1	0	0
NTSC 2	1	0	1
524	1	1	0
PAL-M	1	1	1

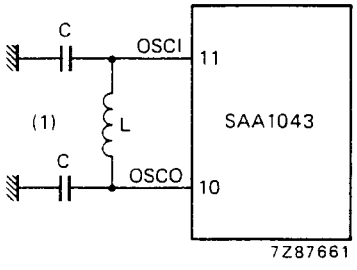
positive logic: 1 = HIGH; 0 = LOW

Oscillator

The built-in oscillator of the SAA1043 functions with an external LC-circuit (Fig. 3) or with a crystal of the parallel resonance type (Fig. 4). For operation in the VCR mode the LC oscillator circuit is recommended. The frequencies required for the operating standards are shown in Table 2.

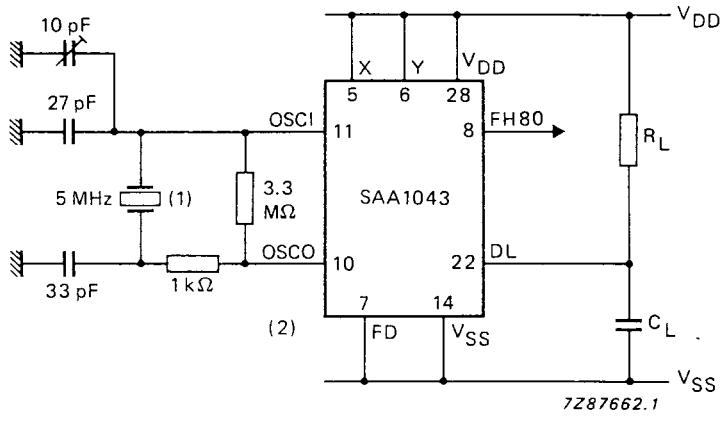
Table 2 Oscillator input frequencies

operating standard	osc. frequency (f_{OSCI}) MHz	vertical divider (FD)	vertical frequency (f_V) Hz	horizontal frequency (f_H) Hz
PAL, SECAM, 624	5.0	0	50	15625
NTSC, PAL-M, 524	5.034964	1	59.94	15734.26
PAL, SECAM, 624	2.5	H2 (pin 24)	50	15625
NTSC, PAL-M, 524	2.51782	H1 (pin 23)	59.94	15734.26



(1) Component values can be calculated from the formula $f_{OSCI} = 1/2\pi\sqrt{LC_V}$ where $C_V = C/2 + C_p$ and C_p = parasitic capacitance of typically 5 pF.

Fig. 3 LC oscillator circuit.



(1) Catalogue number of crystal: 8222 298 40760.

(2) All inputs not shown are at V_{SS}.

Fig. 4 Crystal oscillator circuit showing test set-up for oscillator frequency measurement.

Synchronization to an external sync signal

Use is made of the phase comparator output PH to lock the internally generated sync pulses to an external sync signal. Reset pulses derived at each falling edge of the external sync signal (ECS) reset the the sync counter which is clocked at the internal horizontal frequency by the horizontal counter. At each horizontal scan period the sync counter opens the sync pulse gate and allows the ECS to be applied to the phase comparator where it is compared with the phase of the internally generated horizontal sync pulse. When the two signals are in phase the output PH is in a high impedance state. When a phase difference exists PH is pulled towards V_{DD} or V_{SS} depending on the direction of the error (Fig. 5). The phase-analogue voltage on PH is used to correct the frequency at OSCI via a voltage-controlled oscillator and null the phase error between internal and external signals. Pulses occurring on the ECS outside of the sync pulse gating time (serration and equalization pulses) do not effect the phase comparator.

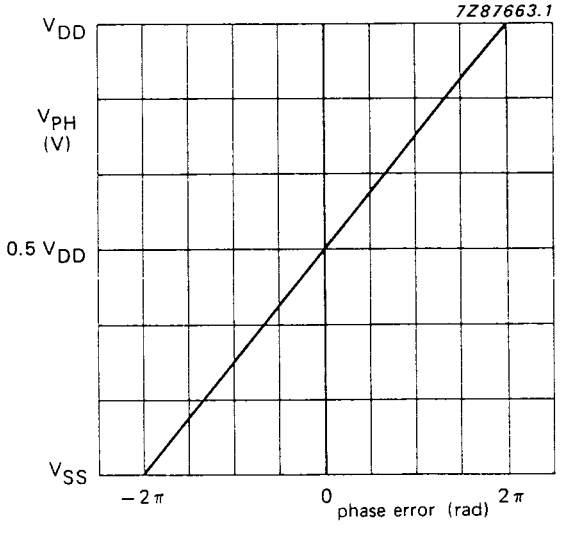


Fig. 5 Phase comparator characteristic.

FUNCTIONAL DESCRIPTION (continued)

Synchronization to an external sync signal (continued)

The circuit will lock to standard and non-standard sync signals. With standard signals the resetting of the sync counter is permitted after 3/4 of the horizontal scan period and if one reset pulse is missed the next pulse will reset the counter. With non-standard signals a narrow reset window is imposed to avoid disturbances which would otherwise be visible on the screen during vertical blanking time. The width of this window is $64 - 15.2 <$ reset time $< 64 + 15.2$ μs. If a reset pulse does not occur within this window the same window timing is specified for the next horizontal scan.

A no-sync signal is generated by the sync pulse gate if the sync counter is not reset from the ECS. The no-sync signal (NS) occurs 6.4 μs after the time of the missing reset pulse.

Detection of the vertical sync in the ECS is performed using a double sampling method which minimizes detection failures. Vertical lock is performed by comparing the internal vertical sync with a pulse derived from the ECS and using the result to modify the period of the vertical counter. This is achieved by manipulating the DL ($2 \times f_H$) input to the vertical counter via the addition/subtraction logic. The DL pulses are added or suppressed to bring the circuit into lock in the shortest possible time; the direction taken is determined by a logic decision based on the half picture in which the ECS derived pulse occurred.

Vertical reset input (RR)

The RR is used when external synchronization runs on separate vertical (V) and horizontal (H) pulses instead of composite sync (CS) pulses.

- RR = LOW : no external sync or external CS to ECS input
- RR = V-pulses: external sync with H and V requires H-pulses to ECS input
  duration of H-pulse < 5 μs
  duration of V-pulse 1 μs $< t_V < 3$ μs

VCR standard input (VCR)

The VCR input sets the synchronization standard for VCRs.

- VCR = HIGH: normal mode

Then the ECS input expects a 64 μs ± 16 μs H-part of the CS pulse.
If the pulse fits inside the window, the SAA1043 will continue to take synchronizing pulses only inside the window.
If the pulse does not occur inside the window, the synchronizing circuit will take off the window and accept pulses at any time.

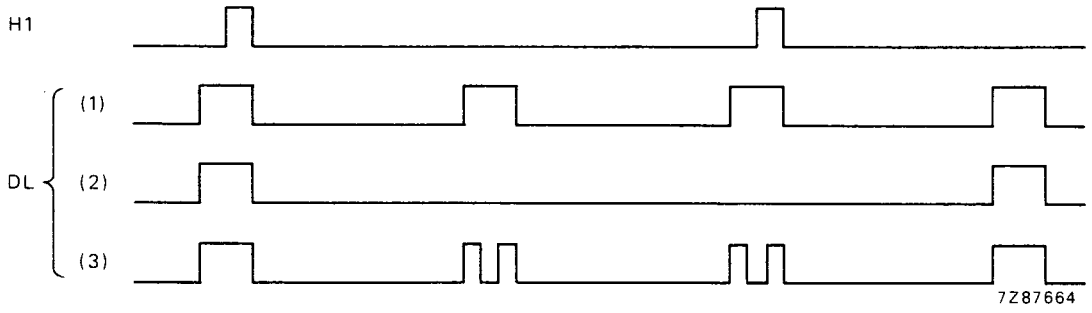
- VCR = LOW: VCR mode

The window ± 16 μs is always applied.

If the colour burst is not present in the correct position, or FH2 is not in phase with the incoming signal, the set identification input (SI) must be set to logic HIGH on line 2 for the duration of 1 line.

Use in non-standard systems

For systems requiring a non-standard horizontal frequency the number of horizontal scans per picture can be manipulated using the open drain input/output DL. The addition or suppression of pulses during the high ohmic period of DL modifies the vertical counter value. The suppression of two DL pulses per half picture will give one extra horizontal scan and the addition of two DL pulses will remove one horizontal scan from the half picture (see Fig. 6).



(1) Normal waveform at DL; $f_{DL} = 2 \times f_H$.

(2) Waveform at DL with two pulses suppressed increases the number of horizontal scans per half picture by 1.

(3) Waveform at DL with two additional pulses decreases the number of horizontal scans per half picture by 1.

Fig. 6 Manipulation of the horizontal frequency for non-standard systems.

Output waveforms

The output waveforms for the different modes of operation are shown in Figs 7 and 8.

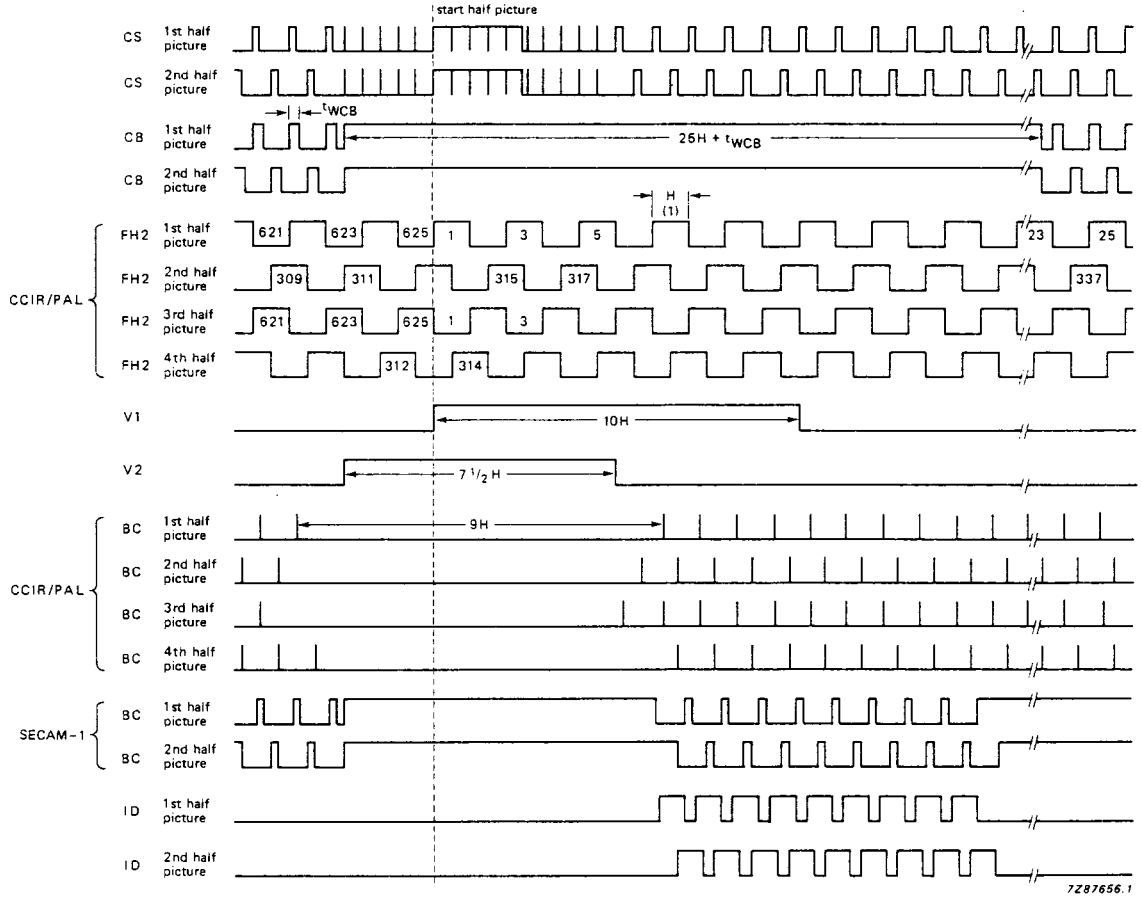
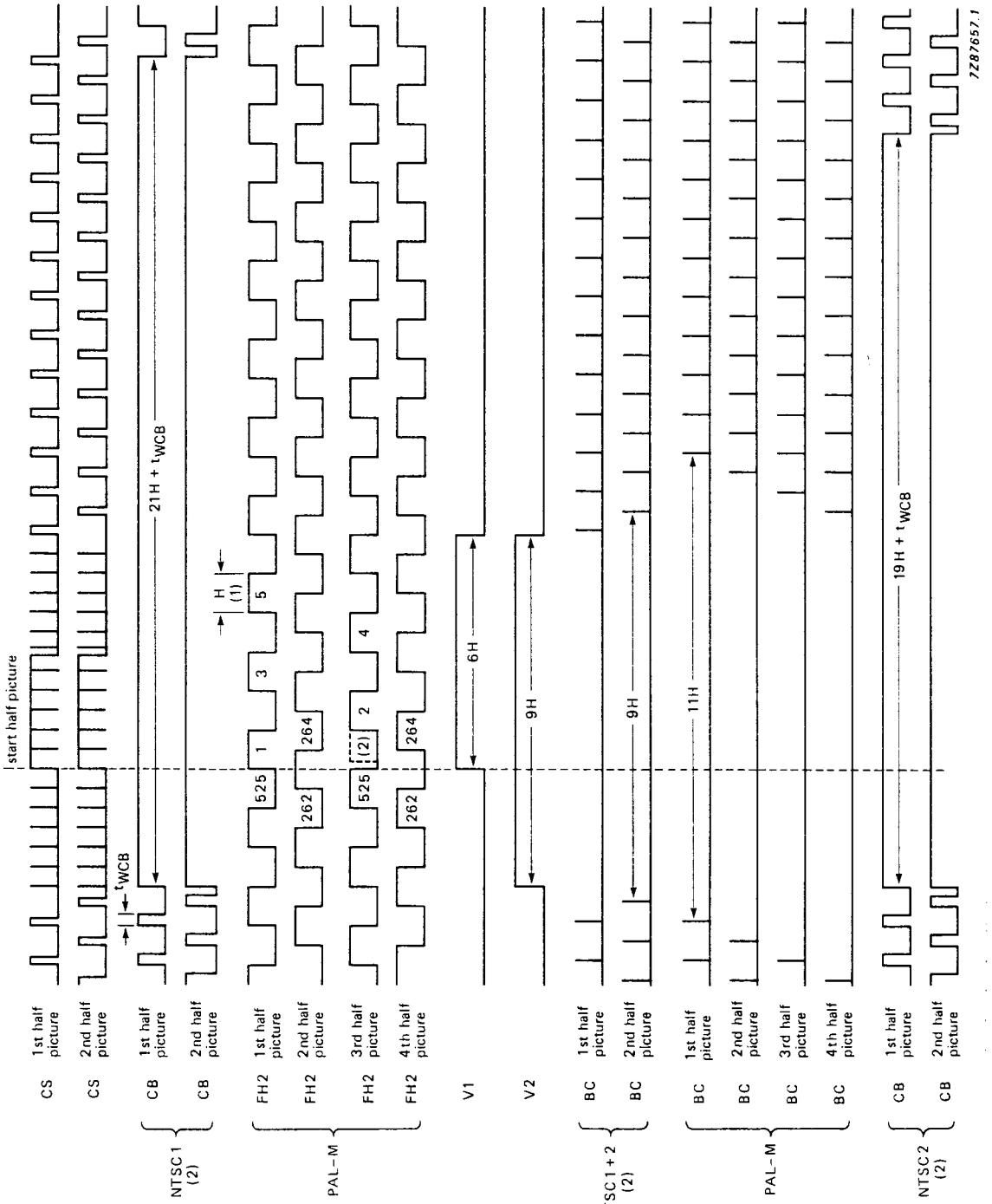


Fig. 7 Typical output waveforms for PAL/CCIR and SECAM. In the 624-line mode the output waveforms are identical to the 1st half picture of PAL/CCIR and are not interlaced (0.5 H subtracted from the waveform timing).



(1) H = 1 horizontal scan.

(2) NTSC mode reset; the 4th half picture is identical to the 2nd half picture for NTSC.

Fig. 8 Typical output waveforms for NTSC and PAL-M. In the 524-line mode the output waveforms are identical to the 1st half picture of NTSC and are not interlaced (0.5 H subtracted from the waveform timing).

WAVEFORM TIMING (Table 3, Figs 9 and 10)

The waveform timing depends on the frequency of the oscillator input (f_{OSCI}). This is shown in Table 3 as the number (n) of oscillations at OSCI. The timings given are derived from $n \times t_{OSCI} \pm 100$ ns. One horizontal scan (H) = $320 \times t_{OSCI} = 1/f_H$. Note that the number of horizontal scans per half picture can be modified for non-standard systems using input/output DL as shown in Fig. 6.

Table 3 Waveform timing

parameter	symbol	PAL	NTSC	PAL-M	SECAM	unit	n
CS							
Horizontal sync pulse width	t_{WSC1}	4.8	4.77	4.77	4.8	µs	24
Equalizing pulse width	t_{WSC2}	2.4	2.38	2.38	2.4	µs	8
Serration pulse width	t_{WSC3}	4.8	4.77	4.77	4.8	µs	24
Duration of pre-equalizing pulses		2.5	3	3	2.5	H	
Duration of post-equalizing pulses		2.5	3	3	2.5	H	
Duration of serration pulses		2.5	3	3.5	2.5	H	
CB							
Horizontal blanking pulse width							
PAL/SECAM/PAL-M	t_{WCB}	12	–	11.12	12	µs	60
NTSC 1	t_{WCB}	–	11.12	–	–	µs	56
NTSC 2	t_{WCB}	–	10.53*	–	–	µs	53
Front porch	t_{PCBCS}	1.6	1.59	1.59	1.6	µs	8
Duration of vertical blanking							
PAL/SECAM/PAL-M		$25H+t_{WCB}$	–	$21H+t_{WCB}$	$25H+t_{WCB}$		
NTSC 1		–	$21H+t_{WCB}$	–	–		
NTSC 2		–	$19H+t_{WCB}$	–	–		
BC (PAL)							
Burst key pulse width	t_{WBC}	2.4	2.38	2.38	–	µs	12
Sync to burst delay	t_{PCSBC}	5.6	5.56	5.76	–	µs	28
Burst suppression		9	9	11	–	H	
Position of burst suppression: 1st half picture		H623 to H6	H523 to H6	H523 to H8	–		
2nd half picture		H310 to H318	H261 to H269	H260 to H270	–		
3rd half picture		H622 to H5	H523 to H6	H522 to H7	–		
4th half picture		H311 to H319	H261 to H269	H259 to H269	–		

parameter	symbol	PAL	NTSC	PAL-M	SECAM	unit	n
BC (SECAM)							
Chrominance pulse width	t_{WBC}	–	–	–	7.2	µs	36
Chrominance to sync delay	t_{PBCCS}	–	–	–	1.6	µs	8
Duration of vertical blanking: SECAM 1	1st half picture : 25H + t_{WBC} except H320 to H328 2nd half picture: 24.5H + t_{WBC} except H7 to H15						
SECAM 2	1st half picture : 25H + t_{WBC} 2nd half picture: 24.5H + t_{WBC}						
CLP							
Clamp pulse width	t_{WCLP}	2.4	2.38	2.38	2.4	µs	12
Sync to clamp delay	t_{PCSCLP}	2.4	2.38	2.38	2.4	µs	12
DL							
Frequency	f_{DL}	2 x f_H	2 x f_H	2 x f_H	2 x f_H		
Pulse width	t_{WDL}	9.6	9.53	9.53	9.6	µs	48
DL to sync delay	t_{PCLCS}	5.6	5.56	5.56	5.6	µs	28
FH80							
Frequency	f_{FH80}	80 x f_H	80 x f_H	80 x f_H	80 x f_H		
Sync to FH80 delay		0.2	0.2	0.2	0.2	µs	1
H1, H2							
H1 pulse width	t_{WH1}	7.2	7.15	7.15	7.2	µs	36
H2 pulse width	t_{WH2}	7.2	7.15	7.15	7.2	µs	36
H1 to sync delay	t_{PH1CS}	0.8	0.79	0.79	0.8	µs	4
Sync to H2 delay	t_{PCSH2}	0.8	0.79	0.79	0.8	µs	4
Repetition period		64	63.56	63.56	64	µs	
V1, V2							
V1 duration		10	6	6	10	H	
V2 duration		7.5	9	9	7.5	H	
V1 to sync delay	t_{PV1CS}	1.6	1.59	1.59	1.6	µs	8
Sync to V2 delay	t_{PV2CS}	1.6	1.59	1.59	1.6	µs	8
FH2							
Frequency	f_{FH2}	$f_H/2$	$f_H/2$	$f_H/2$	$f_H/2$		
Sync to FH2 delay		0	0	0	0	µs	
FH3							
Frequency	f_{FH3}	400	360	360	$f_H/3$		
Sync to FH3 delay		–	–	–	0	µs	

WAVEFORM TIMING (continued)

Table 3 (continued)

parameter	symbol	PAL	NTSC	PAL-M	SECAM	unit	n
WMP							
WMP pulse width		2.4	2.38	2.38	2.4	μs	12
Sync to WMP delay		34.4	34.16	34.16	34.4	μs	172
Duration of WMP		10	9	9	10	H	
Position of WMP							
1st half picture:		H163 to H173	H134 to H143	H134 to H143	H163 to H173		
2nd half picture:		H475 to H485	H396 to H405	H396 to H405	H475 to H485		
RI							
Frequency		$f_V/2$	$f_V/2$	$f_V/2$	$10f_H$		
Position of edges		H6 and H318	H7 and H269	H7 and H269	–		
ID							
ID pulse width	t_{WID}	12.0	11.12	11.12	12.0	μs	60
ID to sync delay	t_{PIDCS}	1.6	1.59	1.59	1.6	μs	8
Position of ID							
1st half picture:		H7 to H15	H8 to H22	H8 to H22	H7 to H15		
2nd half picture:		H320 to H328	H271 to H285	H271 to H285	H320 to H328		

* Horizontal blanking pulse width for NTSC 2 can be 11.12 μs maximum.

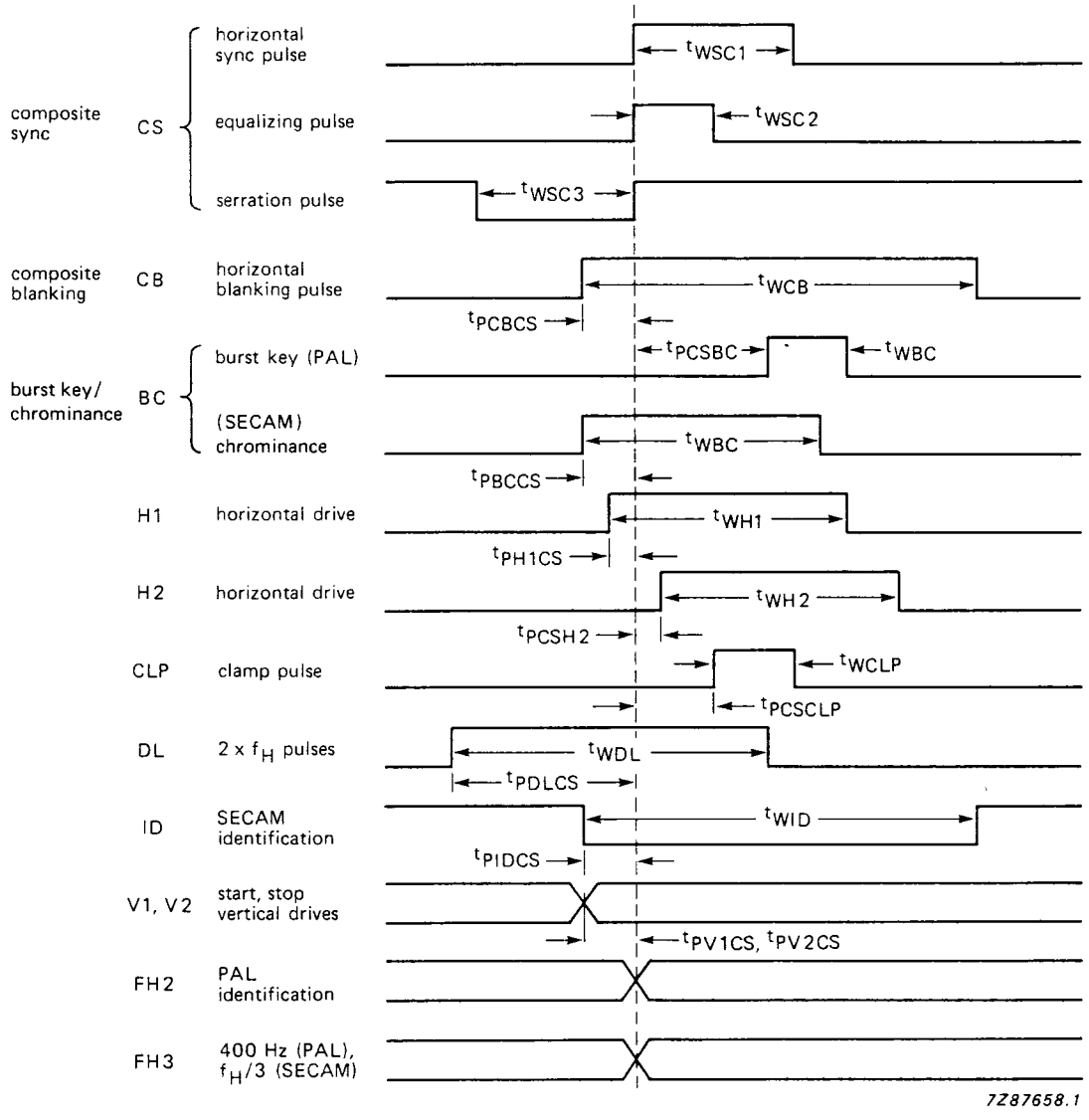


Fig. 9 Waveform timings; PAL/CCIR; SECAM; 624-line modes.

WAVEFORM TIMING (continued)

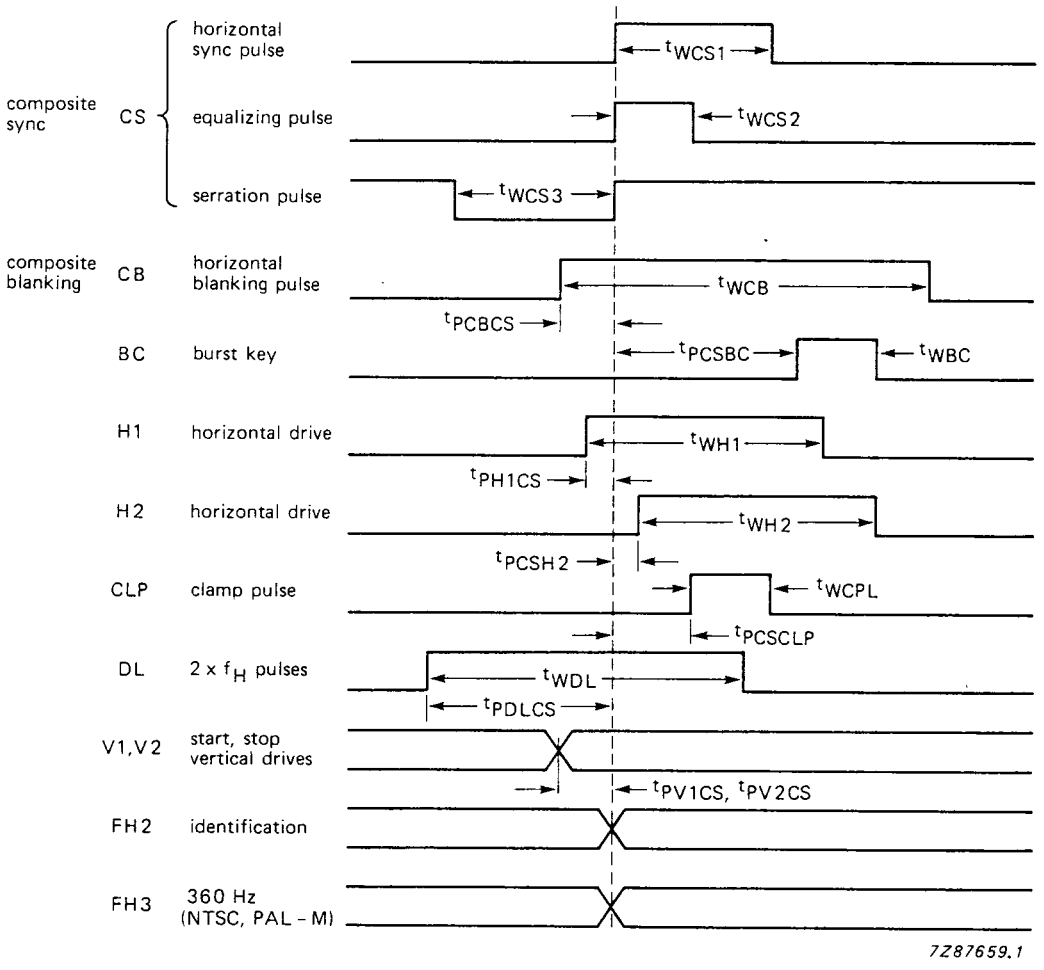


Fig. 10 Waveform timings: NTSC; PAL-M; 524-line modes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range with respect to V_{SS}	V_{DD}	−0.5	+ 15	V
Input voltage range	V_I	−0.5	V_{DD} + 0.5*	V
Input current	$\pm I_I$	—	10	mA
Output voltage range	V_O	−0.5	V_{DD} + 0.5*	V
Output current	$\pm I_O$	—	10	mA
Total power dissipation per package	P_{tot}	—	200	mW
Power dissipation per output	P_O	—	100	mW
Operating ambient temperature range	T_{amb}	−25	+ 70	°C
Storage temperature range	T_{stg}	−55	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

* V_{DD} + 0.5 V not to exceed 15 V.

CHARACTERISTICS

V_{DD} = 5.7 to 7.5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage	V_{DD}	5.7	–	7.5	V
Supply current (quiescent) at I_O = 0 mA at all outputs; V_{DD} = 7.5 V; T_{amb} = 25 °C	I_{DD}	–	–	10	μA
Inputs					
Input voltage HIGH	V_{IH}	$0.7V_{DD}$	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	$0.3V_{DD}$	V
Input leakage current at V_I = 7.5 V; V_{DD} = 7.5 V; T_{amb} = 25 °C	I_{LI}	–	–	1	μA
Input leakage current at V_I = 0 V; V_{DD} = 7.5 V; T_{amb} = 25 °C	$-I_{LI}$	–	–	1	μA
Outputs (except PH and OSC0)					
Output voltage HIGH at $-I_{OH}$ = 0.5 mA	V_{OH}	$V_{DD} - 0.5$	–	–	V
Output voltage LOW at I_{OL} = 0.5 mA	V_{OL}	–	–	0.4	V
Output PH					
Output voltage HIGH at $-I_{OH}$ = 0.9 mA	V_{OH}	$V_{DD} - 0.5$	–	–	V
Output voltage LOW at I_{OL} = 1.0 mA	V_{OL}	–	–	0.4	V
Output leakage current at V_O = 7.5 V; V_{DD} = 7.5 V	I_{LO}	–	–	5	μA
Output leakage current at V_O = 7.5 V; V_{DD} = 7.5 V; T_{amb} = 25 °C	I_{LO}	–	–	1	μA
Output leakage current at V_O = 0 V; V_{DD} = 7.5 V	$-I_{LO}$	–	–	5	μA
Output leakage current at V_O = 0 V; V_{DD} = 7.5 V; T_{amb} = 25 °C	$-I_{LO}$	–	–	1	μA
Output OSCO					
Output voltage HIGH at V_{OSCI} = 0 V; $-I_{OH}$ = 0.9 mA	V_{OH}	$V_{DD} - 0.5$	–	–	V
Output voltage LOW at V_{OSCI} = V_{DD}; I_{OL} = 1.0 mA	V_{OL}	–	–	0.4	V

parameter	symbol	min.	typ.	max.	unit
Input/output DL (open drain)*					
Output voltage LOW at I_{OL} = 1.0 mA	V_{OL}	–	–	0.4	V
Output leakage current at V_O = 7.5 V; V_{DD} = 7.5 V	I_{LO}	–	–	5	μA
Output leakage current at V_O = 7.5 V; V_{DD} = 7.5 V; T_{amb} = 25 °C	I_{LO}	–	–	1	μA
Load resistance (Fig. 4)					
at V_{DD} = 5.7 V	R_L	1.4	–	–	kΩ
at V_{DD} = 7.5 V	R_L	0.82	–	–	kΩ
Time constant (Fig. 4)					
at V_{DD} = 5.7 V	R_LC_L	–	–	19	ns
at V_{DD} = 7.5 V	R_LC_L	–	–	13	ns
Oscillator frequency (Fig. 4)					
Maximum oscillator frequency at V_{DD} = 5.7 V	f_{OSC}	5.1	–	–	MHz

* An external pull-up resistor (3.9 kΩ) must be connected between DL and V_{DD}. The time constant R_LC_L must not exceed the values given.

APPLICATION INFORMATION

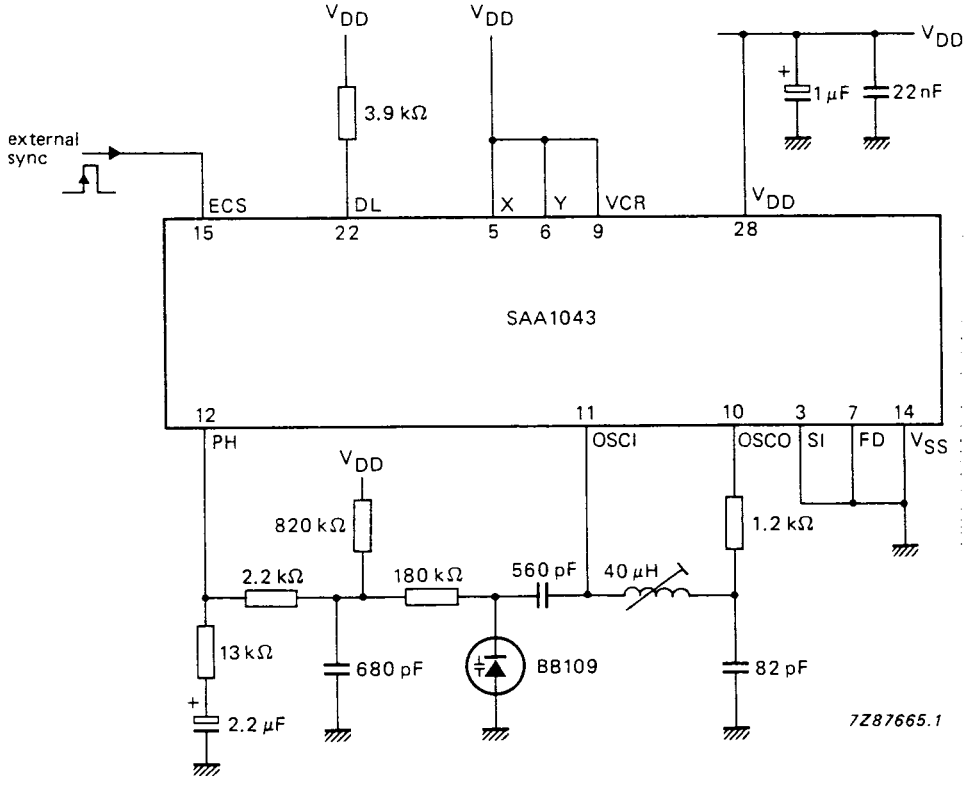


Fig. 11 Synchronizing circuit using passive filter network.