SONY

CXA3017R

Decoder/Driver/Timing Generator for Color LCD Panels

For the availability of this product, please contact the sales office.

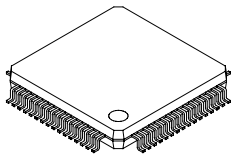
Description

The CXA3017R is an IC designed to drive the color LCD panels LCX005BK/BKB, LCX009AK/AKB, LCX024AK/AKB, LCX027AK/AKB and DCX501BK.

This IC allows two-panel simultaneous and switching drive by simultaneously outputting the timing pulses for the LCX005BK/BKB, LCX009AK/AKB, LCX024AK/AKB, LCX027AK/AKB and DCX501BK.

This IC greatly reduces the number of peripheral circuits and parts by incorporating an RGB decoder, driver, and timing generator for video signals onto a single chip. This chip has a built-in serial interface circuit and electronic attenuators which allow various settings to be performed by microcomputer control, etc.

64 pin LQFP (Plastic)



Features

- Color LCD panel LCX005BK/BKB, LCX009AK/AKB, LCX024AK/AKB, LCX027AK/AKB and DCX501BK driver
- Supports two-panel simultaneous and switching drive using the LCX005BK/BKB, LCX009AK/AKB, LCX024AK/AKB, LCX027AK/AKB and the DCX501BK
- Supports NTSC and PAL systems
- Supports 16:9 wide display (letter box and pulse elimination display)
- Supports composite inputs, Y/C inputs and Y/color difference inputs
- Serial interface circuit
- Electronic attenuators (D/A converter)
- VCO
- BPF, trap and delay line
- Sharpness function
- 2-point γ correction circuit
- R, G, B signal delay time adjustment circuit
- Polarity inversion circuit (line inverted mode)
- Supports external RGB input
- D/A output pin (0 to 3V, 8 levels)
- Supports AC drive for LCD panel during no signal

Applications

- Compact LCD monitors
- LCD viewfinders
- Compact liquid crystal projectors, etc.

Structure

Bi-CMOS IC

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	$V_{CC}1$ – GND1	6	V
	$V_{CC}2$ – GND2	14	V
	$V_{CC}3$ – GND3	14	V
	$V_{DD}1, 2$ – V_{SS}	4.5	V
• Analog input pin voltage	VINA	–0.3 to $V_{CC}1$	V
• Digital input pin voltage	VIND	–0.3 to $V_{DD}1$ + 0.3V	
• Operating temperature	Topr	–15 to +75	°C
• Storage temperature	Tstg	–40 to +125	°C

• Allowable power dissipation*1

P_D (Ta ≤ 75°C)

Approximately 350mW

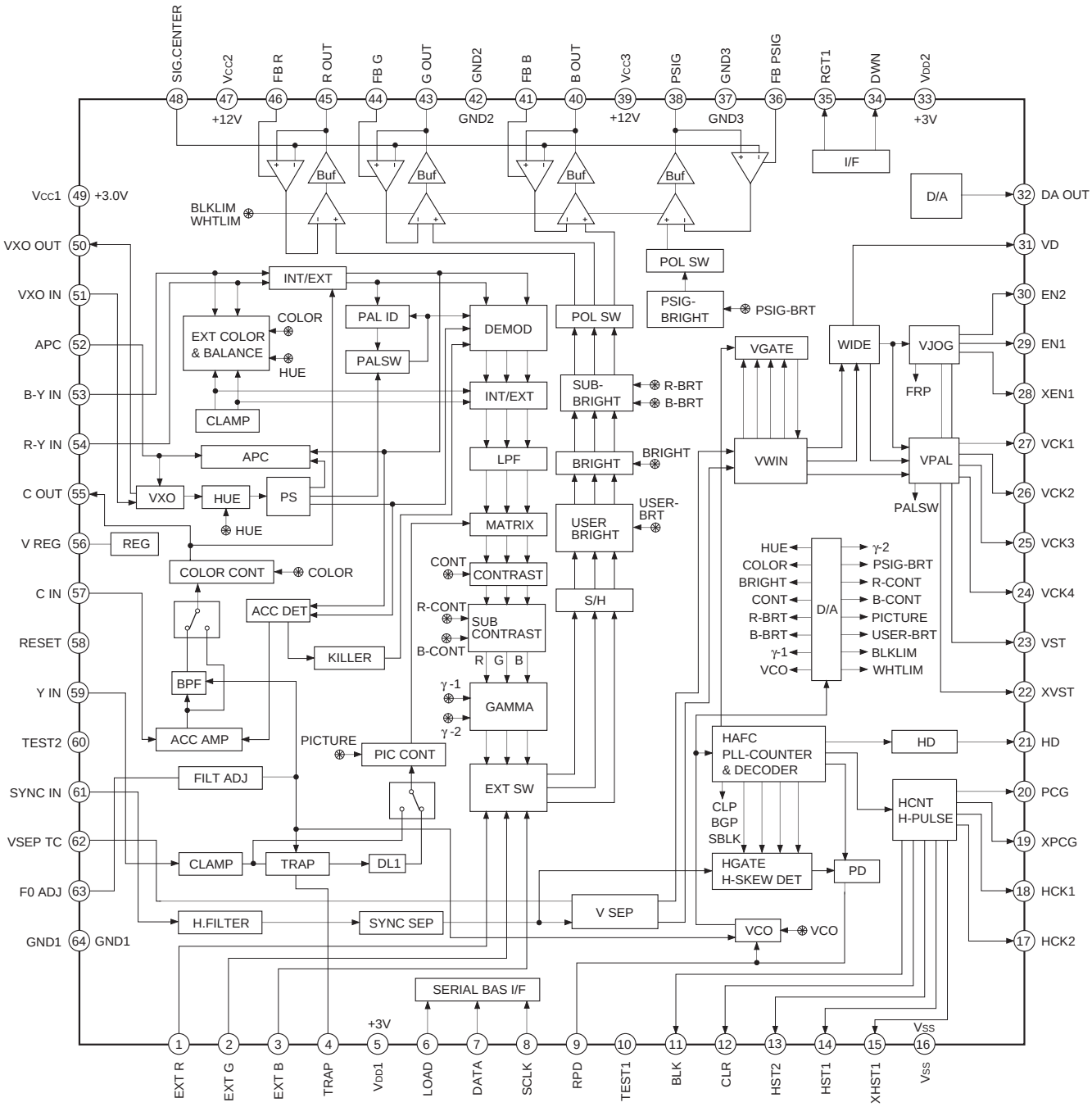
Operating Conditions

Supply voltage	$V_{CC}1$ – GND1	2.7 to 3.6	V
	$V_{CC}2$ – GND2	11.0 to 13.5	V
	$V_{CC}3$ – GND3	11.0 to 13.5	V
	$V_{DD}1, 2$ – V_{SS}	2.7 to 3.6	V

*1 With substrate Size: 30 × 30 × 1.6mm
Material: Glass fabric base epoxy

E98Y29-PS

Block Diagram



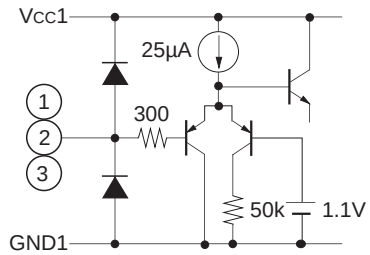
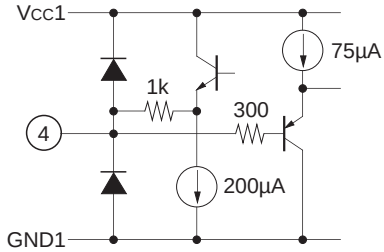
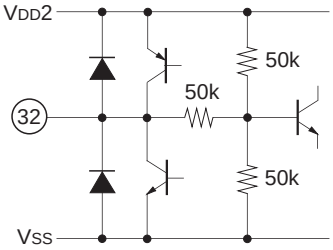
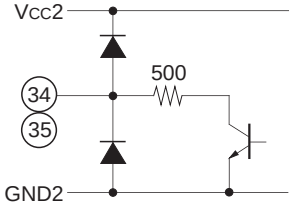
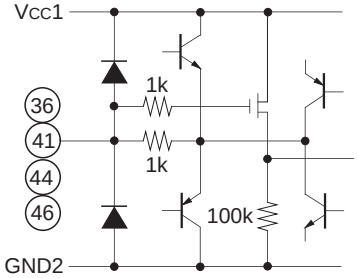
Pin Description

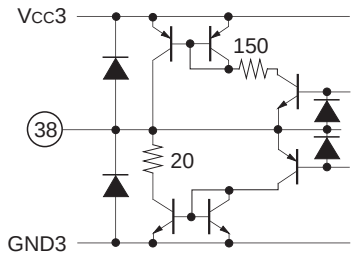
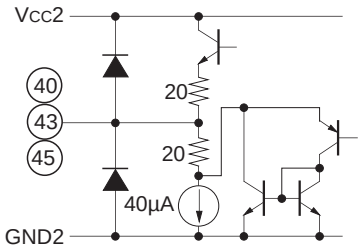
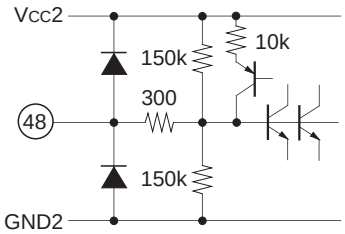
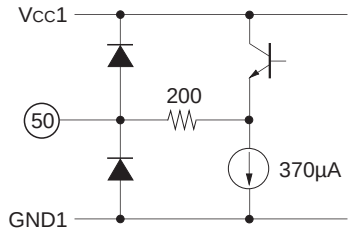
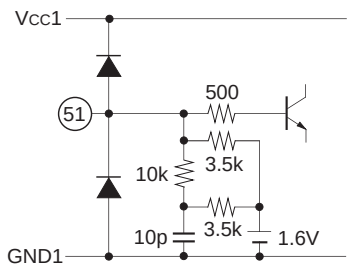
Pin No.	Symbol	I/O	Description	Input pin processing for open status
1	EXT R	I	External digital R input	
2	EXT G	I	External digital G input	
3	EXT B	I	External digital B input	
4	TRAP	O	External trap connection	
5	$V_{DD}1$		Digital 3V power supply for oscillation cell	
6	LOAD	I	Serial interface load input	
7	DATA	I	Serial interface data input	
8	SCLK	I	Serial interface clock input	
9	RPD	O	Phase comparator output	
10	TEST1	I	Test (Connect to GND.)	L
11	BLK	O	BLK pulse output	
12	CLR	O	CLR pulse output	
13	HST2	O	H start pulse 2 output	
14	HST1	O	H start pulse 1 output	
15	XHST1	O	XH start pulse 1 output (reverse polarity of HST1)	
16	V_{SS}		Digital 3V GND	
17	HCK2	O	H clock pulse 2 output	
18	HCK1	O	H clock pulse 1 output	
19	XPCG	O	XPCG pulse output (reverse polarity of PCG)	
20	PCG	O	PCG (precharge) pulse output	
21	HD	O	HD pulse output	
22	XVST	O	XV start pulse output (reverse polarity of VST)	
23	VST	O	V start pulse output	
24	VCK4	O	V clock pulse 4 output	
25	VCK3	O	V clock pulse 3 output	
26	VCK2	O	V clock pulse 2 output	
27	VCK1	O	V clock pulse 1 output	
28	XEN1	O	XEN pulse 1 output (reverse polarity of EN1)	
29	EN1	O	EN pulse 1 output	
30	EN2	O	EN pulse 2 output	
31	VD	O	VD pulse output	
32	DA OUT	O	DAC output	
33	$V_{DD}2$		Digital 3V power supply	
34	DWN	O	DCX501BK up/down inverted display switching (open collector output)	

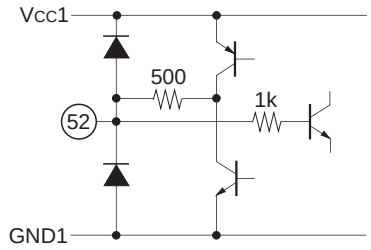
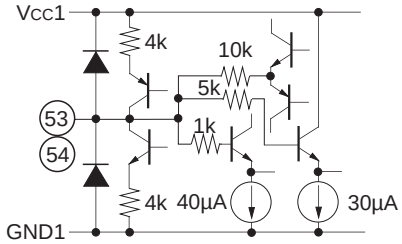
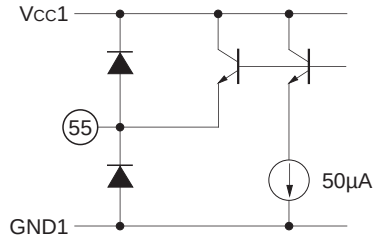
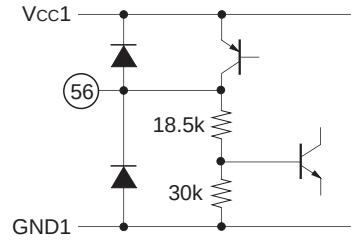
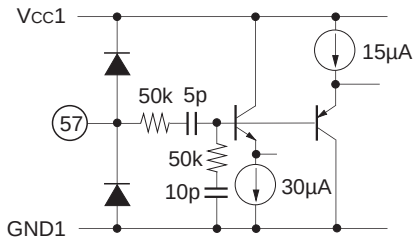
Pin No.	Symbol	I/O	Description	Input pin processing for open status
35	RGT1	O	DCX501BK right/left inverted display switching (open collector output)	
36	FB PSIG	I	PSIG signal DC voltage feedback circuit capacitor connection	
37	GND3		Analog 12V GND for PSIG	
38	PSIG	O	PSIG output	
39	$V_{CC}3$		Analog 12V power supply for PSIG	
40	B OUT	O	B signal output	
41	FB B	I	B signal DC voltage feedback circuit capacitor connection	
42	GND2		Analog 12V GND	
43	G OUT	O	G signal output	
44	FB G	I	G signal DC voltage feedback circuit capacitor connection	
45	R OUT	O	R signal output	
46	FB R	I	R signal DC voltage feedback circuit capacitor connection	
47	$V_{CC}2$		Analog 12V power supply	
48	SIG.CENTER	I	R, G, B and PSIG output DC voltage adjustment	
49	$V_{CC}1$		Analog 3V power supply	
50	VXO OUT	O	VXO output	
51	VXO IN	I	VXO input	
52	APC	O	APC detective filter connection	
53	B-Y IN	I	B-Y color difference signal input	
54	R-Y IN	I	R-Y color difference signal input	
55	C OUT	O	Chroma signal output	
56	V REG	O	Constant voltage capacitor connection	
57	C IN	I	Chroma signal input	
58	RESET	I	System reset	
59	Y IN	I	Y signal input	
60	TEST2	I	Test (Connect to GND.)	L
61	SYNC IN	I	Video input for sync separation	
62	VSEP TC		Capacitor connection for vertical sync separation (or external VSYNC input)	
63	F0 ADJ	O	Internal filter adjusting resistor connection	
64	GND1		Analog 3V GND	

* DWN: DOWN SCAN and UP SCAN RGT: RIGHT SCAN and LEFT SCAN

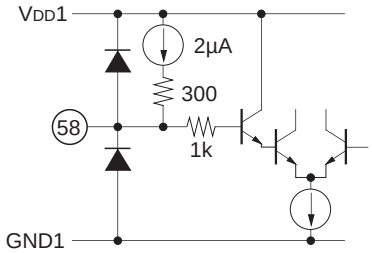
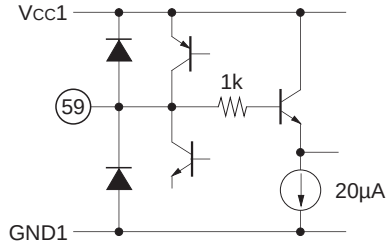
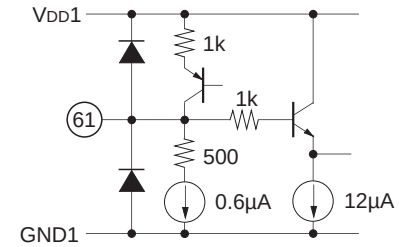
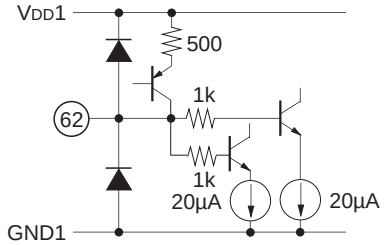
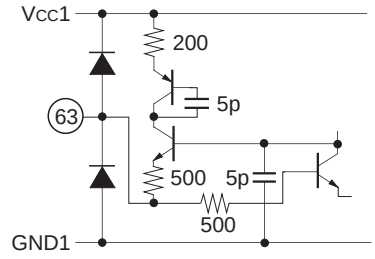
Analog Block Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	EXT-R	—		External digital signal inputs. There are two thresholds: Vth1 (= 1.0V) and Vth2 (= 2.0V). When one of the RGB signals exceeds Vth1, all of the RGB outputs go to black level; when an input exceeds Vth2, only the corresponding output goes to white level. Connect these pins to GND when not used.
2	EXT-G			
3	EXT-B			
4	TRAP	1.0V		External trap connection. Connect the trap between this pin and GND to eliminate the chroma component. Leave this pin open when using Y/C and Y/color difference mode.
32	DA OUT	0.2 to 2.9V		DAC output. 8-level, 7-step DC voltage from approximately 0.2 to 2.9V is output from this pin.
34	DWN	—		DCX501BK up/down and right/left inversion switching. These pins are open collector outputs, so first connect a 100kΩ resistor between these pins and the panel VDD (15.5V) and then connect to the DCX501BK.
35	RGT1	—		
36	FB PSIG	1.5V		Smoothing capacitor connection for the feedback circuit of R, G, B and PSIG output DC level control. Use a low-leakage capacitor because of high impedance.
41	FB B			
44	FB G			
46	FB R			
37	GND3	0V		GND for the PSIG circuit.

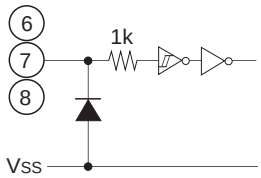
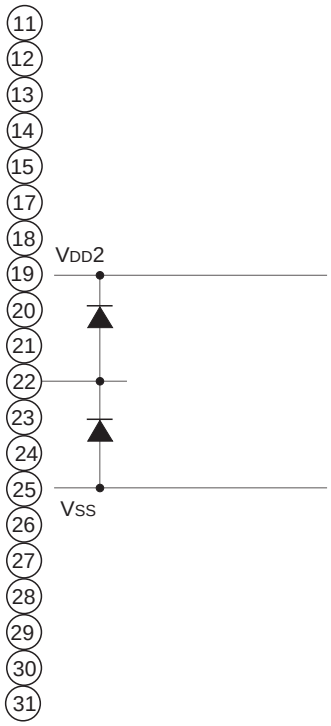
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
38	PSIG	$\frac{Vcc2}{2}$		PSIG signal output.
39	Vcc3	12V		12V power supply for the PSIG circuit.
40	B OUT	$\frac{Vcc2}{2}$		RGB signal outputs.
43	G OUT			
45	R OUT			
42	GND2	0V		12V GND.
47	Vcc2	12V		12V power supply.
48	SIG. CENTER	$\frac{Vcc2}{2}$		RGB/PSIG output DC voltage control. When used with a Vcc2 or Vcc3 of 12V or more, or when used with a signal center voltage of other than Vcc2/2 or Vcc3/2, apply voltage of 5.2 to 6.5V from an external source.
49	Vcc1	3.0V		3.0V power supply.
50	VXO OUT	1.2V		VXO output. Leave this pin open when using Y/color difference mode.
51	VXO IN	1.6V		VXO input. Leave this pin open when using Y/color difference mode.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
52	APC	1.7V		APC detective filter connection. Leave this pin open when using Y/color difference mode.
53	B-Y IN	—		Y/color difference signal inputs. When using color difference input, the standard signal input level is 0.3Vp-p (75% color bar) and the clamp level is approximately 1.7V. During D-PAL, the COUT (Pin 55) chroma signal is U/V separated and then input. Input at low impedance (75Ω or less).
54	R-Y IN			
55	C OUT	1.2V		Color adjusted chroma signal output during D-PAL. The output level is tripled in order to compensate for the attenuation of the external U/V separation delay line. The standard burst output level is approximately 200mVp-p. Leave this pin open in modes other than D-PAL.
56	V REG	2.0V		Smoothing capacitor connection for the internally generated constant voltage source circuit. Connect a capacitor of 1µF or more.
57	C IN	—		Video signal input when using composite signal input. Chroma signal input when using Y/C signal input. Leave this pin open when using Y/color difference mode.

* D-PAL is a demodulation method that uses an external delay line during demodulation.
S-PAL is a demodulation method that internally processes chroma demodulation.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
58	RESET	—		TG block system reset pin. The system is reset when this pin is connected to GND. Connect a capacitor between this pin and GND.
59	Y IN	1.6V		Y signal input. The standard signal input level is 0.5Vp-p (100% white level from the sync tip). Input at low impedance (75Ω or less).
61	SYNC IN	1.6V		Sync input. Normally inputs the Y signal. The standard signal input level is 0.5Vp-p (100% white level from the sync tip). Input at low impedance (75Ω or less).
62	VSEP TC	1.7V		Capacitor connection for vertical sync separation.
63	F0 ADJ	1.5V		Filter reference current generation. Connect resistance of 15 kΩ between this pin and GND1 to adjust the internal filters using the outflow current value. Leave this pin open when using Y/C or Y/color difference mode.
64	GND1	0V		3.0V GND.
60	TEST2	0V		Test. Connect to GND.

Digital Block Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
5	$V_{DD}1$			Power supply for VCO.
6	LOAD			Serial bus inputs.
7	DATA			
8	SCLK			
9	RPD			Phase comparator output.
33	$V_{DD}2$			Power supply for digital block.
10	TEST1			Test. Connect to GND.
11	BLK			Digital block outputs.
12	CLR			
13	HST2			
14	HST1			
15	XHST1			
17	HCK2			
18	HCK1			
19	XPCG			
20	PCG			
21	HD			
22	XVST			
23	VST			
24	VCK4			
25	VCK3			
26	VCK2			
27	VCK1			
28	XEN1			
29	EN1			
30	EN2			
31	VD			

Setting Conditions for Measuring Electrical Characteristics

Use the Electrical Characteristics Measurement Circuit on page 30 while measuring electrical characteristics. Also, the TG (timing generator) block must be initialized by performing Settings 1 and 2 below.

Setting 1. System reset

After turning on the power, set SW58 to ON and start up V58 from GND in order to activate the TG block system reset. (See Fig. 1-1.)
The serial bus is set to the default values.

Setting 2. Horizontal AFC adjustment

Input SIG5 (VL = 0mV) to (A) and adjust serial bus register VCO so that the TP9 phase comparison output waveform (near VSYNC) is horizontal.
SW48 = OFF, SW58 = ON, V58 = 3.0V
(See Fig. 1-2.)

Note) When measuring a band of 2MHz or more such as Y signal frequency response or sharpness characteristics among the items being measured, the measurement must be made with the sample-and-hold circuit set to through (sample and hold not performed) by the serial bus.

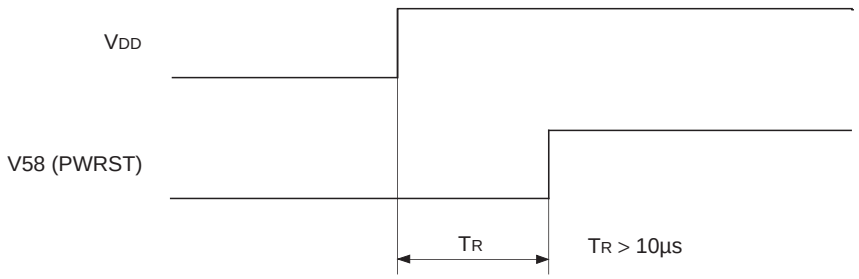


Fig. 1-1. System reset

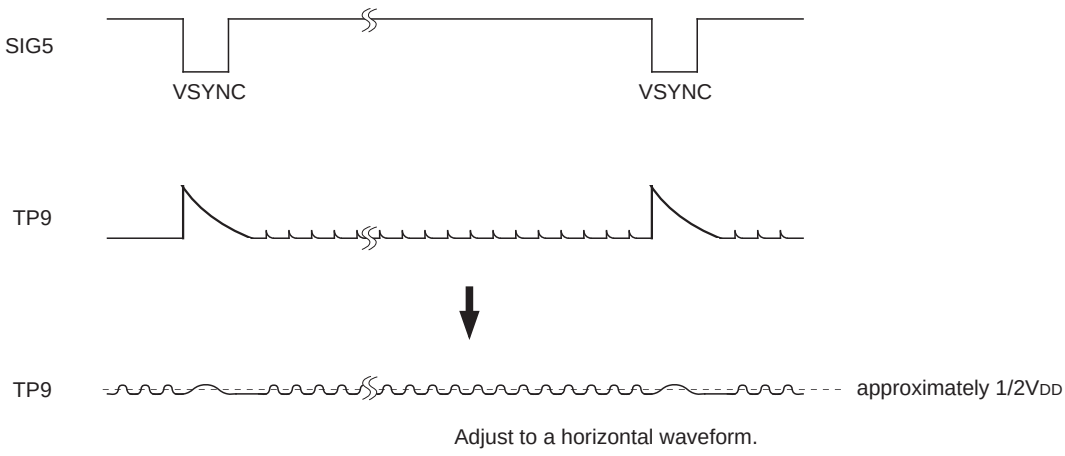


Fig. 1-2. Horizontal AFC adjustment

Electrical Characteristics — DC Characteristics

Unless otherwise specified, Settings 1 and 2 and the following setting conditions are required.
$V_{CC}1$ = 3.0V, $V_{CC}2$ = $V_{CC}3$ = 12.0V, GND1 = GND2 = GND3 = 0V, $V_{DD}1$ = $V_{DD}2$ = 3.0V, V_{SS} = 0V, Ta = 25°C
SW1/SW2/SW3 = A, SW53/SW54/SW57 = B
SW58 = ON, SW48 = OFF
V58 = 3.0V
Set the serial bus registers to the "Serial Bus Register Initial Settings". Unspecified items should be set to the default settings.

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current characteristics						
Current consumption $V_{CC}1$	$I_{CC}11$	Input SIG4 to (A) and SIG2 (0dB) to (B), and measure the $I_{CC}1$ current value. COMP input mode. SW57 = A	27	34	41	mA
	$I_{CC}12$	Input SIG4 to (A) and SIG2 (0dB) to (B), and measure the $I_{CC}1$ current value. Y/C input mode. SW57 = A	24	30	37	mA
	$I_{CC}13$	Input SIG4 to (A), (D) and (E) and measure the $I_{CC}1$ current value. Y/color difference input mode. SW53 = SW54 = A	19	25	30	mA
Current consumption $V_{CC}2$, 3	$I_{CC}2$	Input SIG4 to (A) and SIG2 (0dB) to (B), and measure the $I_{CC}2$ current value. SW57 = A	6	8	10	mA
Current consumption $V_{DD}1$, 2	$I_{DD}1$	Input SIG4 to (A) and SIG2 (0dB) to (B), and measure the $I_{DD}3$ and $I_{DD}4$ current values. $I_{DD}1$ = $I_{DD}3$ + $I_{DD}4$, LCX009AK/AKB SW57 = A	8.5	11	13.5	mA
	$I_{DD}2$	Input SIG4 to (A) and SIG2 (0dB) to (B), and measure the $I_{DD}3$ and $I_{DD}4$ current values. $I_{DD}2$ = $I_{DD}3$ + $I_{DD}4$, LCX005BK/BKB SW57 = A	7.5	10	12.5	mA
Digital block I/O characteristics						
Low level input voltage	VIL	Digital block input pins*1 SW57 = A (A) = SIG4, (B) = SIG2			0.3V_{DD}	V
High level input voltage	VIH	Digital block input pins*1 SW57 = A (A) = SIG4, (B) = SIG2	0.7V_{DD}			V
High level output voltage	VOH1	V_{DD} = 3.0V IOH = –1.2mA*2 SW57 = A (A) = SIG4, (B) = SIG2	2.8			V
		V_{DD} = 2.7V IOH = –1.2mA*2 SW57 = A (A) = SIG4, (B) = SIG2	2.6			V
Low level output voltage	VOL1	IOL = 1.2mA*2 SW57 = A (A) = SIG4, (B) = SIG2			0.3	V

*1 Digital block input pins: SCLK, DATA, LOAD

*2 Output pins except RPD: BLK, CLR, HST2, HST1, XHST1, HCK2, HCK1, XPCG, PCG, HD, XVST, VST, VCK4, VCK3, VCK2, VCK1, XEN1, EN1, EN2, VD

Electrical Characteristics — AC Characteristics

Unless otherwise specified, Settings 1 and 2 and the following setting conditions are required.
$V_{CC}1$ = 3.0V, $V_{CC}2$ = $V_{CC}3$ = 12.0V, GND1 = GND2 = GND3 = 0V, $V_{DD}1$ = $V_{DD}2$ = 3.0V, V_{SS} = 0V, Ta = 25°C
SW1, SW2, SW3 = A SW53, SW54, SW57 = B
SW58 = ON SW48 = OFF
V58 = 3.0V
Set the serial bus registers to the "Serial Bus Register Initial Settings". Unspecified items should be set to the default settings.
Unless otherwise specified, measure the non-inverted outputs for TP40, TP43 and TP45.

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Y signal system							
Video maximum gain	GV	Input SIG4 to (A) and measure the ratio between the output amplitude (white-black) and input amplitude at TP43.		19	21	23	dB
Contrast characteristics TYP	GCNTTP	Input SIG4 to (A) and measure the ratio between the output amplitude (white-black) and input amplitude at TP43.		14	16	18	dB
Contrast characteristics MIN	GCNTMN	Input SIG4 to (A) and measure the ratio between the output amplitude (white-black) and input amplitude at TP43.		–3	1	3	dB
Y signal frequency response	FCYYC	Assume the output amplitude at TP43 when SIG1 (0dB, no burst, 100kHz) is input to (A) as 0dB. Vary the frequency of the input signal to obtain the frequency with an output amplitude of –3dB. CL = 400pF	Y/C input	5.0			MHz
	FCYCMN		Composite input (NTSC)	2.5			MHz
	FCYCMP		Composite input (PAL)	3.0			MHz
Picture quality adjustment variable amount 1 (Y/C input) LCX009AK/AKB	GSHP1X	Assume the output amplitude at TP43 when SIG7 (100kHz) is input to (A) as 0dB. Obtain the amount by which the output amplitude of SIG7 (2.5MHz or 1.8MHz) changes when PICTURE is set to the MAX and MIN values.	2.5MHz MAX	11	14		dB
	GSHP1N		2.5MHz MIN		–3	0	dB
Picture quality adjustment variable amount 2 (Y/C input) LCX005BK/BKB	GSHP2X		1.8MHz MAX	11	14		dB
	GSHP2N		1.8MHz MIN		–1	2	dB
Picture quality adjustment variable amount 3 (composite input) LCX005BK/BKB	GSHP3X	Assume the output amplitude at TP43 when SIG7 (100kHz) is input to (A) as 0dB. Obtain the amount by which the output amplitude of SIG7 (1.8MHz or 2.5MHz) changes when PICTURE is set to the MAX and MIN values.	1.8MHz MAX	8	11		dB
	GSHP3N		1.8MHz MIN		–5	–2	dB
Picture quality adjustment variable amount 4 (composite input) LCX009AK/AKB	GSHP4X		2.5MHz MAX	6	9		dB
	GSHP4N		2.5MHz MIN		–6	–3	dB

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Carrier leak (residual carrier)	CRLEKY	Input SIG2 (0dB) to (A). Using a spectrum analyzer, measure the input and the 3.58MHz or 4.43MHz component of TP43, and obtain $CRLEKY = 150mV \times 10^{\Delta CLK/20}$ using their difference ΔCLK.				30	mV
Y signal I/O delay time	TDYYC	Input SIG9 to (A). Measure the delay time from the 2T pulse peak of the input signal to the 2T pulse peak of the non-inverted output at TP43.	Y/C input	260	360	460	ns
	TDYCMN		Composite input (NTSC)	520	620	720	ns
	TDYCMP		Composite input (PAL)	520	620	720	ns
	TDYDEF		Y/color difference input SW53 = SW54 = A	100	200	300	ns
Chroma signal block							
ACC amplitude characteristics 1	ACC1	Input SIG5 (VL = 150mV) to (A) and SIG2 (0dB/+6dB/–20dB, 3.58MHz burst/chroma phase = 180°, or 4.43MHz burst/chroma phase = ±135°) to (B). Measure the output amplitude at TP55, assuming the output corresponding to 0dB, +6dB and –20dB as V0, V1 and V2, respectively. ACC1 = 20 log (V1/V0) ACC2 = 20 log (V2/V0)	NTSC	–3	0	3	dB
			PAL	–3	0	3	dB
ACC amplitude characteristics 2	ACC2		NTSC	–3	0	3	dB
			PAL	–3	0	3	dB
APC pull-in range	FAPC	Input SIG5 (VL = 150mV) to (A) and SIG2 (0dB, 3.58MHz burst/chroma phase = 180°, or 4.43MHz burst/chroma phase = ±135°) to (B). Vary the SIG2 burst frequency and measure the frequency f1 at which the TP40 output appears (the killer mode is canceled). NTSC: FAPCN = f1 – 3579545Hz PAL: FAPCP = f1 – 4433619Hz	NTSC	±500			Hz
			PAL	±500			Hz
Color adjustment characteristics MAX	GCOLMX	Input SIG5 (VL = 150mV) to (A) and SIG2 (0dB, 3.58MHz burst/chroma phase = 180°) to (B). Assume the chroma signal amplitude at TP55 when serial bus register COLOR = 128, 255 and 0 as V0, V1 and V2, respectively. GCOLMX = 20 log (V1/V0) GCOLMN = 20 log (V2/V0)		+3	+5		dB
Color adjustment characteristics MIN	GCOLMN				–25	–20	dB
HUE adjustment characteristics MAX	HUEMX	Input SIG5 (VL = 150mV) to (A) and SIG2 (0dB, burst/chroma phase variable) to (B). Assume the phase at which the output amplitude at TP40 reaches a minimum when serial bus register HUE = 128, 255 and 0 as θ0, θ1 and θ2, respectively. HUEMX = θ1 – θ0 HUEMN = θ2 – θ0 SW57 = A		–30	–40		deg
HUE adjustment characteristics MIN	HUEMN			30	60		deg

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Killer operation input level	ACKN	Input SIG5 (VL = 150mV) to (A) and SIG2 (level variable, 3.58MHz burst/chroma phase = 180°, or 4.43MHz burst/chroma phase = ±135°) to (B), and measure the output amplitude at TP40. Gradually reduce the SIG2 amplitude level and measure the level at which the killer operation is activated. SW57 = A	NTSC		–36	–30	dB
	ACKP		PAL		–36	–30	dB
Demodulation output amplitude ratio (NTSC)	VRBN	Input SIG5 (VL = 150mV) to (A) and SIG2 (0dB, 3.58MHz) to (B) and vary the chroma phase. Assume the maximum amplitude at TP40 as VB, the maximum amplitude at TP43 as VG, and the maximum amplitude at TP45 as VR. VRBN = VR/VB, VGBN = VG/VB SW57 = A		0.53	0.63	0.73	
	VGBN			0.25	0.32	0.39	
Demodulation output phase difference (NTSC)	θRBN	Input SIG5 (VL = 150mV) to (A) and SIG2 (0dB, 3.58MHz) to (B) and vary the chroma phase. Assume the phase at which the amplitude at TP40, TP43 and TP45 reaches a maximum as θB, θG and θR, respectively. θRBN = θR – θB, θGBN = θG – θB SW57 = A		99	109	119	deg
	θGBN			230	242	254	deg
Demodulation output amplitude ratio (PAL)	VRBP	Input SIG5 (VL = 150mV) to (A) and SIG2 (0dB, 4.43MHz) to (B) and vary the chroma phase. Assume the maximum amplitude at TP40 as VB, the maximum amplitude at TP43 as VG, and the maximum amplitude at TP45 as VR. VRBP = VR/VB, VGBP = VG/VB SW57 = A		0.65	0.75	0.85	
	VGBP			0.33	0.40	0.47	
Demodulation output phase difference (PAL)	θRBP	Input SIG5 (VL = 150mV) to (A) and SIG2 (0dB, 4.43MHz) to (B) and vary the chroma phase. Assume the phase at which the amplitude at TP40, TP43 and TP45 reaches a maximum as θB, θG and θR, respectively. θRBP = θR – θB, θGBP = θG – θB SW57 = A		80	90	100	deg
	θGBP			232	244	256	deg
Color difference input color adjustment characteristics MAX	GEXCMX	Input SIG5 (VL = 150mV) to (A) and SIG1 (0dB, 100kHz, no burst) to (D). Assume the output amplitude at TP40 (100kHz) when serial bus register COLOR = 128 as VC0, when COLOR = 0 as VC2, and when SIG1 is set to –10dB and COLOR = 255 as VC1. GEXCMX = 20 log (VC1/VC0) + 10 GEXCMN = 20 log (VC2/VC0) SW53 = SW54 = A		+3	+5		dB
Color difference input color adjustment characteristics MIN	GEXCMN				–20	–15	dB
Color difference balance	VEXCBL	Input SIG5 (VL = 150mV) to (A) and SIG1 (0dB, 100kHz, no burst) to (D) and (E). Assume the output amplitude at TP40 (100kHz) as VB and the output amplitude at TP45 (100kHz) as VR. VEXCBL = VR/VB SW53 = SW54 = A		0.8	1.0	1.2	

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Color difference input balance adjustment R	GEXRMX	Input SIG5 (VL = 150mV) to (A) and SIG1 (–6dB, 100kHz, no burst) to (D) and (E). Assume the output amplitude at TP45 (100kHz) and TP40 (100kHz) when serial bus register HUE = 128 as VR0 and VB0, respectively, when HUE = 255 as VR1 and VB1, respectively, and when HUE = 0 as VR2 and VB2, respectively. GEXRMX = 20 log (VR1/VR0) GEXRMN = 20 log (VR2/VR0) GEXBMX = 20 log (VB1/VB0) GEXBMN = 20 log (VB2/VB0) SW53 = SW54 = A		–5	–2	dB
	GEXRMN		+2	+3		dB
Color difference input balance adjustment B	GEXBMX		+2	+3		dB
	GEXBMN			–5	–2	dB
G-Y matrix characteristics (NTSC)	VEXGBN	Input SIG5 (VL = 150mV) to (A) and SIG1 (0dB, 100kHz, no burst) to (D). Assume the output amplitude at TP40 (100kHz) as VEXB and the output amplitude at TP43 (100kHz) as VEXBG. VEXGBN = VEXBG/VEXB SW53 = SW54 = A	0.23	0.26	0.29	
	VEXGRN	Input SIG5 (VL = 150mV) to (A) and SIG1 (0dB, 100kHz, no burst) to (E). Assume the output amplitude at TP45 (100kHz) as VEXR and the output amplitude at TP43 (100kHz) as VEXRG. VEXGRN = VEXRG/VEXR SW53 = SW54 = A	0.46	0.51	0.56	
G-Y matrix characteristics (PAL)	VEXGBP	Input SIG5 (VL = 150mV) to (A) and SIG1 (0dB, 100kHz, no burst) to (D). Assume the output amplitude at TP40 (100kHz) as VEXB and the output amplitude at TP43 (100kHz) as VEXBG. VEXGBP = VEXBG/VEXB SW53 = SW54 = A	0.17	0.20	0.23	
	VEXGRP	Input SIG5 (VL = 150mV) to (A) and SIG1 (0dB, 100kHz, no burst) to (E). Assume the output amplitude at TP45 (100kHz) as VEXR and the output amplitude at TP43 (100kHz) as VEXRG. VEXGRP = VEXRG/VEXR SW53 = SW54 = A	0.46	0.51	0.56	
RGB signal output block						
RGB signal and PSIG output DC voltage	VOUT	Input SIG5 (VL = 0mV) to (A). Adjust serial bus registers BRIGHT and PSIG-BRT so that the output (black-black) at TP43 and TP38 is 9Vp-p and measure the DC voltage at TP40, TP43, TP45 and TP38.	5.85	6.00	6.15	V
RGB signal and PSIG output DC voltage difference	ΔVOUT	Input SIG5 (VL = 0mV) to (A). Adjust serial bus registers BRIGHT and PSIG-BRT so that the output (black-black) at TP43 and TP38 is 9Vp-p, measure the DC voltage at TP40, TP43, TP45 and TP38, and obtain the maximum difference between each of these values.		0	100	mV
SIG center variable range	VORNG	Set V48 to 5.2V or 6.5V in the VOUT measurement conditions and confirm that ΔVOUT in the preceding item is satisfied and that $\|V48 - VOUT\| \leq 0.15V$. SW48 = ON	5.2		6.5	V

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
RGB and PSIG output black limiter operation voltage	VLIMMX	Input SIG3 to (A). Vary BLKLIM and measure the maximum value VLIMMX and minimum value VLIMMN of the voltage range (black-black) over which the black limiter operates for the TP38, TP40, TP43 and TP45 outputs. Assume the value when BLKLIM = 0 as VLIMMX, and when BLKLIM = 255 as VLIMMN.	9.0			Vp-p
	VLIMMN				7.0	Vp-p
Amount of change in PSIG output	PSIGMX	Input SIG3 (VL = 0mV) to (A) and measure the output (black-black) at TP38 when serial bus register PSIG-BRT = 255.	9.0			Vp-p
	PSIGMN	Input SIG3 (VL = 0mV) to (A) and measure the output (black-black) at TP38 when serial bus register PSIG-BRT = 0.			1.5	Vp-p
Amount of change in user brightness	UBRTMX	Input SIG3 to (A) and measure the amount of change in the black level output at TP40, TP43 and TP45 when serial bus register USER-BRT is changed from 128 to 255.	2.5	3.0		V
	UBRTMN	Input SIG3 to (A) and measure the amount of change in the white level output at TP40, TP43 and TP45 when serial bus register USER-BRT is changed from 128 to 0.		–3.0	–2.5	V
Amount of change in brightness	BRTMX	Input SIG3 to (A) and measure the black level output at TP40, TP43 and TP45 when serial bus register BRIGHT is changed from 128 to 255.	2.0	2.5		V
	BRTMN	Input SIG3 to (A) and measure the white level output at TP40, TP43 and TP45 when serial bus register BRIGHT is changed from 128 to 0.		–2.5	–2.0	V
Amount of change in sub-brightness	SBBRT	Input SIG5 (VL = 0mV) to (A) and measure the difference between the outputs (black-black) at TP40 and TP45 and the output (black-black) at TP43 when serial bus registers R-BRT = B-BRT = 0 and when R-BRT = B-BRT = 255.	±1.3	±1.7		V
Difference in gain between RGB output signals	ΔGRGB	Input SIG4 to (A) and obtain the level difference between the maximum and minimum non-inverted output amplitudes (white-black) at TP40, TP43 and TP45.	–0.6	0	0.6	dB
Amount of change in sub-contrast	SBCNT	Input SIG4 to (A) and measure the difference between the non-inverted outputs (white-black) at TP40 and TP45 and the non-inverted output (white-black) at TP43 when serial bus registers R-CNT = B-CNT = 0 and when R-CNT = B-CNT = 255.	±1.5	±2		dB
Difference in RGB output inverted/ non-inverted gain	ΔGINV	Input SIG4 to (A) and obtain the difference between the non-inverted output amplitudes (white-black) and the inverted output amplitudes at TP40, TP43 and TP45.	–0.3	0	0.3	dB
Difference in black level potential between RGB output signals	ΔVBL	Input SIG4 to (A) and obtain the level difference between the maximum and minimum black levels of both the inverted and non-inverted outputs at TP40, TP43 and TP45.			300	mV

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
γ gain	Gγ1	Input SIG8 to (A). Adjust the non-inverted output amplitude (black-white) at TP43 to 3.5Vp-p with serial bus register CONT and the black level at TP43 to 1.5V with serial bus register RBT. Measure VG1, VG2 and VG3. Gγ1 = 20 log (VG1/0.0375) Gγ2 = 20 log (VG2/0.0375) Gγ3 = 20 log (VG3/0.0375) (See Fig. 5 for definitions of VG1, VG2 and VG3.)	23.0	26.0	29.0	dB
	Gγ2		12.0	15.0	18.0	dB
	Gγ3		18.0	22.0	26.0	dB
γ1 adjustment variable range	Vγ1MN	Input SIG8 to (A) and adjust serial bus register BRIGHT so that the output at TP43 is 9Vp-p (black-black). Read the point where the gain of the non-inverted output at TP43 changes when serial bus register γ1 = 0 and 255 from the input signal IRE level. Vγ1MN when γ1 = 0, and Vγ1MX when γ1 = 255.			0	IRE
	Vγ1MX		100			IRE
γ2 adjustment variable range	Vγ2MN	Input SIG8 to (A) and adjust serial bus register BRIGHT so that the output at TP43 is 9Vp-p (black-black). Read the point where the gain of the non-inverted output at TP43 changes when serial bus register γ2 = 0 and 255 from the input signal IRE level. Vγ2MN when γ2 = 0, and Vγ2MX when γ2 = 255.	100			IRE
	Vγ2MX				0	IRE
PSIG transition time	tPSIGH	Input SIG4 to (A) and adjust serial bus register PSIG-BRT so that the output at TP38 is 9Vp-p (black-black). Measure the time it takes to change to an amplitude of 9Vp-p. tPSIGH: rise time, tPSIGL: fall time Load: 20000pF		1.5	3.0	µs
	tPSIGL			1.5	3.0	µs
RGB output white limiter operation voltage	VWLIMX	Input SIG3 to (A) and measure the potential difference between the white limiter level of the TP43 output and SIGCENTER. VWLIMX when WHITELIM = 0 VWLIMN when WHITELIM = 3	1.0	1.1	1.2	V
	VWLIMN		0.45	0.55	0.65	V
Black limiter DC voltage difference	ΔVBLIM	Input SIG5 (VL = 0mV) to (A) and adjust BLKLIM so that the output at TP43 is 9Vp-p (black-black). Measure the DC voltage at TP40, TP43 and TP45 and obtain the difference versus the RGB output voltage VOUT.		0	100	mV
White limiter DC voltage difference	ΔVWLIM	Input SIG5 (VL = 350mV) to (A). Measure the DC voltage at TP40, TP43 and TP45 and obtain the difference versus the RGB output voltage VOUT.		0	100	mV
RGB output range when FRP polarity inversion is stopped	VDROFF	Input SIG8 to (A). Assume the black limiter level of the output at TP40, TP43 and TP45 when serial bus register BRIGHT = 0 as VDRB and the white limiter level when BRIGHT = 255 as VDRW. VDROFF = VDRW – VDRB	3.0			Vp-p

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Filter characteristics							
Amount of BPF attenuation	ATBPF	Assume the chroma amplitude at TP55 when SIG5 (VL = 0mV) is input to (A) and SIG1 (0dB at input center frequency (3.58MHz or 4.43MHz)) is input to (B) as 0dB. Obtain the amount by which the output at TP55 is attenuated when the frequencies noted on the right are input. SW57 = A	NTSC 1.5MHz		–18	–12	dB
			PAL 2.0MHz		–16	–10	dB
			NTSC 5.5MHz		–6	–2	dB
			PAL 6.8MHz		–6	–2	dB
Amount of TRAP attenuation	ATRAPN	Input SIG2 (0dB, 3.58MHz and 4.43MHz) to (A) and measure the output at TP43 with a spectrum analyzer. Assume the amplitude at TP43 during Y/C input mode as 0dB, and obtain the amount of attenuation during COMP input mode.	NTSC		–40	–30	dB
	ATRAPP		PAL		–40	–30	dB
R-Y and B-Y LPF characteristics	DEMLPF	Assume the amplitude of the 100kHz component of the output at TP43 when SIG5 (VL = 150mV) is input to (A) and SIG2 (0dB, 3.58MHz + 100kHz) is input to (B) as 0dB. Obtain the frequency which attenuates the beat component of the output by 3dB when the SIG2 frequency is increased with respect to 3.58MHz.		0.9	1.2	1.5	MHz
Sync separation, TG block							
Input sync signal width sensitivity	WSSEP	Input SIG5 (VL = 0mV, VS = 143mV, WS variable) to (A) and confirm that it is synchronized with the HD output at TP21. Gradually narrow the WS of SIG5 from 4.7µs and obtain the WS at which synchronization with the HD output at TP21 is lost.		2.0			µs
Sync separation input sensitivity	VSSEP	Input SIG5 (VL = 0mV, WS = 4.7µs, VS variable) to (A) and confirm that it is synchronized with the HD output at TP21. Gradually reduce the VS of SIG5 from 143mV and obtain the VS at which synchronization with the HD output at TP21 is lost.			40	60	mV
HD output delay time	TDSY1	Input SIG5 (VL = 0mV, WS = 4.7µs, VS = 143mV) to (A) and measure the delay time with the HD output at TP21. TDSY1 is from the falling edge of the input HSYNC to the rising edge of the HD output, and TDSY2 is from the falling edge of the input HSYNC to the falling edge of the HD output.		2.3	2.6	2.9	µs
	TDSY2			4.3	4.6	4.9	µs
Horizontal pull-in range	HPLLN	Input SIG5 (VL = 0mV, WS = 4.7µs, VS = 143mV, horizontal frequency variable) to (A) and confirm that it is synchronized with the HD output at TP21. Obtain the frequency f_H at which the input and output are synchronized by changing the horizontal frequency of SIG5 from the non-synchronized condition. HPLLN = f_H – 15734, HPLLP = f_H – 15625	NTSC	±500	±1000		Hz
	HPLLP		PAL	±500	±1000		Hz

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output transition time (page 11*2 pins)	tTLH	Input SIG5 (VL = 0mV) to (A) and measure the transition time for each output. Load = 50pF (See Fig. 3.) SW57 = A			30	ns
	tTHL				30	ns
Cross-point time difference	ΔT	Input SIG5 (VL = 0mV) to (A) and measure HCK1/HCK2, VCK1/VCK2 and VCK3/VCK4. Load = 50pF (See Fig. 4.) SW57 = A			10	ns
HCK duty	DTYHC	Input SIG5 (VL = 0mV) to (A) and measure the HCK1/HCK2 duty. Load = 50pF, SW57 = A	47	50	53	%
DA OUT output voltage	VBKLTH	Measure the output voltage at TP23 when DA OUT = 7. I_{OH} = –1mA	2.7			V
	VBKLTL	Measure the output voltage at TP23 when DA OUT = 0. I_{OH} = 1mA			0.3	V
External I/O characteristics						
External RGB input threshold voltage	VTEXTB	Input SIG5 (VL = 0mV) to (A) and SIG6 (VL variable) to (C). Raise the SIG6 amplitude (VL) from 0V and assume the voltage where the outputs at TP40, TP43 and TP45 go to black level as VTEXTB. Then raise the amplitude further and assume the voltage where these outputs go to white level as VTEXTW. SW1 = SW2 = SW3 = B	0.8	1.0	1.2	V
	VTEXTW		1.8	2.0	2.2	V
Propagation delay time between external RGB input and output	TD1EXT	Input SIG5 (VL = 0mV) to (A) and SIG6 (VL = 3V) to (C). Measure the rise delay time TD1EXT and the fall delay time TD2EXT of the outputs at TP40, TP43 and TP45. (See Fig. 2.) SW1 = SW2 = SW3 = B	50	90	130	ns
	TD2EXT		50	100	140	ns
Output blanking level during external RGB input	EXTBK	Input SIG5 (VL = 0mV) to (A) and SIG6 (VL = 1.7V) to (C). Measure the difference from the black level of the outputs at TP40, TP43 and TP45. SW1 = SW2 = SW3 = B			0	V
Output white level during external RGB input	EXTWT	Input SIG5 (VL = 0mV) to (A) and SIG6 (VL = 2.7V) to (C). Measure the difference from the black level of the outputs at TP40, TP43 and TP45. SW1 = SW2 = SW3 = B	3.0			V
Minimum pulse width during external RGB input	TEXMIN	Input SIG5 (VL = 0mV) to (A) and SIG6 (VL = 2.7V) to (C). Measure the minimum pulse width at which each of the outputs at TP40, TP43 and TP45 reach the white limiter. SW1 = SW2 = SW3 = B			180	ns

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Serial transfer block						
Data setup time	ts0	LOAD setup time, activated by the rising edge of SCLK. (See Fig. 6.)	150			ns
	ts1	DATA setup time, activated by the rising edge of SCLK. (See Fig. 6.)	150			ns
Data hold time	th0	LOAD hold time, activated by the rising edge of SCLK. (See Fig. 6.)	150			ns
	th1	DATA hold time, activated by the rising edge of SCLK. (See Fig. 6.)	150			ns
Minimum pulse width	tw1L	SCLK pulse width. (See Fig. 6.)	156			ns
	tw1H	SCLK pulse width. (See Fig. 6.)	156			ns
	tw2	LOAD pulse width. (See Fig. 6.)	1			µs

Description of Electrical Characteristics Measurement Methods
Serial Bus Register Initial Settings

Item		Symbol	Serial bus																				
			Mode settings					DAC settings															
			Input	System	Panel	S/H	FRP	HUE	COL	BRT	CNT	R-BRT	B-BRT	γ1	γ2	PSIG BRT	R-CNT	B-CNT	BLK LIM	PIC	USER-BRT	VCO	WHITE LIM	DA OUT
Setting 2	Horizontal AFC adjustment		COMP	NTSC	—	1	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
Current characteristics	Current consumption $V_{CC}1$	$I_{CC}11$	COMP	NTSC	—	1	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
		$I_{CC}12$	Y/C	NTSC	—	1	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
		$I_{CC}13$	Y/color difference	NTSC	—	1	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	Current consumption $V_{CC}2$, 3	$I_{CC}2$	COMP	NTSC	501	1	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	Current consumption $V_{DD}1$, 2	$I_{DD}1$	COMP	NTSC	009	1	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
		$I_{DD}2$	COMP	NTSC	005	1	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
Digital block I/O characteristics	Low level input voltage	VIL	COMP	NTSC	—	1	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	High level input voltage	VIH	COMP	NTSC	—	1	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	High level output voltage	VOH1	COMP	NTSC	—	1	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	Low level output voltage	VOL1	COMP	NTSC	—	1	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
Y signal block	Video maximum gain	GV	COMP	NTSC	—	ALL	ON	128	128	128	255	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	Contrast characteristics TYP	GCNTTP	COMP	NTSC	—	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	Contrast characteristics MIN	GCNTMN	COMP	NTSC	—	ALL	ON	128	128	128	0	128	128	0	0	128	128	128	0	128	128	ADJ	3	—

VCO must be reset when the panel mode is changed.

(—: don't care, ADJ: adjustment, SET: setting)

Item		Symbol	Serial bus																					
			Mode settings					DAC settings																
			Input	System	Panel	S/H	FRP	HUE	COL	BRT	CNT	R-BRT	B-BRT	γ1	γ2	PSIG BRT	R-CNT	B-CNT	BLK LIM	PIC	USER-BRT	VCO	WHITE LIM	DA OUT
Y signal block	Y signal frequency response	FCYYC	Y/C	NTSC	009	ALL	ON	128	128	128	128	128	180	0	0	128	128	128	0	180	128	ADJ	3	—
		FCYCMN	COMP	NTSC	005	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
		FCYCMP	COMP	SPAL	005	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	Picture quality adjustment variable amount 1	GSHP1X	Y/C	NTSC	009	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	255	128	ADJ	3	—
		GSHP1N	Y/C	NTSC	009	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	0	128	ADJ	3	—
	Picture quality adjustment variable amount 2	GSHP2X	Y/C	NTSC	005	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	255	128	ADJ	3	—
		GSHP2N	Y/C	NTSC	005	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	0	128	ADJ	3	—
	Picture quality adjustment variable amount 3	GSHP3X	COMP	NTSC	005	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	255	128	ADJ	3	—
		GSHP3N	COMP	NTSC	005	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	0	128	ADJ	3	—
	Picture quality adjustment variable amount 4	GSHP4X	COMP	NTSC	009	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	255	128	ADJ	3	—
		GSHP4N	COMP	NTSC	009	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	0	128	ADJ	3	—
	Carrier leak (Y block)	CRLEKY	COMP	—	—	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	Y signal I/O delay time	TDYYC	Y/C	—	—	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
		TDYCMN	COMP	NTSC	—	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
		TDYCMP	COMP	SPAL	—	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
		TDYDEF	Y/color difference	—	—	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
Chroma signal block	ACC amplitude characteristics 1	ACC1	COMP	NTSC	—	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
			COMP	SPAL	—	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	ACC amplitude characteristics 2	ACC2	COMP	NTSC	—	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
			COMP	SPAL	—	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	APC pull-in range	FAPC	COMP	NTSC	—	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
			COMP	SPAL	—	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—

VCO must be reset when the panel mode is changed.

(—: don't care, ADJ: adjustment, SET: setting)

Item		Symbol	Serial bus																					
			Mode settings					DAC settings																
			Input	System	Panel	S/H	FRP	HUE	COL	BRT	CNT	R-BRT	B-BRT	γ1	γ2	PSIG BRT	R-CNT	B-CNT	BLK LIM	PIC	USER -BRT	VCO	WHITE LIM	DA OUT
Chroma signal block	Color adjustment characteristics MAX	GCOLMX	COMP	NTSC	—	ALL	ON	128	255	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	Color adjustment characteristics MIN	GCOLMN	COMP	NTSC	—	ALL	ON	128	0	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	HUE adjustment characteristics MAX	HUEMX	COMP	NTSC	—	ALL	ON	255	128	150	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	HUE adjustment characteristics MIN	HUEMN	COMP	NTSC	—	ALL	ON	0	128	150	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	Killer operation input level	ACKN	COMP	NTSC	—	ALL	ON	128	128	150	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
		ACKP	COMP	SPAL	—	ALL	ON	128	128	150	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	Demodulation output amplitude ratio (NTSC)	VRBN	COMP	NTSC	—	ALL	ON	128	128	150	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
		VGBN	COMP	NTSC	—	ALL	ON	128	128	150	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	Demodulation output phase difference (NTSC)	θRBN	COMP	NTSC	—	ALL	ON	128	128	150	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
		θGBN	COMP	NTSC	—	ALL	ON	128	128	150	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	Demodulation output amplitude ratio (PAL)	VRBP	COMP	SPAL	—	ALL	ON	128	128	150	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
		VGBP	COMP	SPAL	—	ALL	ON	128	128	150	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	Demodulation output phase difference (PAL)	θRBP	COMP	SPAL	—	ALL	ON	128	128	150	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
		θGBP	COMP	SPAL	—	ALL	ON	128	128	150	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	Color difference input color adjustment	GEXCMX	Y/color difference	—	—	ALL	ON	128	255	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
		GEXCMN	Y/color difference	—	—	ALL	ON	128	0	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	Color difference balance	VEXCBL	Y/color difference	—	—	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—

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Item		Symbol	Serial bus																					
			Mode settings					DAC settings																
			Input	System	Panel	S/H	FRP	HUE	COL	BRT	CNT	R-BRT	B-BRT	γ1	γ2	PSIG BRT	R-CNT	B-CNT	BLK LIM	PIC	USER-BRT	VCO	WHITE LIM	DA OUT
Chroma signal block	Color difference input balance adjustment R	GEXRMX	Y/color difference	—	—	ALL	ON	255	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
		GEXRMN	Y/color difference	—	—	ALL	ON	0	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	Color difference input balance adjustment B	GEXBMX	Y/color difference	—	—	ALL	ON	255	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
		GEXBMN	Y/color difference	—	—	ALL	ON	0	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	G-Y matrix characteristics (NTSC)	VEXGBN	Y/color difference	NTSC	—	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
		VEXGRN	Y/color difference	NTSC	—	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	G-Y matrix characteristics (PAL)	VEXGBP	Y/color difference	SPAL	—	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
		VEXGRP	Y/color difference	SPAL	—	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
RGB signal output block	RGB/PSIG output DC voltage	VOUT	—	—	—	ALL	ON	128	128	ADJ	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	RGB/PSIG output DC voltage difference	ΔVOUT	—	—	—	ALL	ON	128	128	ADJ	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	SIG center variable range	VORNG	—	—	—	ALL	ON	128	128	ADJ	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	RGB output/PSIG black limiter operation voltage	VLIMMX	—	—	—	ALL	ON	128	128	80	255	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
		VLIMMN	—	—	—	ALL	ON	128	128	80	255	128	128	0	0	128	128	128	255	128	128	ADJ	3	—
	Amount of change in PSIG output	PSIGMX	—	—	—	ALL	ON	128	128	128	255	128	128	0	0	255	128	128	0	128	128	ADJ	3	—
		PSIGMN	—	—	—	ALL	ON	128	128	128	255	128	128	0	0	0	128	128	0	128	128	ADJ	3	—

VCO must be reset when the panel mode is changed.

(—: don't care, ADJ: adjustment, SET: setting)

	Item	Symbol	Serial bus																					
			Mode settings					DAC settings																
			Input	System	Panel	S/H	FRP	HUE	COL	BRT	CNT	R-BRT	B-BRT	γ1	γ2	PSIG BRT	R-CNT	B-CNT	BLK LIM	PIC	USER-BRT	VCO	WHITE LIM	DA OUT
RGB signal output block	Amount of change in user brightness	UBRTMX	—	—	—	ALL	ON	128	128	128	255	128	128	0	0	128	128	128	0	128	255	ADJ	3	—
		UBRTMN	—	—	—	ALL	ON	128	128	128	255	128	128	0	0	128	128	128	0	128	0	ADJ	3	—
	Amount of change in brightness	BRTMX	—	—	—	ALL	ON	128	128	255	255	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
		BRTMN	—	—	—	ALL	ON	128	128	0	255	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	Amount of change in sub brightness	SBBRT	—	—	—	ALL	ON	128	128	160	128	SET	SET	0	0	128	128	128	0	128	128	ADJ	3	—
	Difference in gain between RGB signals	ΔGRGB	—	—	—	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	Amount of change in sub-contrast	SBCNT	—	—	—	ALL	ON	128	128	128	128	128	128	0	0	128	SET	SET	0	128	128	ADJ	3	—
	Difference in RGB inverted/non-inverted gain	ΔGINV	—	—	—	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	Difference in black level potential between RGB signals	ΔVBL	—	—	—	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	γ gain	Gγ1	—	—	—	ALL	ON	128	128	ADJ	ADJ	128	128	140	230	128	128	128	0	128	128	ADJ	3	—
		Gγ2	—	—	—	ALL	ON	128	128	ADJ	ADJ	128	128	140	230	128	128	128	0	128	128	ADJ	3	—
		Gγ3	—	—	—	ALL	ON	128	128	ADJ	ADJ	128	128	140	230	128	128	128	0	128	128	ADJ	3	—
	γ1 adjustment variable range	Vγ1MN	—	—	—	ALL	ON	128	128	80	60	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
		Vγ1MX	—	—	—	ALL	ON	128	128	80	60	128	128	255	0	128	128	128	0	128	128	ADJ	3	—
	γ2 adjustment variable range	Vγ2MN	—	—	—	ALL	ON	128	128	80	60	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
		Vγ2MX	—	—	—	ALL	ON	128	128	80	60	128	128	0	255	128	128	128	0	128	128	ADJ	3	—
	PSIG transition time	tPSIG	—	—	—	ALL	ON	128	128	128	128	128	128	128	128	SET	128	128	0	128	128	ADJ	3	—

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Item		Symbol	Serial bus																					
			Mode settings					DAC settings																
			Input	System	Panel	S/H	FRP	HUE	COL	BRT	CNT	R-BRT	B-BRT	γ1	γ2	PSIG BRT	R-CNT	B-CNT	BLK LIM	PIC	USER-BRT	VCO	WHITE LIM	DA OUT
RGB signal output block	RGB output white limiter operation voltage	VWLIM	—	—	—	ALL	ON	128	128	128	128	128	128	0	255	128	128	128	0	128	0	ADJ	SET	—
	Black limiter DC voltage difference	ΔVBLIM	—	—	—	ALL	ON	128	128	0	128	128	128	0	0	128	128	128	ADJ	128	128	ADJ	0	—
	White limiter DC voltage difference	ΔVWLIM	—	—	—	ALL	ON	128	128	255	128	128	128	0	0	128	128	128	0	128	128	ADJ	0	—
	RGB output range when FRP polarity inversion is stopped	VDROFF	—	—	—	ALL	OFF	128	128	SET	128	128	128	0	0	128	128	128	0	128	0	ADJ	3	—
Filter characteristics	Amount of BPF attenuation	ATBPF	COMP	SET	—	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	Amount of TRAP attenuation	ATRAPN	SET	NTSC	—	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
		ATRAPP	SET	SPAL	—	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	R-Y and B-Y LPF characteristics	DEMLPF	Y/C	NTSC	—	ALL	ON	128	128	150	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
Sync, TG block	Input sync signal width sensitivity	WSSEP	—	—	—	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	Sync separation input sensitivity	VSSEP	—	—	—	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	HD output delay time	TDSY1	—	NTSC	009	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
		TDSY2	—	NTSC	009	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	Horizontal pull-in range	HPLLN	—	NTSC	—	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
		HPLLP	—	SPAL	—	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	Output transition time	tTLH	COMP	NTSC	—	1	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
		tTHL	COMP	NTSC	—	1	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—

VCO must be reset when the panel mode is changed.

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Item		Symbol	Serial bus																					
			Mode settings					DAC settings																
			Input	System	Panel	S/H	FRP	HUE	COL	BRT	CNT	R-BRT	B-BRT	γ1	γ2	PSIG BRT	R-CNT	B-CNT	BLK LIM	PIC	USER-BRT	VCO	WHITE LIM	DA OUT
Sync, TG block	Cross-point time difference	ΔT	COMP	NTSC	—	1	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	HCK duty	DTYHC	COMP	NTSC	—	1	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	DA OUT output voltage	VBKLTH	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	7
		VBKLTL	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0
External I/O characteristics	External RGB input threshold voltage	VTEXTB	—	—	—	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
		VTEXTW	—	—	—	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	Propagation delay time between external RGB input and output	TD1EXT	—	—	—	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
		TD2EXT	—	—	—	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	External RGB input blanking level	EXTBK	—	—	—	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	External RGB input output white level	EXTWT	—	—	—	ALL	ON	128	128	100	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—
	External RGB input minimum pulse width	TEXMIN	—	—	—	ALL	ON	128	128	128	128	128	128	0	0	128	128	128	0	128	128	ADJ	3	—

VCO must be reset when the panel mode is changed.

(—: don't care, ADJ: adjustment, SET: setting)

Electrical Characteristic Measurement Method Diagrams

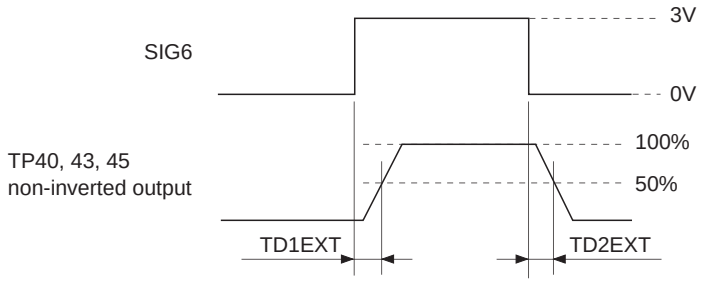


Fig. 2. Conditions for measuring the delay between external RGB input and output

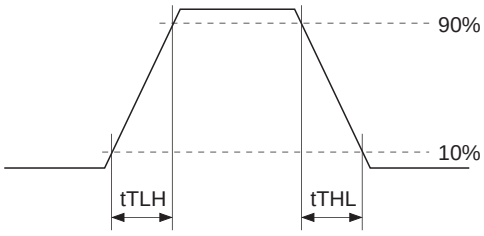


Fig. 3. Output transition time measurement conditions

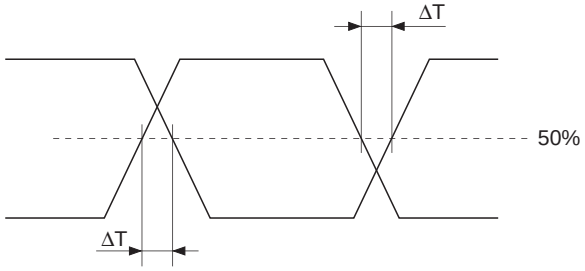


Fig. 4. Cross-point time difference measurement conditions

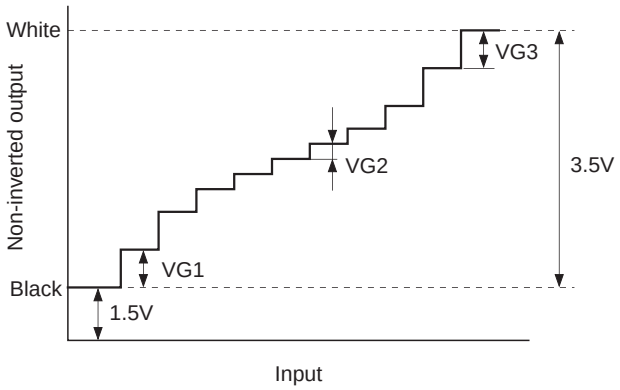


Fig. 5. γ characteristics measurement conditions

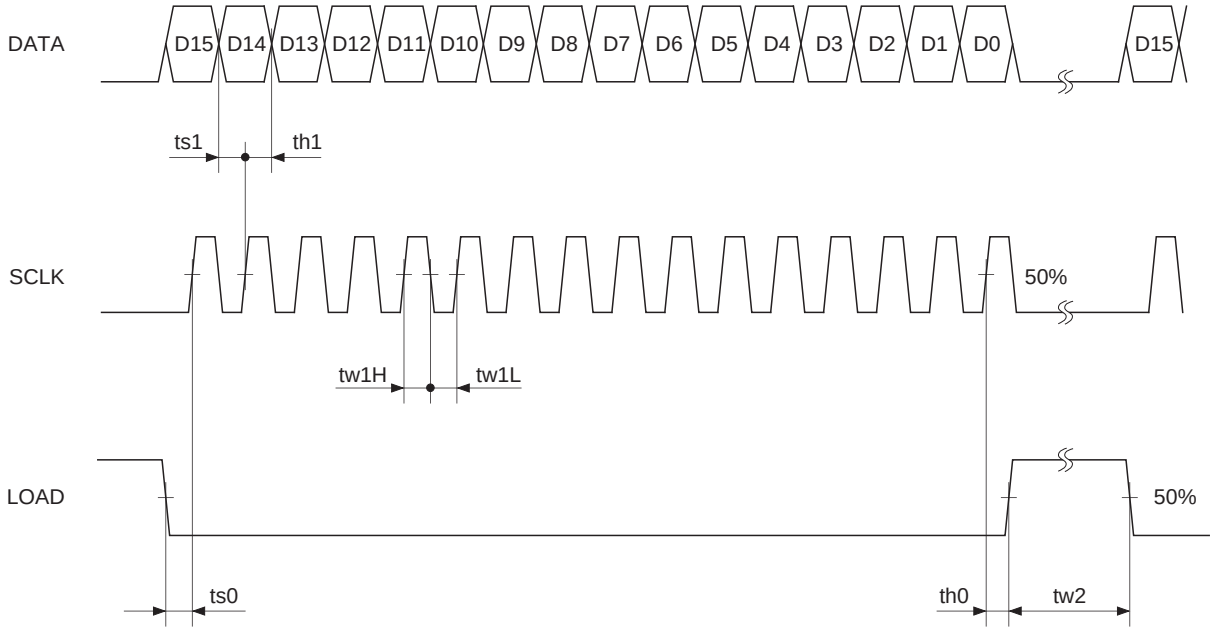
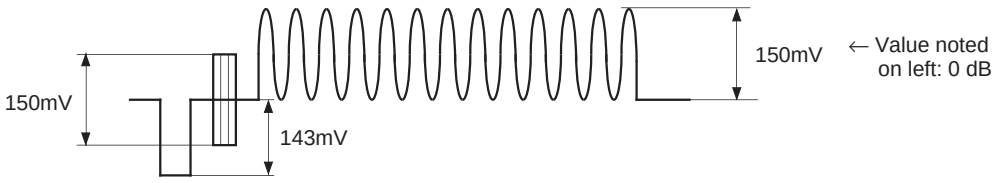
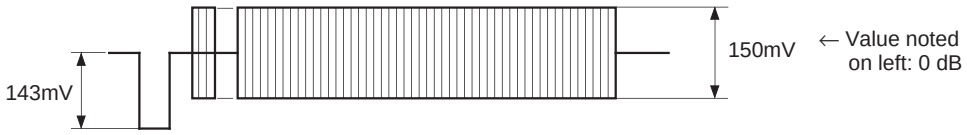
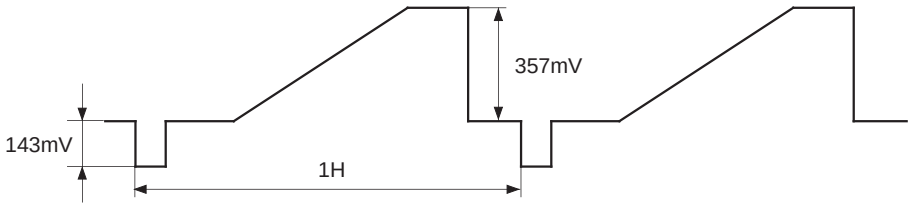
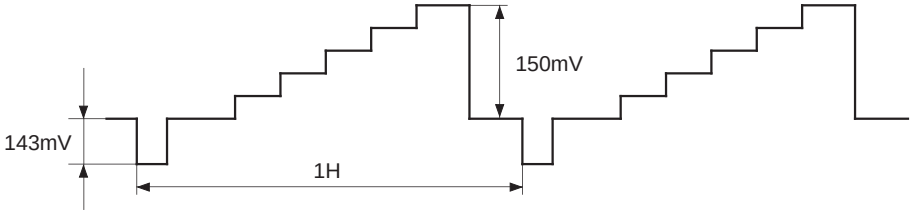
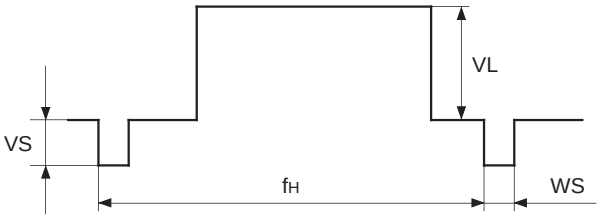
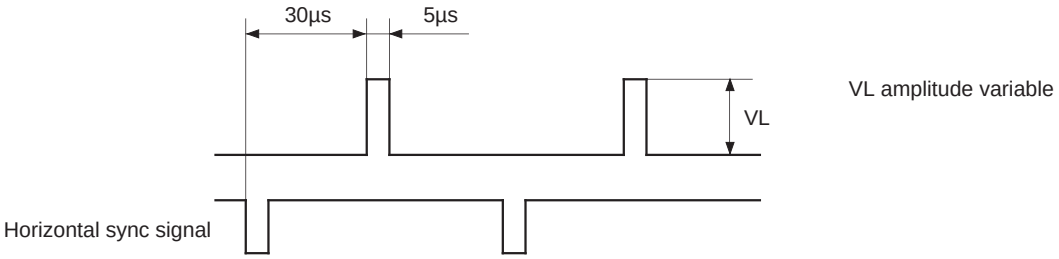
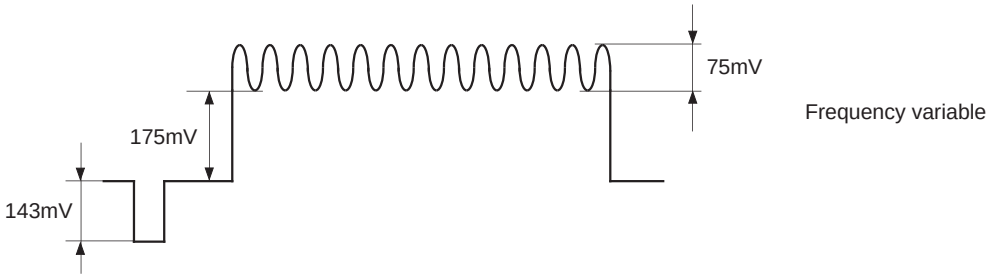
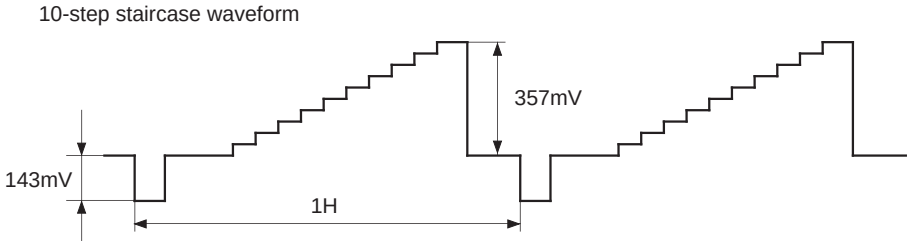
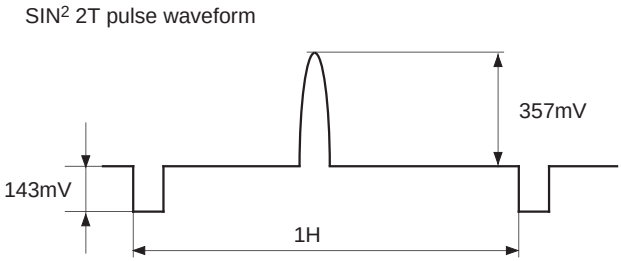


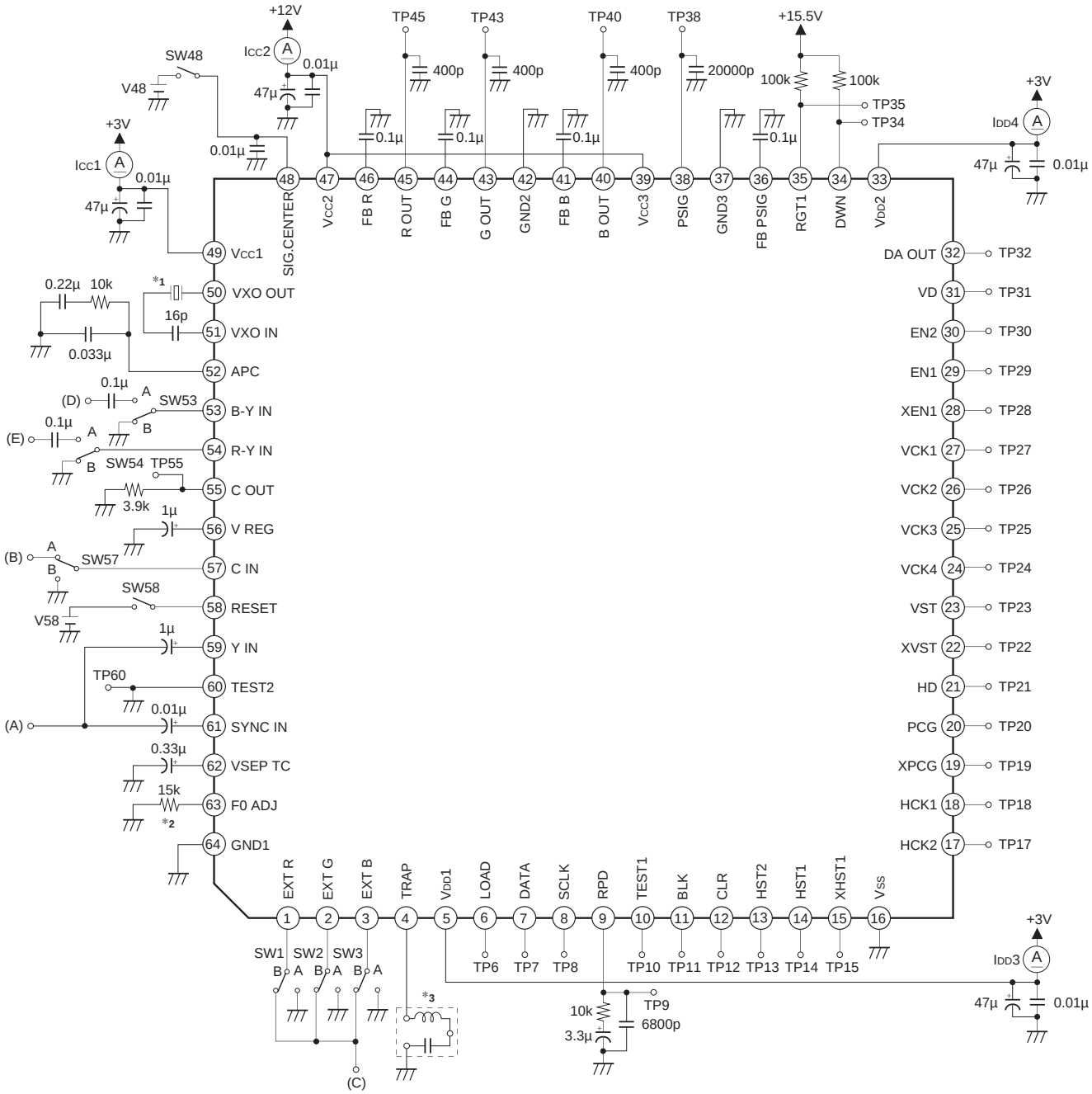
Fig. 6. Serial transfer block measurement conditions

Input Waveforms

SG No.	Waveform
SIG1	Sine wave video signal: With/without burst Amplitude and frequency variable 
SIG2	Chroma signal: Burst, chroma frequency (3.579545MHz, 4.433619MHz) Chroma phase and burst frequency variable 
SIG3	Ramp waveform 
SIG4	5-step staircase waveform 
SIG5	 VL amplitude variable VS variable: 143mV unless otherwise specified WS variable: 4.7µs unless otherwise specified fH variable: 15.734kHz (NTSC) or 15.625kHz (PAL) unless otherwise specified

SG No.	Waveform
SIG6	
SIG7	
SIG8	
SIG9	

Electrical Characteristics Measurement Circuit



*1 Used crystal: KINSEKI CX-5F
Frequency deviation: within ±30ppm,
frequency temperature characteristics: within ±30ppm,
load capacity: 16pF
NTSC: 3.579545MHz
PAL: 4.433619MHz

*2 Resistance value tolerance: ±2%,
temperature coefficient: ±200ppm or less

*3 Trap (TDK)
NTSC: NLT4532-S3R6B
PAL: NLT4532-S4R4

Description of Operation

The CXA3017R incorporates the three functions of an RGB decoder block, an RGB driver block and a timing generator (TG) block onto a single chip using Bi-CMOS technology.

1) RGB decoder block

- Input mode switching
  The input mode (composite input, Y/C input, Y/color difference input) can be switched by the serial bus settings.

  During composite input: The composite signal is input to Pins 57, 59 and 61.
  During Y/C input: The Y signal is input to Pins 59 and 61, and the C signal to Pin 57.
  During Y/color difference input: The Y signal is input to Pins 59 and 61, the B-Y signal to Pin 53, and the R-Y signal to Pin 54.

- System switching
  The input system (NTSC, SPAL, DPAL) can be switched by the serial bus settings. (DPAL uses external delay lines.)

- Trap, BPF
  The center frequency of the built-in trap and BPF can be switched to 3.58MHz during NTSC and 4.43MHz during PAL.
  During composite input, the Y signal enters the trap circuit and the C signal enters the BPF. These signals do not pass through the trap or BPF during Y/C input and Y/color difference input.

- ACC detection, ACC amplifier
  The amplitude of the burst signal output from the ACC amplifier is detected and the ACC amplifier is controlled to maintain the burst signal amplitude at a constant level.

- VXO, APC detection
  The VXO local oscillation circuit is a crystal oscillation circuit. The phases of the input burst signal and the VXO oscillator output are compared in the APC detection block, and the detective output is used to form a PLL that controls the VXO oscillation frequency, which means that the need for adjustments is eliminated.

- External inputs
  These are digital inputs with two thresholds. When one of the RGB inputs is higher than the lower threshold Vth1 (≈ 1.0V), all RGB outputs go to black level. When the higher threshold Vth2 (≈ 2.0V) is exceeded, the output for only the signal in question goes to white level, while the other outputs remain at black level.

2) RGB driver block

• γ correction

In order to support the characteristics of LCD panels, the I/O characteristics are as shown in Fig. 1. The γ gain transition point A voltage changes as shown in Fig. 2 by adjusting the serial bus register γ1, and the transition point B voltage changes as shown in Fig. 3 by adjusting γ2.

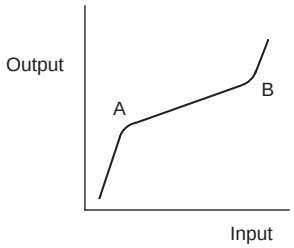


Fig. 1

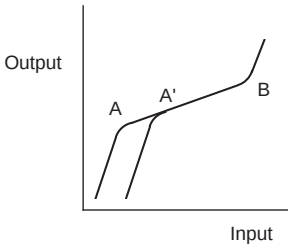


Fig. 2

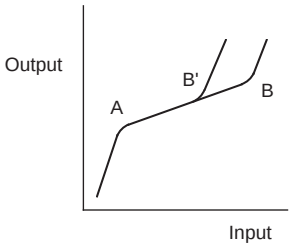
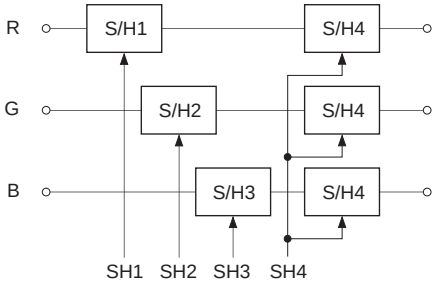
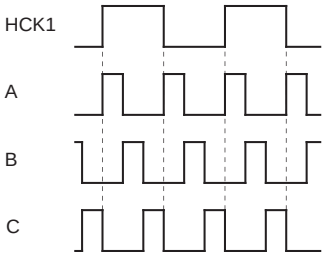


Fig. 3

• Sample-and-hold circuit

As LCD panels sample RGB signals simultaneously, RGB signals output from the CXA3017R must be sampled-and-held in sync with the LCD panel drive pulses.





RGT = H (normal)

	SHS1	SHS2	SHS3
SH1	B	A	C
SH2	Through	Through	Through
SH3	A	C	B
SH4	C	B	A

RGT = L (right/left inversion)

	SHS1	SHS2	SHS3
SH1	B	A	C
SH2	A	C	B
SH3	Through	Through	Through
SH4	C	B	A

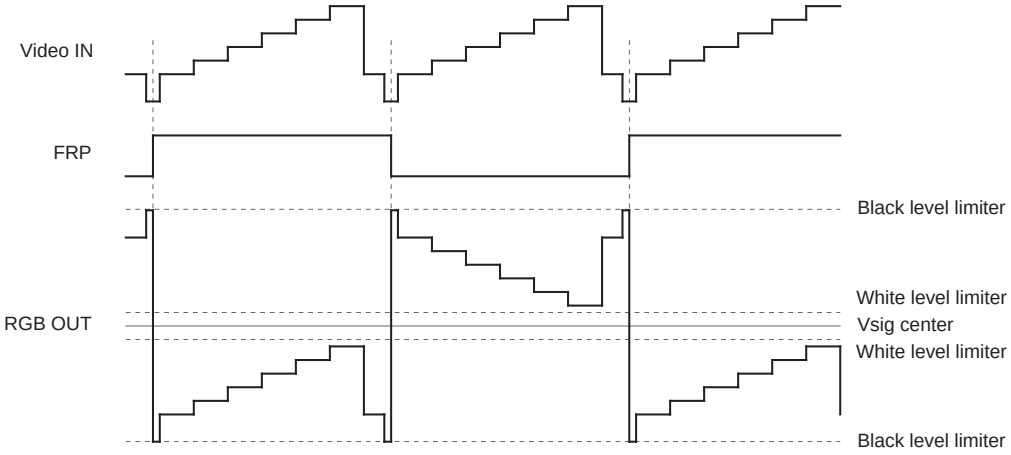
SH1: R signal SH pulse
SH2: G signal SH pulse
SH3: B signal SH pulse
SH4: RGB signal SH pulse

SHS1,2,3: Serial data settings

The sample-and-hold circuit performs sample and hold by receiving the SH1 to SH4 pulses from the TG block. Since LCD panels perform color coding using an RGB delta arrangement, each horizontal line must be compensated by 1.5 dots. This relationship is reversed during right/left inversion. This compensation timing is also generated by the TG block. The sample-and-hold timing changes according to the phase relationship with the HCK1 pulse, so the timing should be set to SHS1, 2 or 3 in accordance with the actual board.

• RGB output

RGB outputs (Pins 40, 43 and 45) are inverted each horizontal line by the FRP pulse (internal pulse) supplied from the TG block as shown in the figure below. Feedback is applied so that the center voltage (Vsig center) of the output signal matches the reference voltage ($V_{CC}2$ + GND2)/2 (or the voltage input to SIG CENTER (Pin 48)). In addition, the white level output is clipped at the limiter operation point that is set by the serial bus register WHITE LIM, and the black level output is clipped at the limiter operation point that is set by the serial bus register BLKLIM.



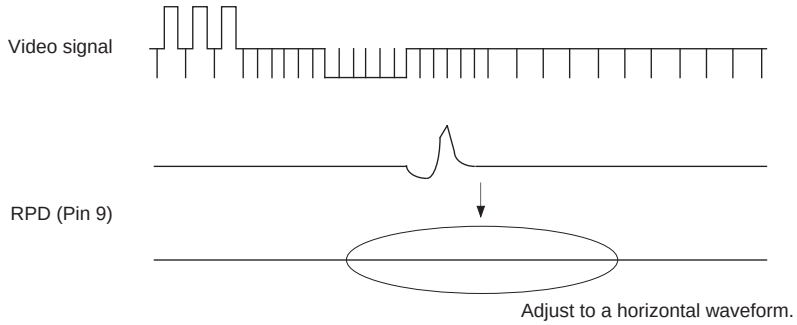
3) TG block

• PLL and AFC circuits

The TG block contains a PLL circuit phase comparator and frequency division counter and a VCO circuit, and comprises a PLL circuit.

The PLL error detection signal is generated by the HSYNC block, and the integral value of the phase comparison output of the entire bottom of HSYNC and the internal frequency division counter becomes RPD (Pin 9).

The CXA3017R controls the internal VCO with the RPD output to stabilize the oscillation frequency at 690f_H (NTSC) or 716f_H (PAL) for the LCX005BK/BKB and LCX024AK/AKB, and 1034f_H (NTSC) or 1072f_H (PAL) for the LCX009AK/AKB, LCX027AK/AKB and DCX501BK. The PLL of this system is adjusted by adjusting the serial bus register VCO so that the RPD output waveform is constant near VSYNC as shown in the figure



Horizontal AFC adjustment

• H position

The horizontal display position can be set at 2f_H intervals in 32 different ways by the serial bus settings. Note that the delay difference between the RGB signal and the drive pulse differs according to the board, so adjust the serial bus register H position so that the picture center matches the center of the LCD panel.

• Right/left inversion

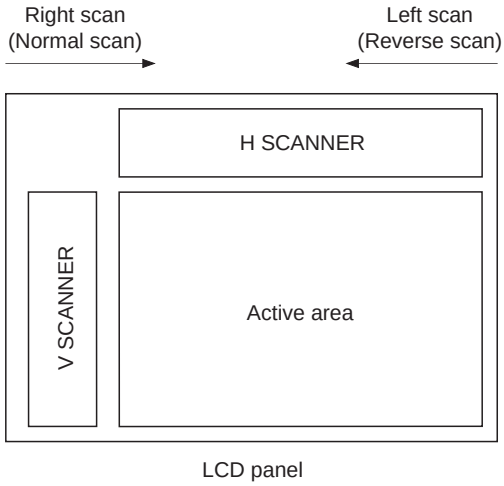
The LCD panel is arranged in a delta arrangement, where identical signal lines are offset by 1.5 dots from adjoining lines. For this reason, a 1.5-bit offset is attached to the horizontal start pulse (HST) between odd lines and even lines. HCK and S/H are also 1.5-bit offset. Therefore, when the panel is driven by left scan (Reverse scan), this offset relationship is inverted for even and odd lines.

Moreover, since the dot arrangement is asymmetrical, the HST position is also changed.

RGT = H: Right scan mode

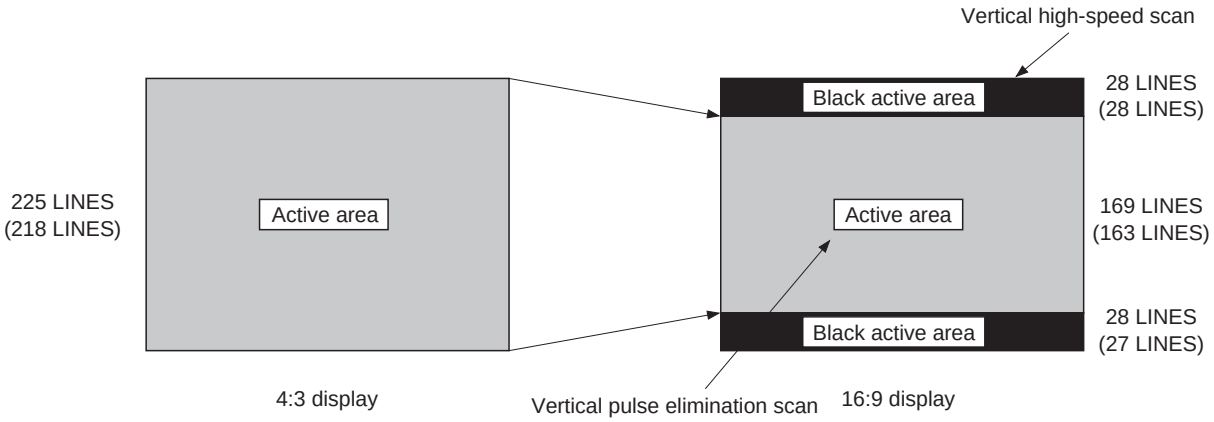
RGT = L: Left scan mode

(H and L are the LCD panel input levels.)



• Wide mode

Wide mode can be selected by setting wide mode with the serial bus aspect switching register. In this mode, aspect ratio conversion is performed by pulse elimination processing to enable 16:9 quasi-WIDE display. Vertical pulse elimination scanning of 1/4 for NTSC and 10/28 for PAL is performed and the video signal is compressed in order to achieve a 16:9 aspect ratio during the wide mode period. In addition, high-speed scan is performed in areas outside of the active area to display black in the upper 28 lines and the lower 28 (27) lines. Black display is performed by limiting the video signal input during the V blanking period and writing a black level signal in its place.



Numbers inside parentheses are for the LCX005BK/BKB and LCX024AK/AKB; other numbers are for the LCX009AK/AKB, LCX027AK/AKB and DCX501BK.

- AC driving of LCD panels during no signal

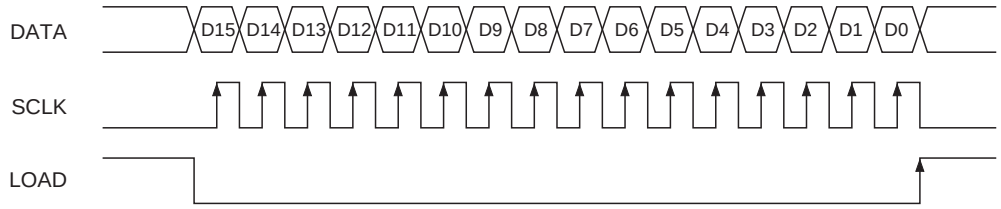
  HST, XHST, HCK1, HCK2, VST, XVST, VCK1, VCK2, PCG, XPCG, EN, XEN, HD, VD, and FRP (internal pulse) are made to run freely so that the LCD panel is AC driven even when there is no composite sync from the SYNCIN pin.

  During this time, the HSYNC separation circuit stops and the PLL counter is made to run freely. In addition, the VSYNC separation circuit is also stopped, so the auxiliary V counter is used to create the reference pulse for generating VD, VST and XVST. The cycle of this V counter is designed to be 525/2H for NTSC and 625/2H for PAL. However, when there is no vertical sync signal for 5 fields, the no signal state is assumed and the free running VD, VST and XVST pulses are generated from the next field. In addition, RPD is kept at high impedance when there is no signal in order to prevent the AFC circuit from causing errors due to phase comparison.

Description of Serial Control Operation

1) Control method

Control data consists of 16 bits of data which is loaded one bit at a time at the rising edge of SCLK. This loading operation starts from the falling edge of LOAD and is completed at the next rising edge.
Digital block control data is established by the vertical sync signal, so if data is transferred multiple times for the same item, the data immediately before the vertical sync signal is valid. Analog (electronic attenuator) block control data becomes valid each time the LOAD signal is input.



Serial transfer timing

2) Serial data map

The serial data map is as follows.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	S/H phase		Aspect	External VSYNC	System		Input switching	
0	0	0	0	0	0	0	1	0	0	Panel 2	TEST1	Supported panels			
0	0	0	0	0	0	1	0	DWN	RGT2	RGT1	SYNC GEN	TEST2	Y/color difference clamp	VD polarity	HD polarity
0	0	0	0	0	0	1	1	0	TEST5	FRP inversion	P-FRP inversion stop	FRP inversion stop	FRP4096 inversion	TEST4	TEST3
0	0	0	0	0	1	0	0	PLL adjust-ment 2	PLL adjust-ment 1	0	0	0	POWER SAVE	0	SYNC detection
0	0	0	0	0	1	0	1	*	*	*	H-POSITION				
0	0	0	0	0	1	1	0	*	*	*	HD-POSITION				
1	0	0	0	0	0	0	0	HUE							
1	0	0	0	0	0	0	1	COLOR							
1	0	0	0	0	0	1	0	BRIGHT							
1	0	0	0	0	0	1	1	CONTRAST							
1	0	0	0	0	1	0	0	R-BRIGHT							
1	0	0	0	0	1	0	1	B-BRIGHT							
1	0	0	0	0	1	1	0	γ-1							
1	0	0	0	0	1	1	1	γ-2							

*: don't care

Serial data map (cont.)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	0	PSIG-BRIGHT							
1	0	0	0	1	0	0	1	R-CONTRAST							
1	0	0	0	1	0	1	0	B-CONTRAST							
1	0	0	0	1	0	1	1	BLK LIM							
1	0	0	0	1	1	0	0	PICTURE							
1	0	0	0	1	1	0	1	USER-BRIGHT							
1	0	0	0	1	1	1	0	VCO							
1	0	0	0	1	1	1	1	*	*	*	*	*	*	WHITE LIM	
1	0	0	1	0	0	0	0	*	*	*	*	*	DA OUT		
1	1	1	0	0	0	0	0	TEST6							

*: don't care

3) Serial data mode settings (X: don't care)

- Input switching

  This switches the input signal format.

D1	D0	
0	X	Composite input (default)
1	0	Y/C input
1	1	Y/color difference input

- System switching

  This switches the input video signal system.

D3	D2	
0	0	NTSC (default)
0	1	TEST
1	0	D-PAL
1	1	S-PAL

- External VSYNC

  Internal VSYNC separation is not performed and an externally input VSYNC is used.

D4	
0	OFF (internal separation) (default)
1	ON (external input)

- Aspect switching

  This switches the video display aspect.

D5	
0	4:3 (normal) (default)
1	16:9 (letterbox, pulse elimination display)

• Sample-and-hold phase
This switches the sample-and-hold timing.

D7	D6	
0	0	SHS1 (default)
0	1	SHS2
1	0	SHS3
1	1	Through (sample-and-hold not performed)

• Supported panels
This switches the supported panels.

D3	D2	D1	D0	Supported panels
0	0	0	0	LCX005BK/BKB single
0	0	0	1	LCX024AK/AKB single
0	0	1	0	LCX009AK/AKB single
0	0	1	1	LCX027AK/AKB single
0	1	0	0	LCX005BK/BKB + (DCX501BK)
0	1	0	1	LCX024AK/AKB + (DCX501BK) (default)
0	1	1	0	LCX009AK/AKB + (DCX501BK)
0	1	1	1	LCX027AK/AKB + (DCX501BK)
1	0	0	0	—
1	0	0	1	DCX501BK single
1	0	1	0	—
1	0	1	1	—
1	1	0	0	DCX501BK + (LCX005BK/BKB)
1	1	0	1	DCX501BK + (LCX024AK/AKB)
1	1	1	0	DCX501BK + (LCX009AK/AKB)
1	1	1	1	DCX501BK + (LCX027AK/AKB)

Two-panel simultaneous drive mode

The supported panels are the main panel and the sub panel (the panel noted inside the parentheses).
The video is not displayed correctly on the sub panel for combinations of the LCX005BK (BKB)/024AK (AKB) and the DCX501BK. Therefore, the sub panel back light should be turned off.
Two-panel simultaneous display is possible with combinations of the LCX009AK (AKB)/027AK (AKB) and the DCX501BK (only when RGT1 = RGT2). However, when the right/left inversion directions of the main and sub panels differ (RGT1 ≠ RGT2), the picture is not displayed correctly due to the line offset. Therefore, use Panel 2 mode in these cases.

• TEST1
This is the test mode. Set to normal mode.

D4	
0	Normal mode (default)
1	TEST mode

• Panel 2
Set this when the right/left inversion direction of the two panels differs (RGT1 ≠ RGT2) during two-panel simultaneous drive using the LCX009AK (AKB)/027AK (AKB)and the DCX501BK.

D5	
0	OFF (default)
1	ON

Notes) 1. The VST connection changes in this mode, so an external inverter is required.
2. Set sample and hold to OFF (through) in this mode.
3. When the right/left inversion direction of the two panels differs (RGT1 ≠ RGT2), the video display start position of the sub panel is advanced by 1H.
4. RGT1 and RGT2 can also be set the same in this mode.

• HD polarity
This switches the HD output (Pin 21) polarity.

D0	
0	Positive polarity (default)
1	Negative polarity

• VD polarity
This switches the VD output (Pin 31) polarity.

D1	
0	Positive polarity (default)
1	Negative polarity

• Y/color difference clamp
This switches the position at which the R-Y and B-Y input signals are clamped during Y/color difference input mode.

D2	
0	Pedestal position (default)
1	SYNC position

• TEST2
This is the test mode. Set to normal mode.

D3	
0	Normal mode (default)
1	TEST mode

• SYNC GEN
This sets the sync generator function. Outputs other than VD and HD of the TG block are stopped.

D4	
0	OFF (default)
1	ON

• RGT1 (right/left inversion 1)
This switches the DCX501BK right/left inverted display timing and the RGT1 output (Pin 34).

D5	
0	OFF (normal display) (default)
1	ON (right/left inverted display)

• RGT2 (right/left inversion 2)
This switches the LCX005BK (BKB)/009AK (AKB)/024AK (AKB)/027AK (AKB)right/left inverted display timing.

D6	
0	OFF (normal display) (default)
1	ON (right/left inverted display)

• DWN (up/down inversion)
This switches the DCX501BK up/down inverted display timing and the DWN output (Pin 35).

D7	
0	OFF (normal display) (default)

• TEST3
This is the test mode. Set to normal mode.

D0

0	Normal mode (default)
1	TEST mode

• TEST4
This is the test mode. Set to normal mode.

D1

0	Normal mode (default)
1	TEST mode

• FRP4096 inversion
This further inverts the polarity of the RGB output that is inverted every 1H for 4096 fields.

D2

0	OFF (default)
1	ON

• FRP inversion stop
This stops R, G and B output polarity inversion.

D3

0	OFF (1H inversion) (default)
1	ON (polarity not inverted)

• P-FRP inversion stop
This stops PSIG output polarity inversion.

D4

0	OFF (1H inversion) (default)
1	ON (polarity not inverted)

• FRP inversion
This switches the FRP output inversion cycle.

D5

0	1H inversion (default)
1	1 field inversion

• TEST5
This is the test mode. Set to normal mode.

D6

0	Normal mode (default)
1	TEST mode

• Sync detection
This prevents (as much as possible) the vertical sync from being lost during weak magnetic field signal input. Set to ON (0).

D0

0	ON (default)
1	OFF

• POWER SAVE

This stops HST1/XHST1 in order to reduce the DCX501BK current consumption.
Set to OFF (0).

D2	
0	OFF (default)
1	ON (HST1/XHST1 stopped)

• PLL adjustment 1, 2

These set the PLL adjustment.

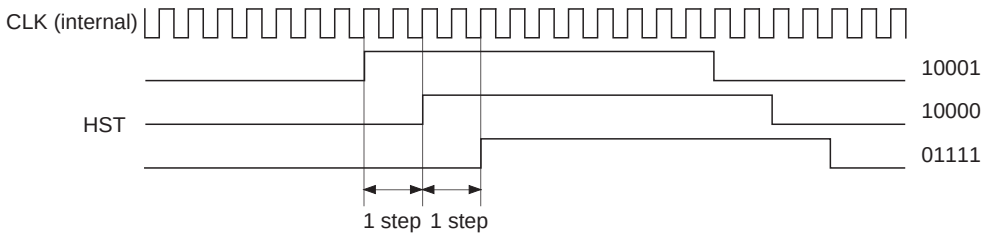
D7	D6	
0	0	(default)
0	1	Set D7 = 0, D6 = 1.
1	0	
1	1	

• H position setting

This sets the horizontal display start position. (2f_H intervals in 32 different ways)

D4	D3	D2	D1	D0	
0	0	0	0	0	
:	:	:	:	:	
1	0	0	0	0	(default)
:	:	:	:	:	
1	1	1	1	1	

Variable in 2f_H (= 1 bit) increments

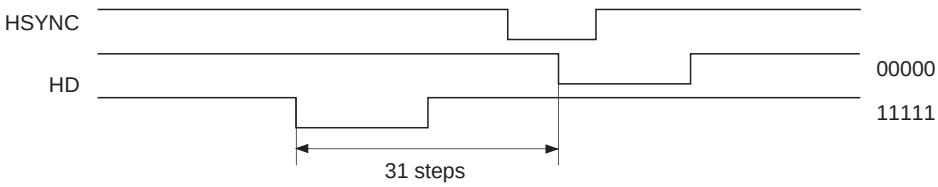


• HD phase setting

This sets the HD output (Pin 21) phase. (4f_H intervals in 32 different ways)

D4	D3	D2	D1	D0	
0	0	0	0	0	(default)
:	:	:	:	:	
1	1	1	1	1	

Variable in 4f_H (= 1 bit) increments



4) Serial data electronic attenuator (D/A converter) settings

	D7	D6	D5	D4	D3	D2	D1	D0	
• HUE	1	0	0	0	0	0	0	0	(default)
• COLOR	1	0	0	0	0	0	0	0	(default)
• BRIGHT	1	0	0	0	0	0	0	0	(default)
• CONTRAST	1	0	0	0	0	0	0	0	(default)
• R-BRT	1	0	0	0	0	0	0	0	(default)
• B-BRT	1	0	0	0	0	0	0	0	(default)
• γ-1	0	0	0	0	0	0	0	0	(default)
• γ-2	0	0	0	0	0	0	0	0	(default)
• PSIG-BRT	1	0	0	0	0	0	0	0	(default)
• R-CONT	1	0	0	0	0	0	0	0	(default)
• B-CONT	1	0	0	0	0	0	0	0	(default)
• BLK LIM	1	0	0	0	0	0	0	0	(default)
• PICTURE	1	0	0	0	0	0	0	0	(default)
• USER-BRIGHT	1	0	0	0	0	0	0	0	(default)
• VCO	1	0	0	0	0	0	0	0	(default)
• WHITE LIM	—	—	—	—	—	—	0	1	(default)

5) DA OUT

This controls the DC level (0 to 3V, 8 steps) of the DA OUT (Pin 32) DAC output.

	D7	D6	D5	D4	D3	D2	D1	D0	
DA OUT	—	—	—	—	—	0	0	0	(default)

6) TEST6

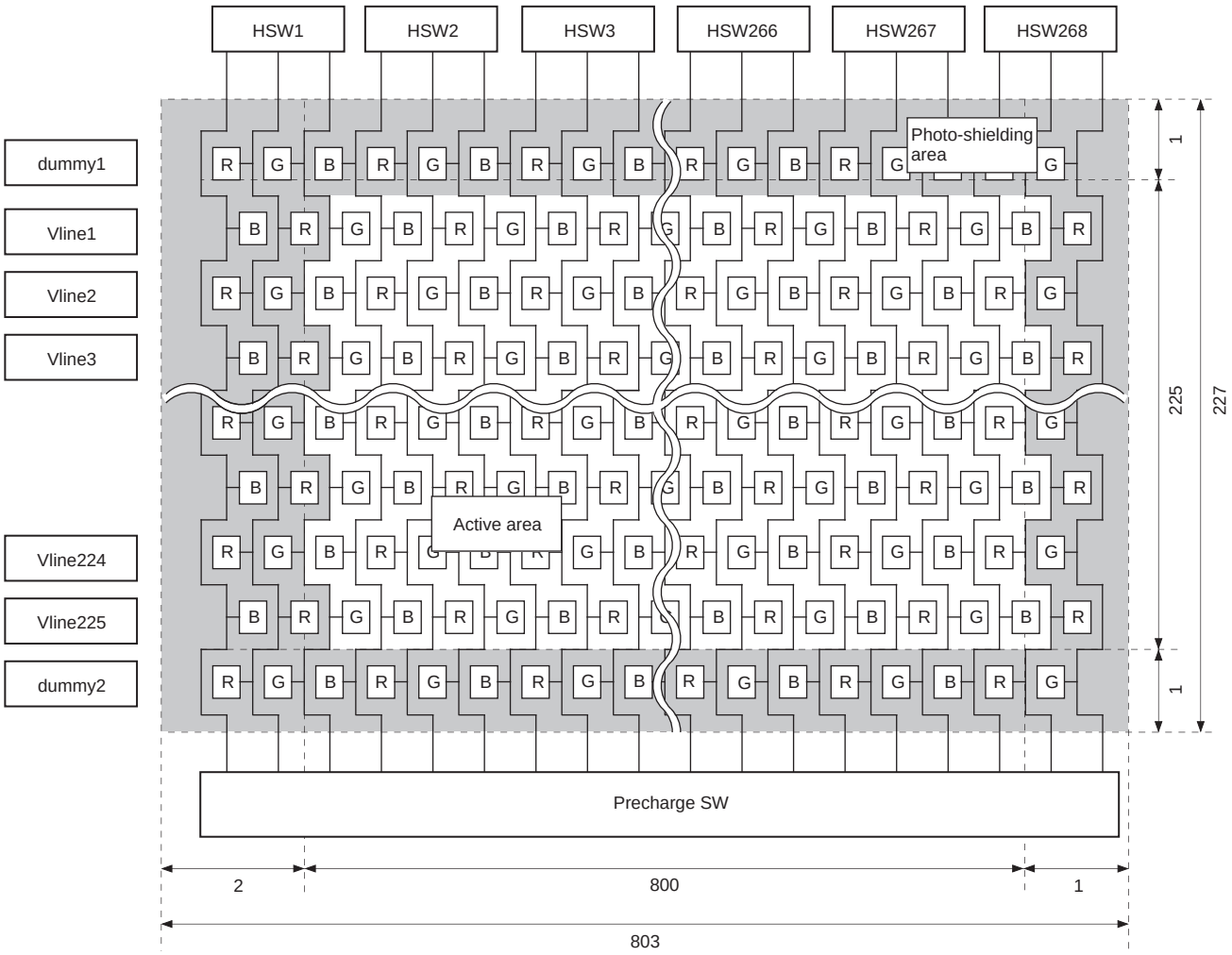
TEST6 is a test mode which results automatically if data is sent to these addresses, regardless of the data contents. For this reason, do not perform data transfer using these addresses.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	0	0	0	0	X	X	X	X	X	X	X	X

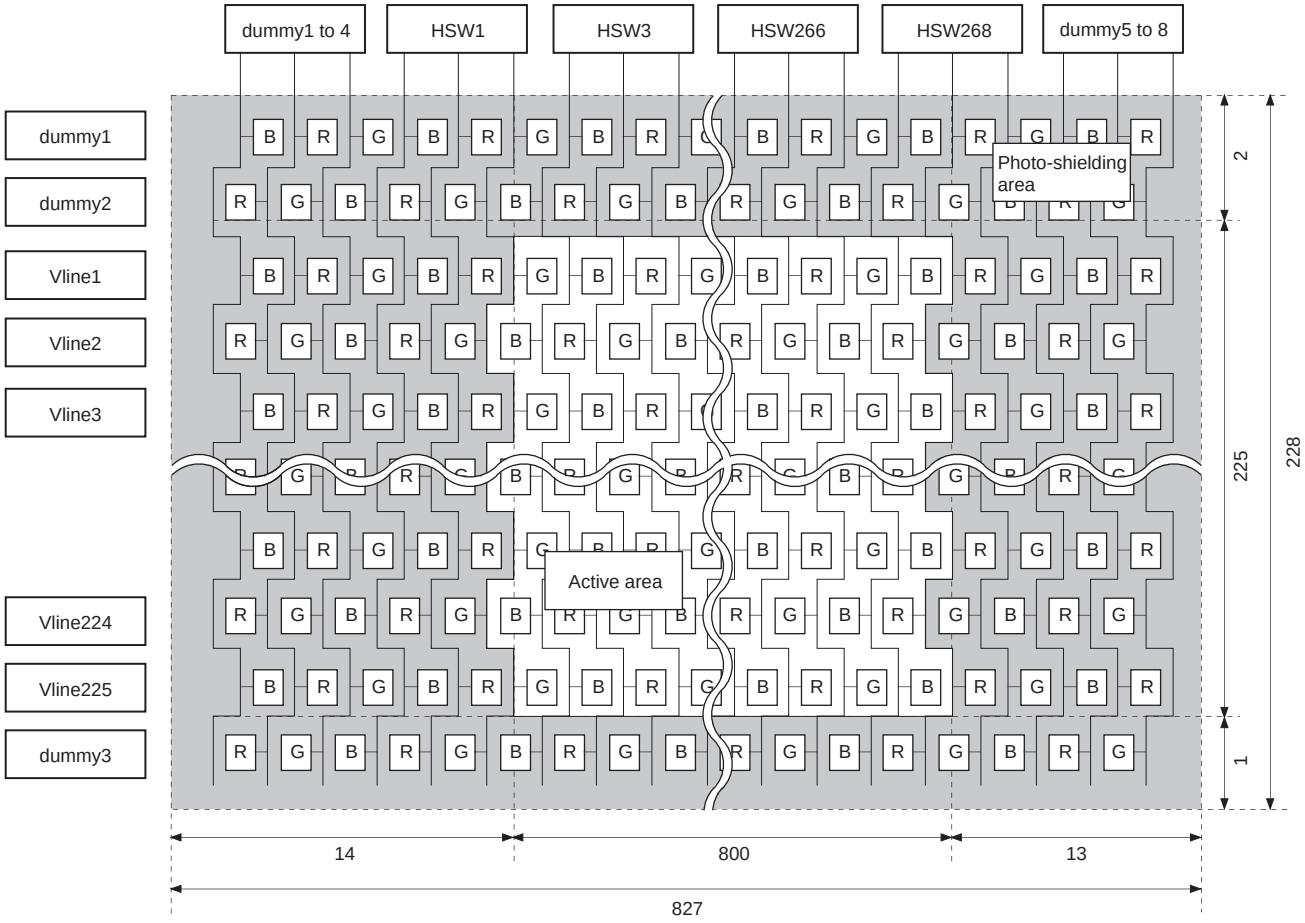
DCX501BK Color Coding Diagram

The CXA3017R supports LCD panels which perform color coding in a delta arrangement.
The shaded areas in the figure are not displayed.

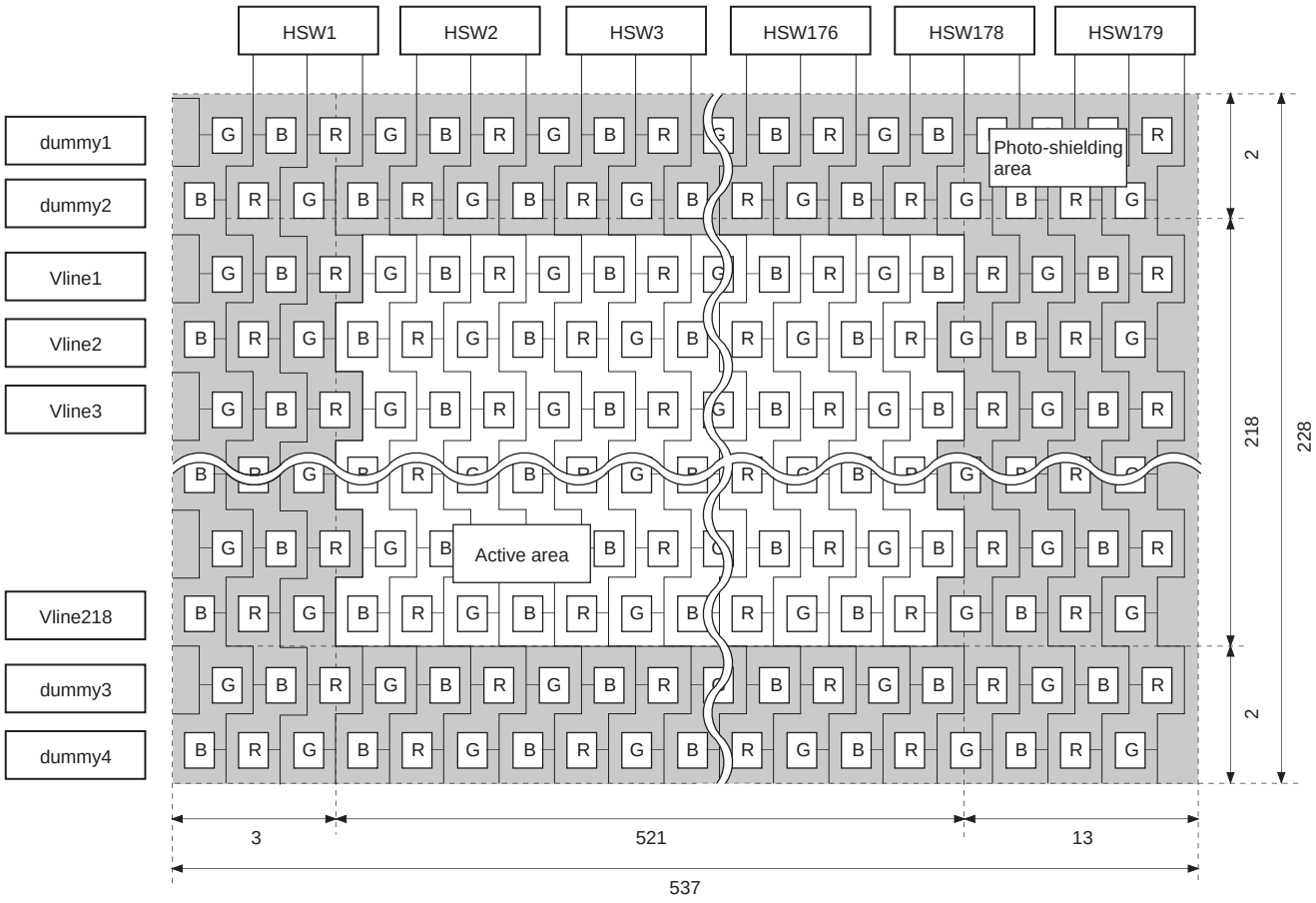
DCX501BK Pixel Arrangement



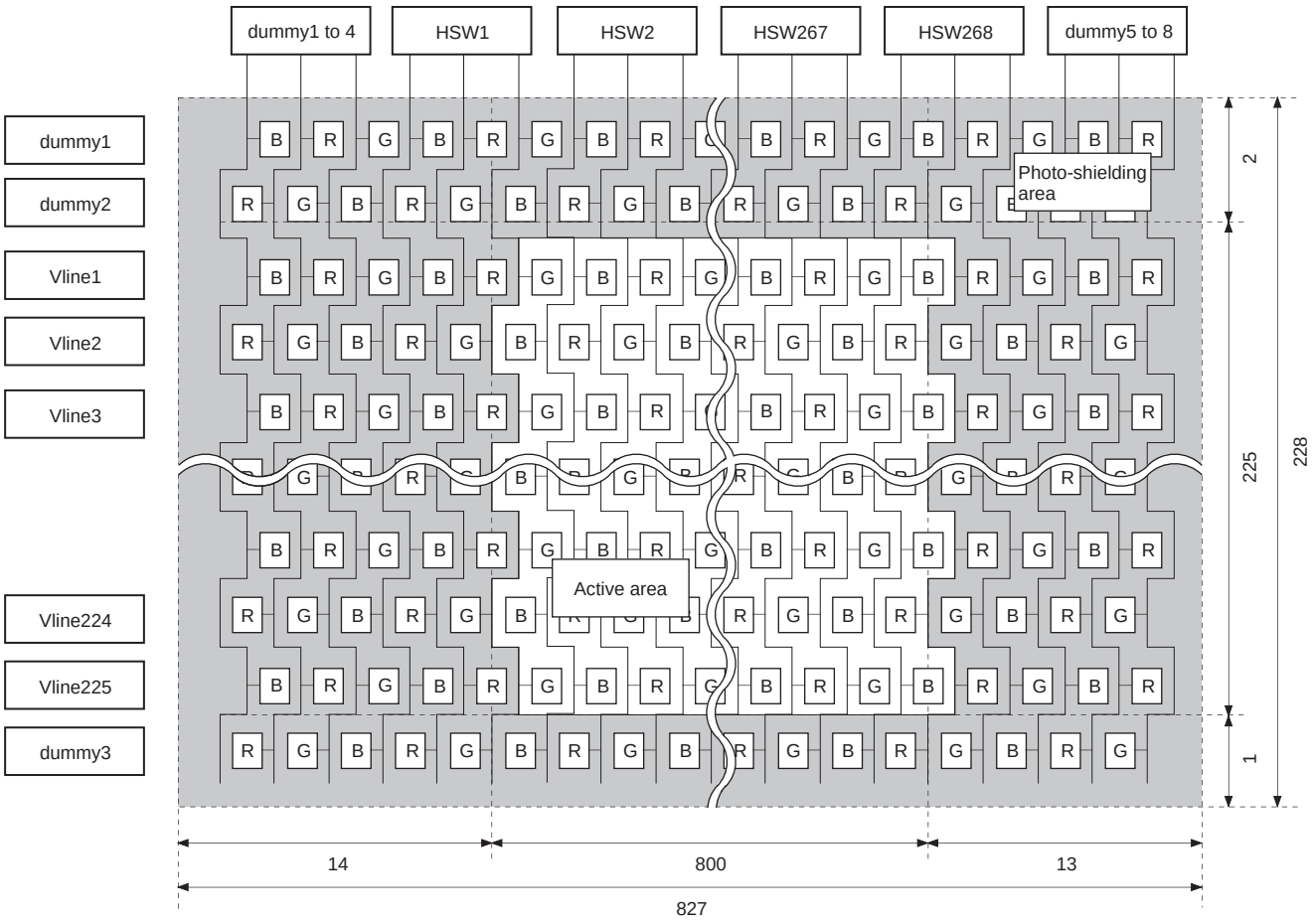
LCX027AK/AKB Pixel Arrangement



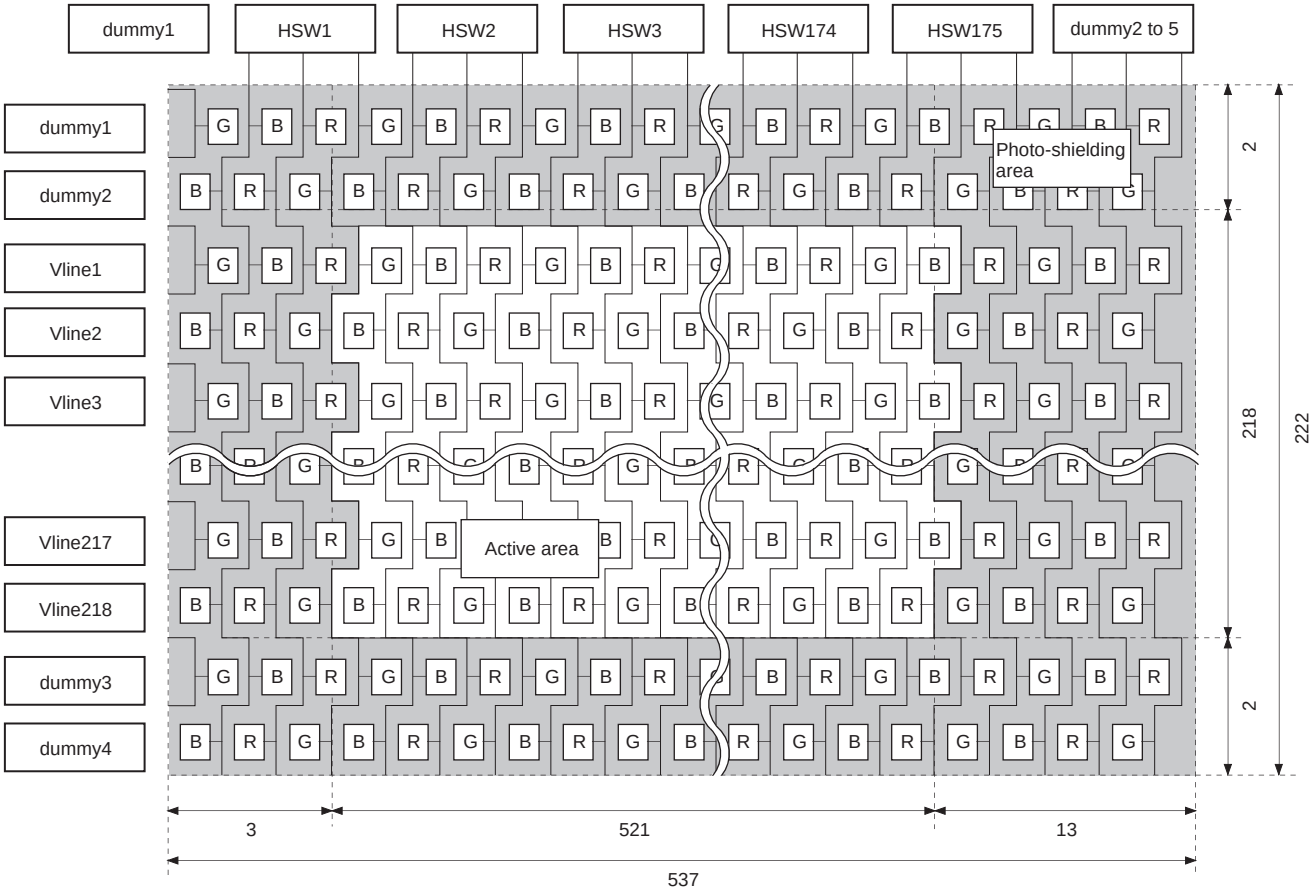
LCX024AK/AKB Pixel Arrangement



LCX009AK/AKB Pixel Arrangement

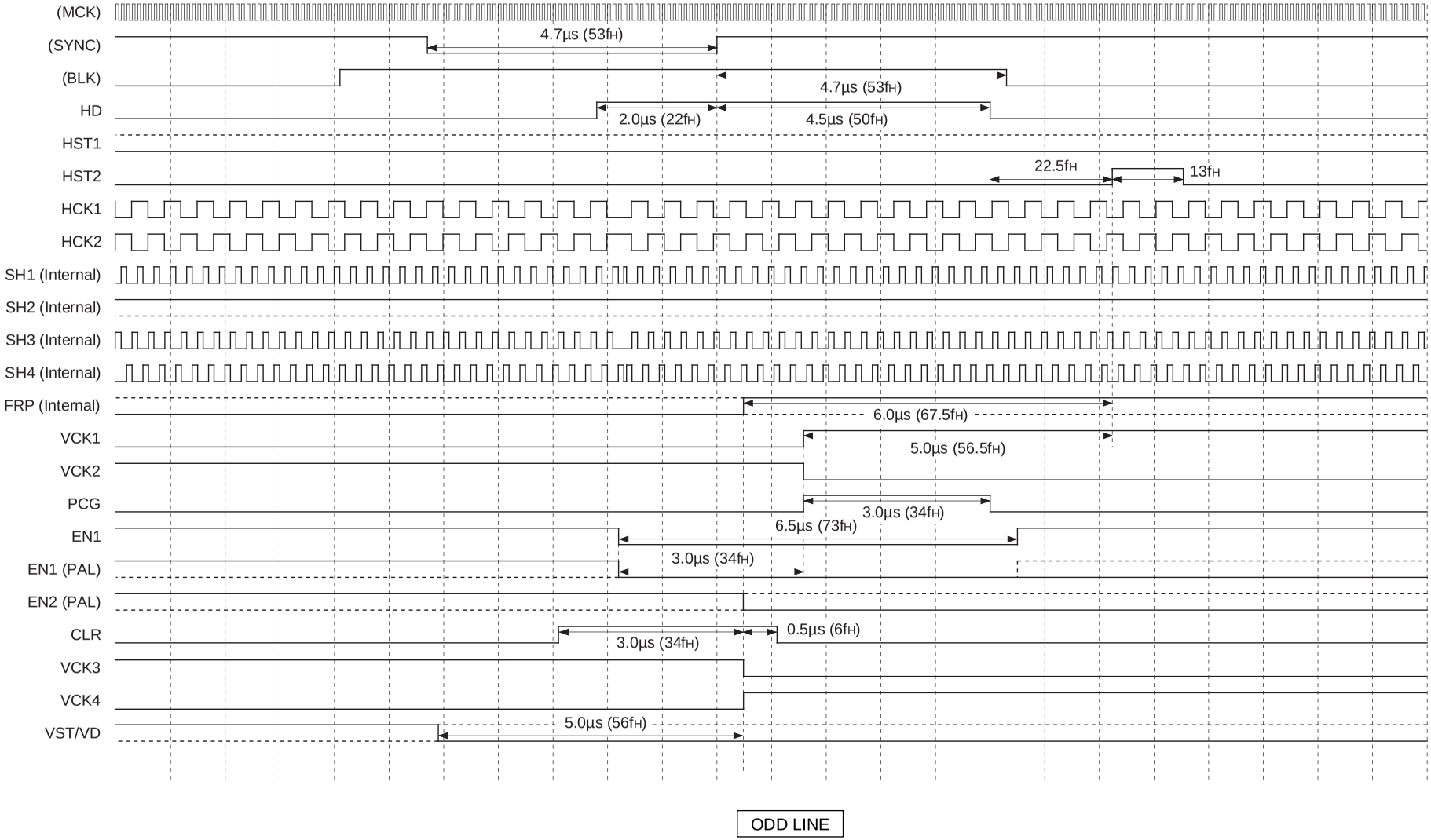


LCX005BK/BKB Pixel Arrangement



Horizontal Direction Timing Chart — NTSC/PAL
LCX005 + (DCX501), LCX024 + (DCX501)

RGT1 = 0, RGT2 = 0, HP = 10000, HD = 00000
Cycle value NTSC: 690 ck, PAL: 716 ck

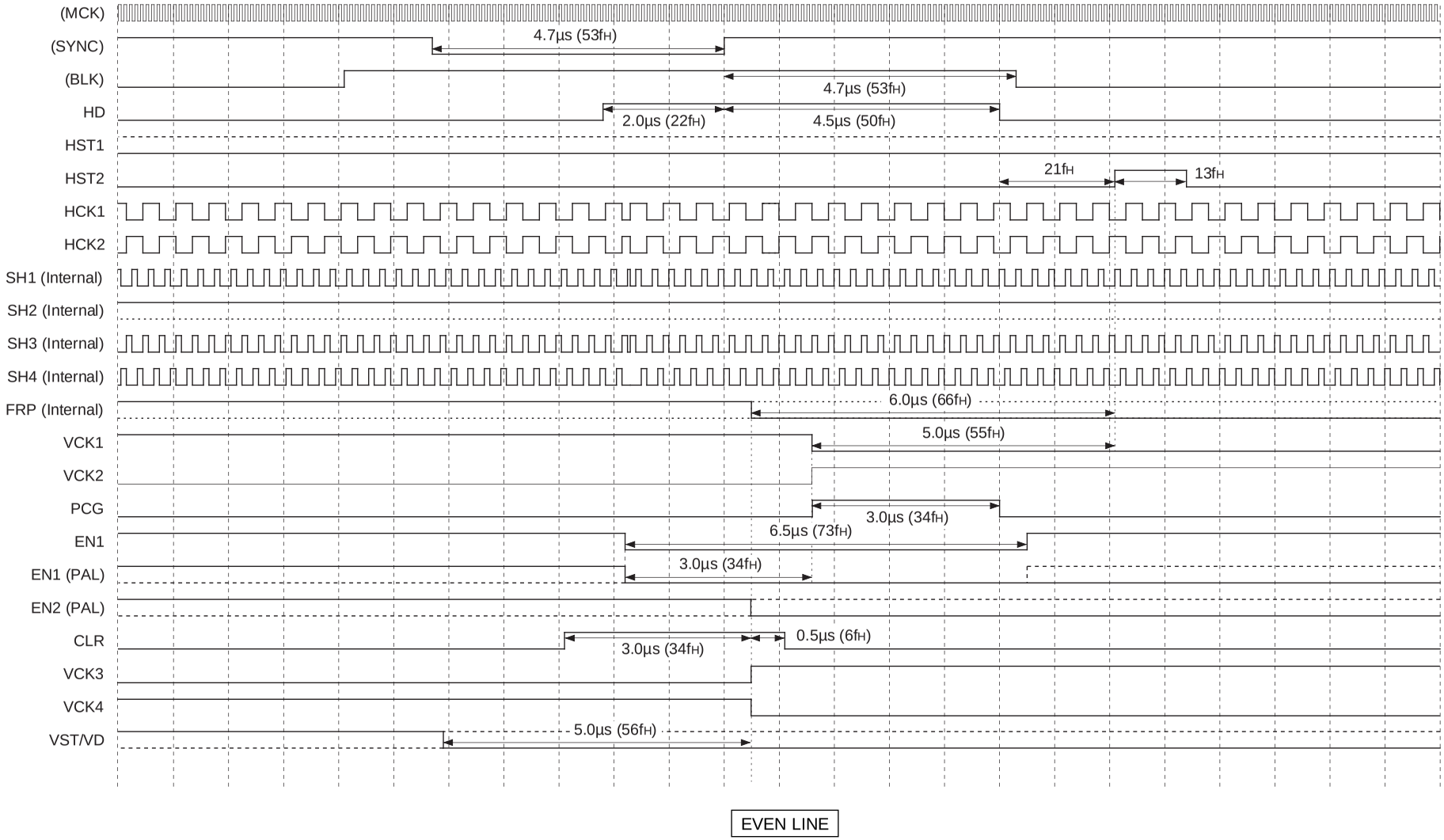


ODD LINE

Note) The first (MCK), second (SYNC) and third (BLK) rows of the timing chart are pulses indicated as a reference and are not pulses output from pins.
FRP polarity is not specified for each line and field.
LCX005/024 drive pulses: HST2, HCK1, HCK2, EN2, CLR, VCK3, VCK4, VST(EN2 is high during NTSC.)
DCX501 drive pulses: HST1, HCK1, HCK2, VCK1, VCK2, PCG, EN1 and VST (HST1, PCG, EN1 and VST output inverted pulses XHST1, XPCG, XEN1 and XVST.)

Horizontal Direction Timing Chart — NTSC/PAL
LCX005 + (DCX501), LCX024 + (DCX501)

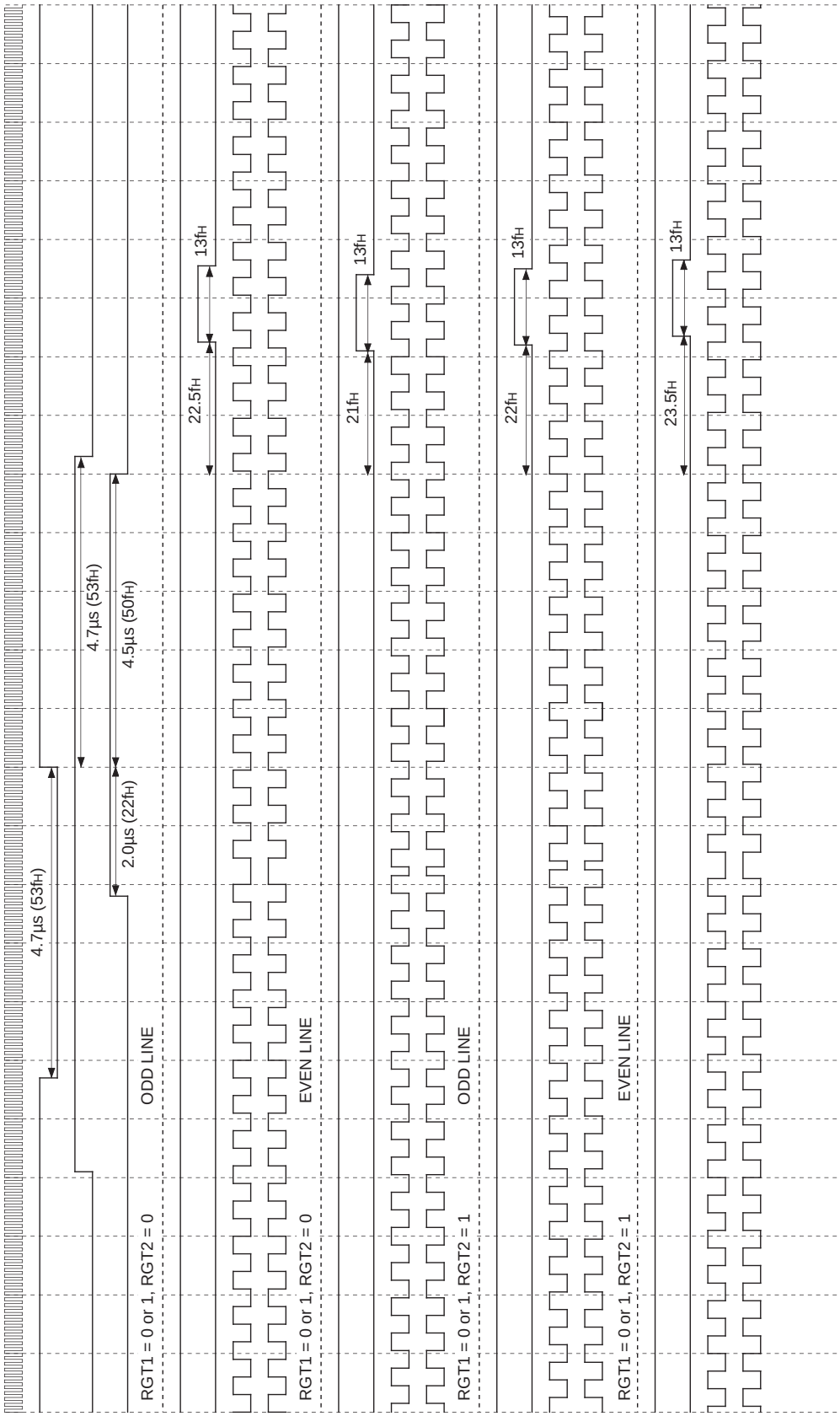
RGT1 = 0, RGT2 = 0, HP = 10000, HD = 00000
Cycle value NTSC: 690 ck, PAL: 716 ck



Note) The first (MCK), second (SYNC) and third (BLK) rows of the timing chart are pulses indicated as a reference and are not pulses output from pins.
FRP polarity is not specified for each line and field.
LCX005/024 drive pulses: HST2, HCK1, HCK2, EN2, CLR, VCK3, VCK4 and VST (EN2 is high during NTSC.)
DCX501 drive pulses: HST1, HCK1, HCK2, VCK1, VCK2, PCG, EN1 and VST (HST1, PCG, EN1 and VST output inverted pulses XHST1, XPCG, XEN1 and XVST.)

Horizontal Direction Timing Chart — NTSC/PAL
LCX005 + (DCX501), LCX024 + (DCX501)

HST1 and HST2 during right/left inversion



Note) The first (MCK), second (SYNC) and third (BLK) rows of the timing chart are pulses indicated as a reference and are not pulses output from pins.

HST1: DCX501 horizontal display start pulse (inverted pulse XHST1 output)

HST2: LCX005/024 horizontal display start pulse

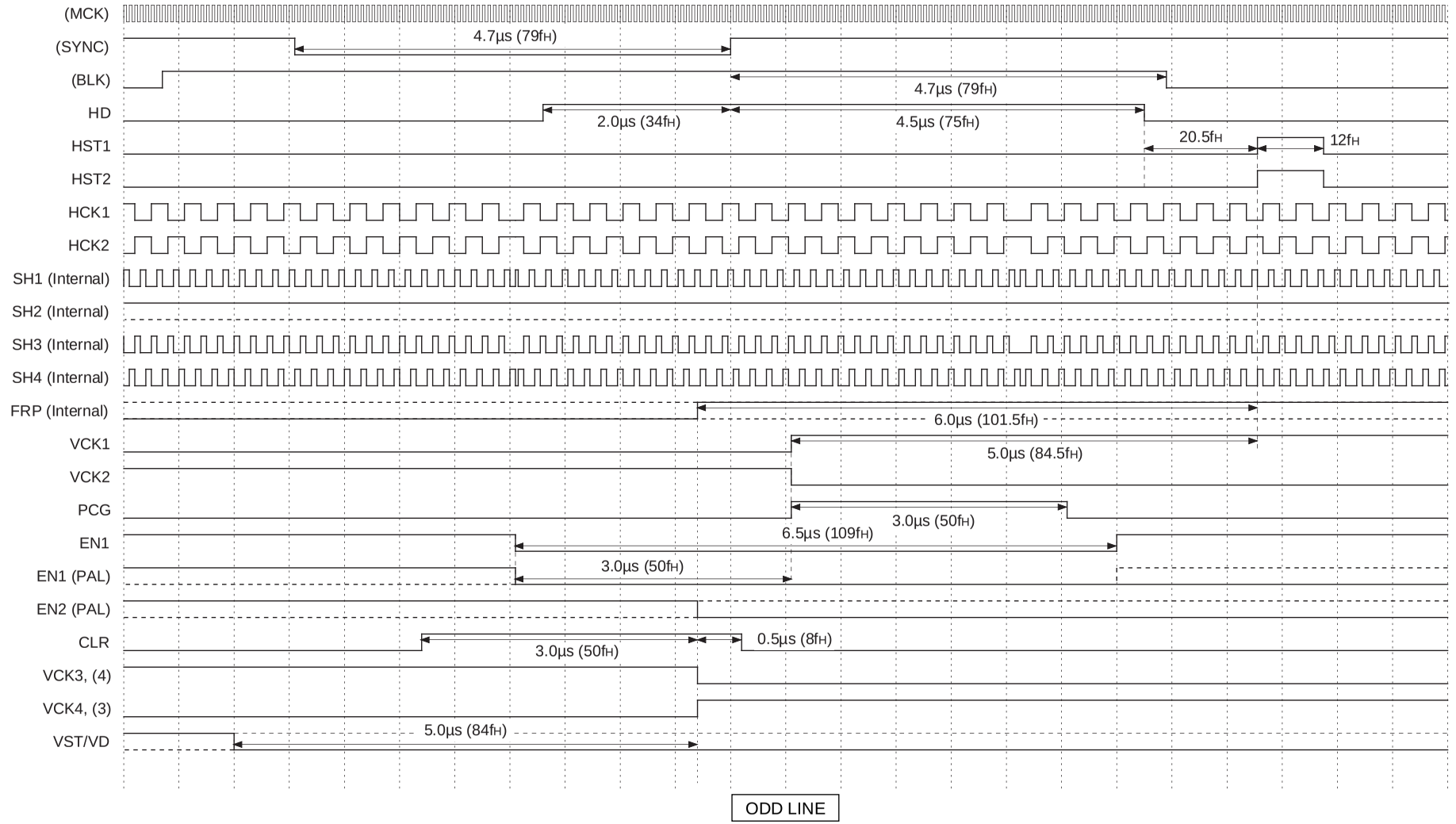
Horizontal Direction Timing Chart — NTSC/PAL

LCX009 + (DCX501), LCX027 + (DCX501)

DCX501 + (LCX009), DCX501 + (LCX027), DCX501 + (LCX005), DCX501 + (LCX024)

RGT1 = 0, RGT2 = 0, HP = 10000, HD = 00000

Cycle value NTSC: 1034 ck, PAL: 1072 ck



Note) The first (MCK), second (SYNC) and third (BLK) rows of the timing chart are pulses indicated as a reference and are not pulses output from pins.

FRP polarity is not specified for each line and field.

In LCX009 + (DCX501) and DCX501 + (LCX009) modes, the VCK3 and VCK4 polarities are inverted. (VCK(3) and VCK(4))

LCX009/027, 005/024 drive pulses: HST2, HCK1, HCK2, EN2, CLR, VCK3, VCK4 and VST (EN2 is high during NTSC.)

DCX501 drive pulses: HST1, HCK1, HCK2, VCK1, VCK2, PCG, EN1 and VST (HST1, PCG, EN1 and VST output inverted pulses XHST1, XPCG, XEN1 and XVST.)

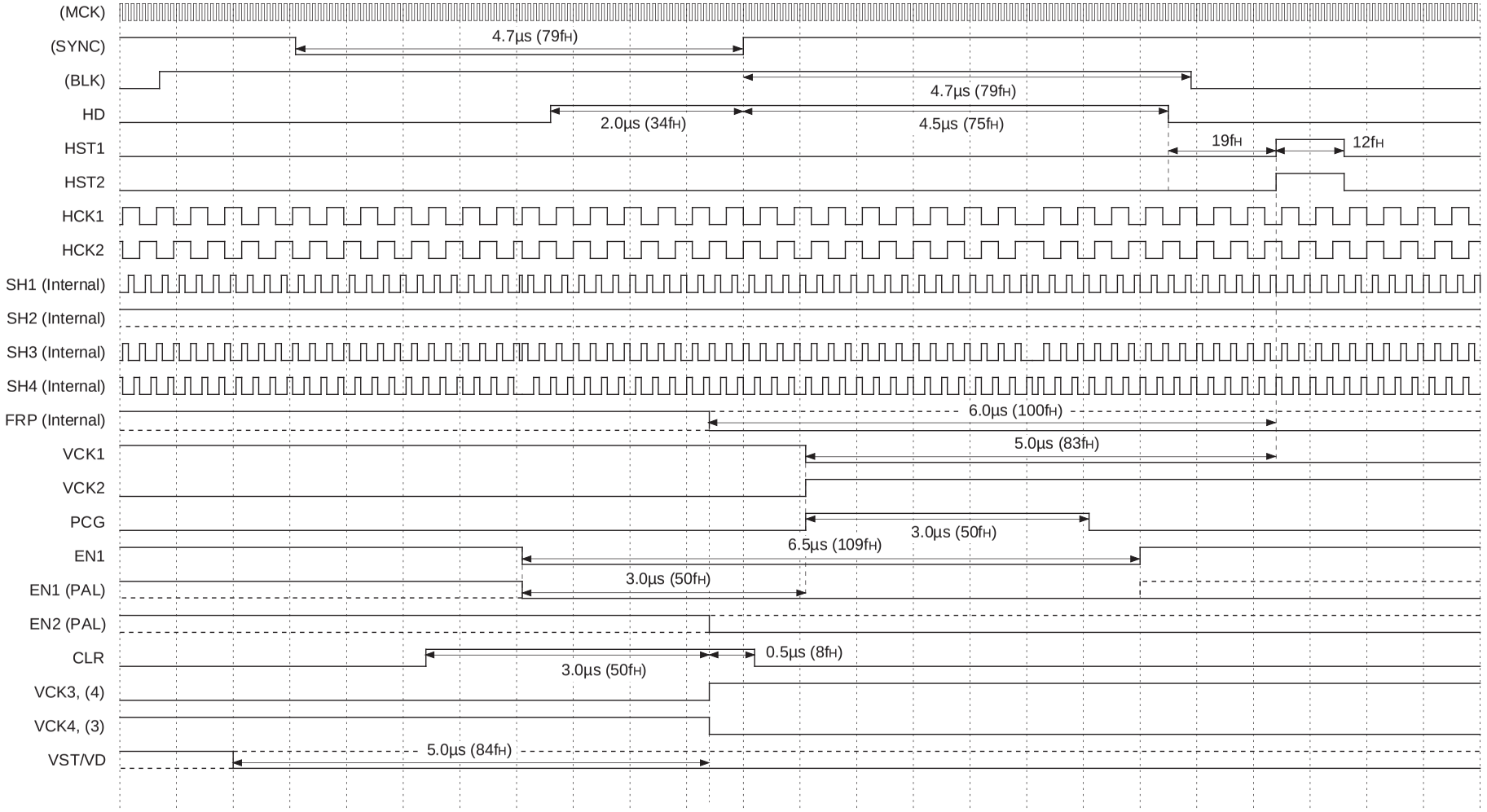
Horizontal Direction Timing Chart — NTSC/PAL

LCX009 + (DCX501), LCX027 + (DCX501)

DCX501 + (LCX009), DCX501 + (LCX027), DCX501 + (LCX005), DCX501 + (LCX024)

RGT1 = 0, RGT2 = 0, HP = 10000, HD = 00000

Cycle value NTSC: 1034 ck, PAL: 1072 ck



Note) The first (MCK), second (SYNC) and third (BLK) rows of the timing chart are pulses indicated as a reference and are not pulses output from pins.

FRP polarity is not specified for each line and field.

In LCX009 + (DCX501) and DCX501 + (LCX009) modes, the VCK3 and VCK4 polarities are inverted. (VCK(3) and VCK(4))

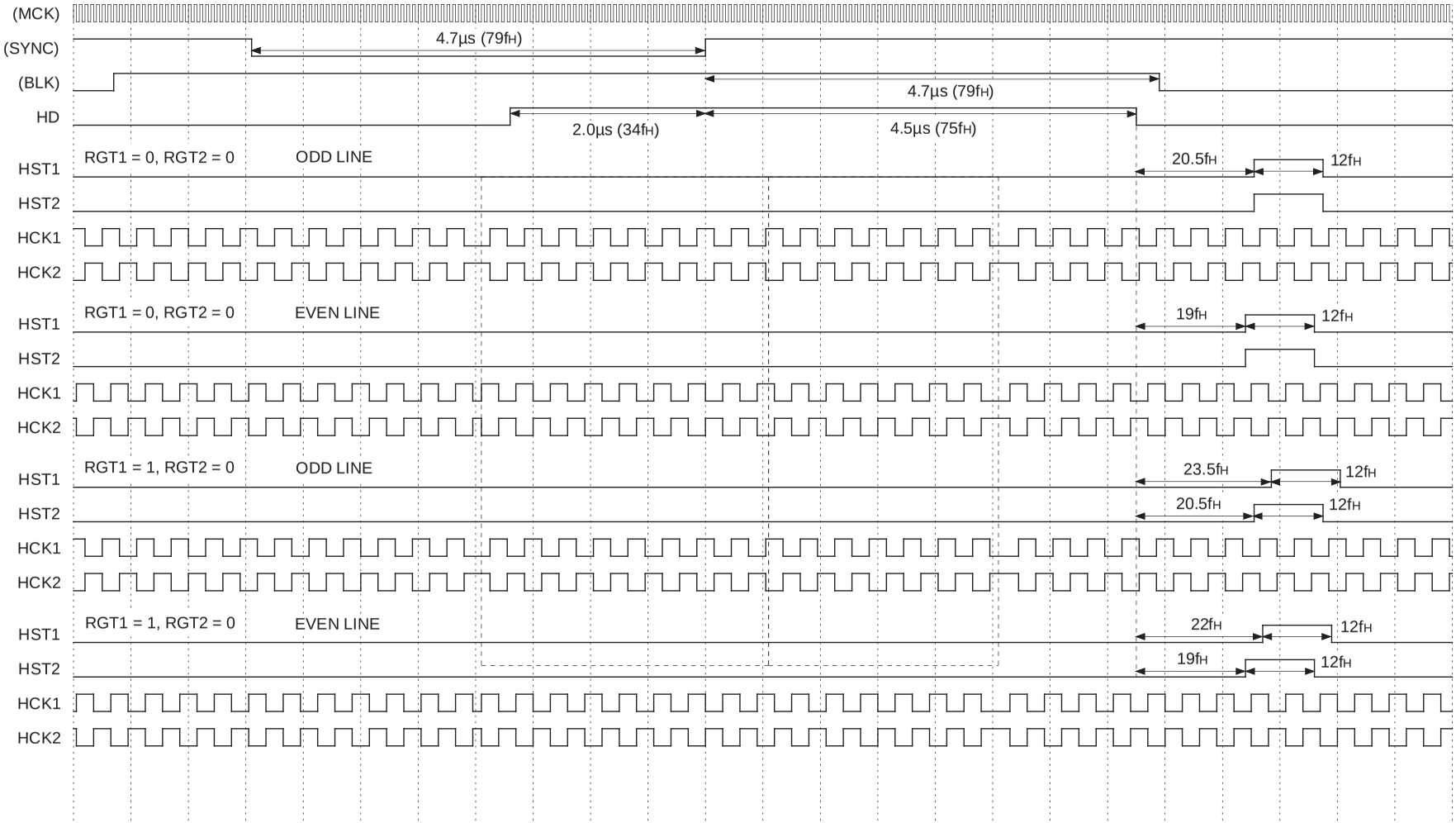
LCX009/027, 005/024 drive pulses: HST2, HCK1, HCK2, EN2, CLR, VCK3, VCK4 and VST (EN2 is high during NTSC.)

DCX501 drive pulses: HST1, HCK1, HCK2, VCK1, VCK2, PCG, EN1 and VST (HST1, PCG, EN1 and VST output inverted pulses XHST1, XPCG, XEN1 and XVST.)

Horizontal Direction Timing Chart — NTSC/PAL

LCX009 + (DCX501), LCX027 + (DCX501)

HST1 and HST2 during right/left inversion, RGT2 = 0



Note) The first (MCK), second (SYNC) and third (BLK) rows of the timing chart are pulses indicated as a reference and are not pulses output from pins.

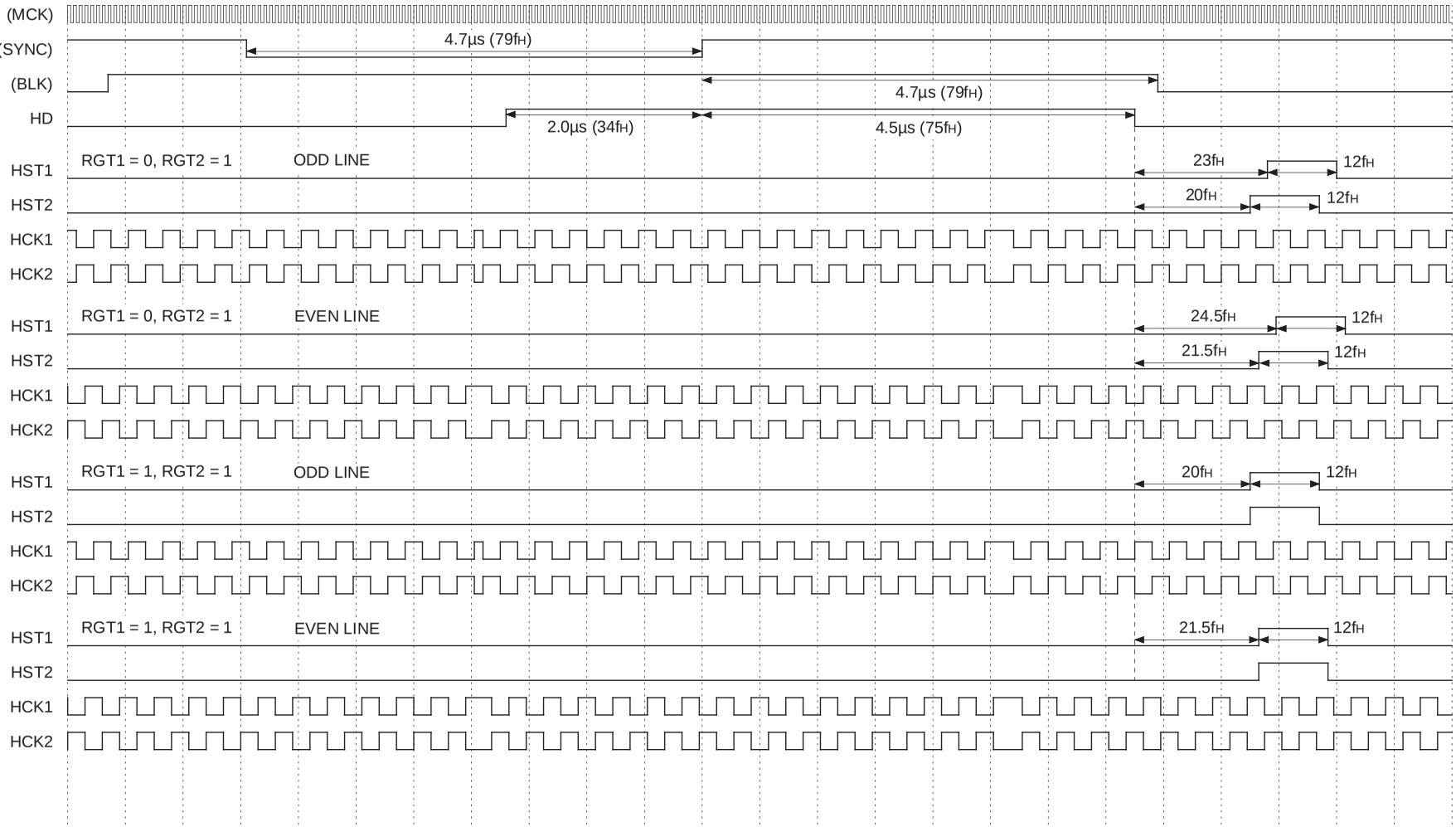
HST1: DCX501 horizontal display start pulse (inverted pulse XHST1 output)

HST2: LCX009/027 horizontal display start pulse

Horizontal Direction Timing Chart — NTSC/PAL

LCX009 + (DCX501), LCX027 + (DCX501)

HST1 and HST2 during right/left inversion, RGT2 = 1



Note) The first (MCK), second (SYNC) and third (BLK) rows of the timing chart are pulses indicated as a reference and are not pulses output from pins.

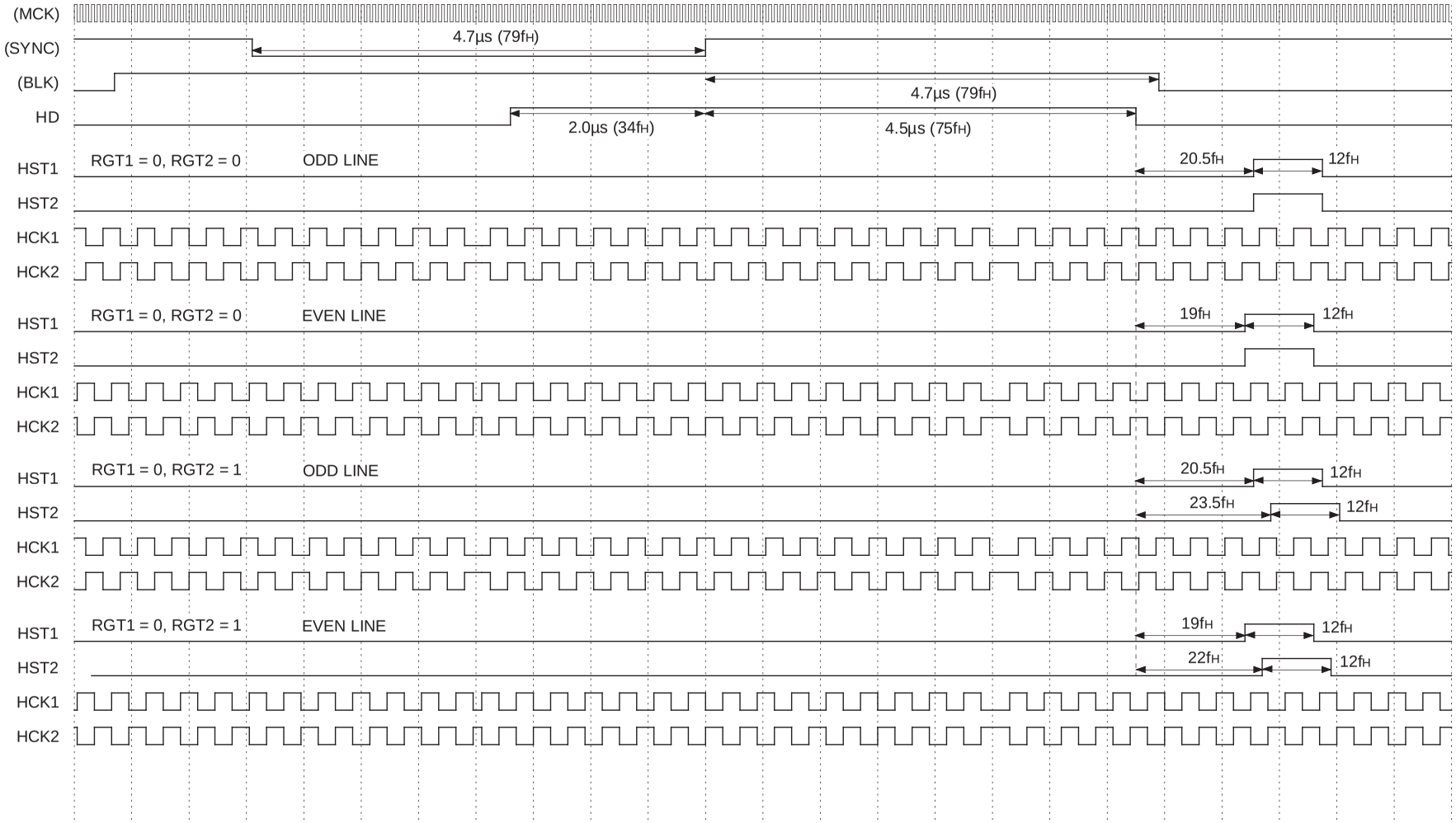
HST1: DCX501 horizontal display start pulse (inverted pulse XHST1 output)

HST2: LCX009/027 horizontal display start pulse

Horizontal Direction Timing Chart — NTSC/PAL

DCX501 + (LCX009), DCX501 + (LCX027)

HST1 and HST2 during right/left inversion, RGT1 = 0



Note) The first (MCK), second (SYNC) and third (BLK) rows of the timing chart are pulses indicated as a reference and are not pulses output from pins.

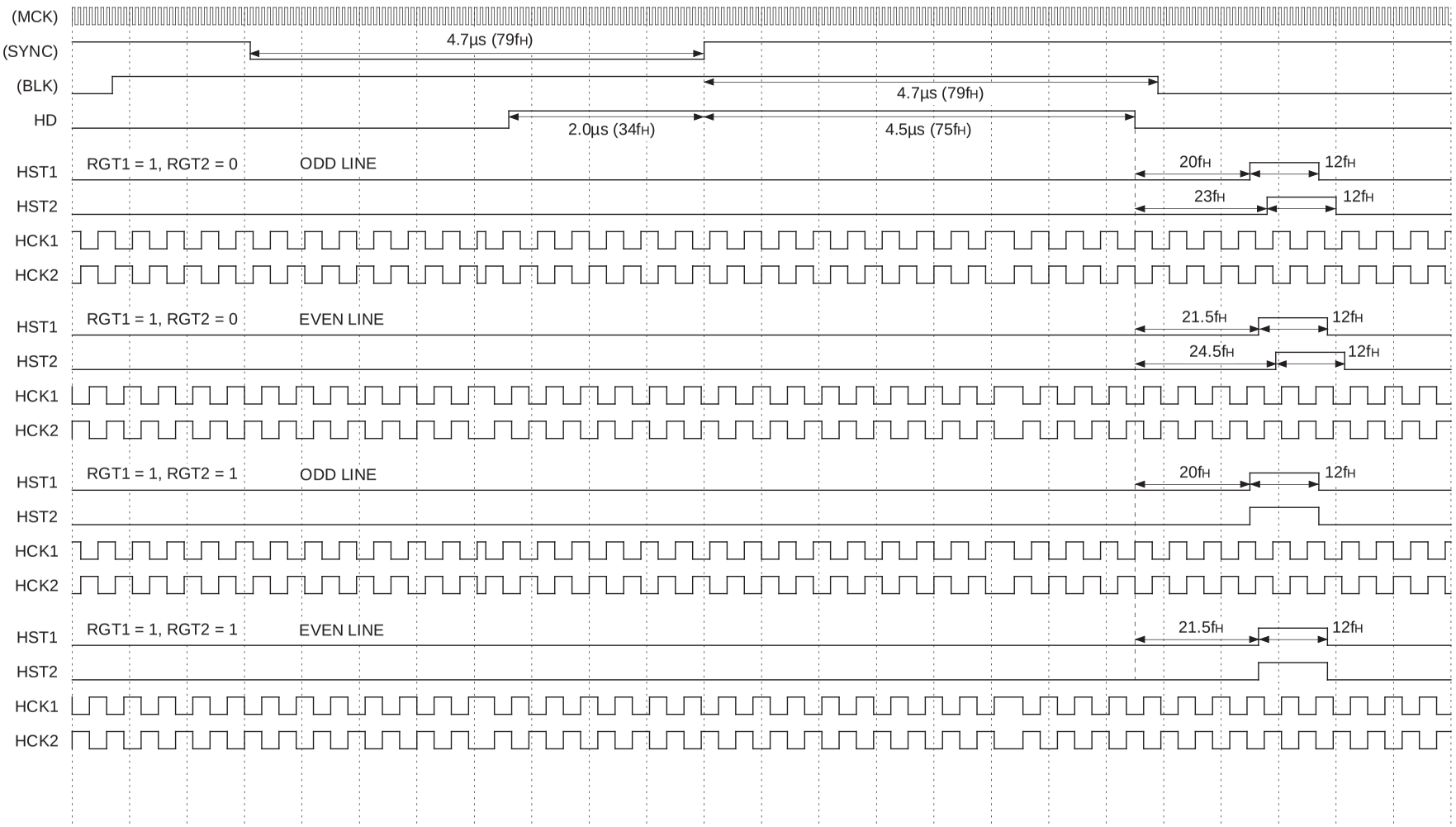
HST1: DCX501 horizontal display start pulse (inverted pulse XHST1 output)

HST2: LCX009/027 horizontal display start pulse

Horizontal Direction Timing Chart — NTSC/PAL

DCX501 + (LCX009), DCX501 + (LCX027)

HST1 and HST2 during right/left inversion, RGT1 = 1



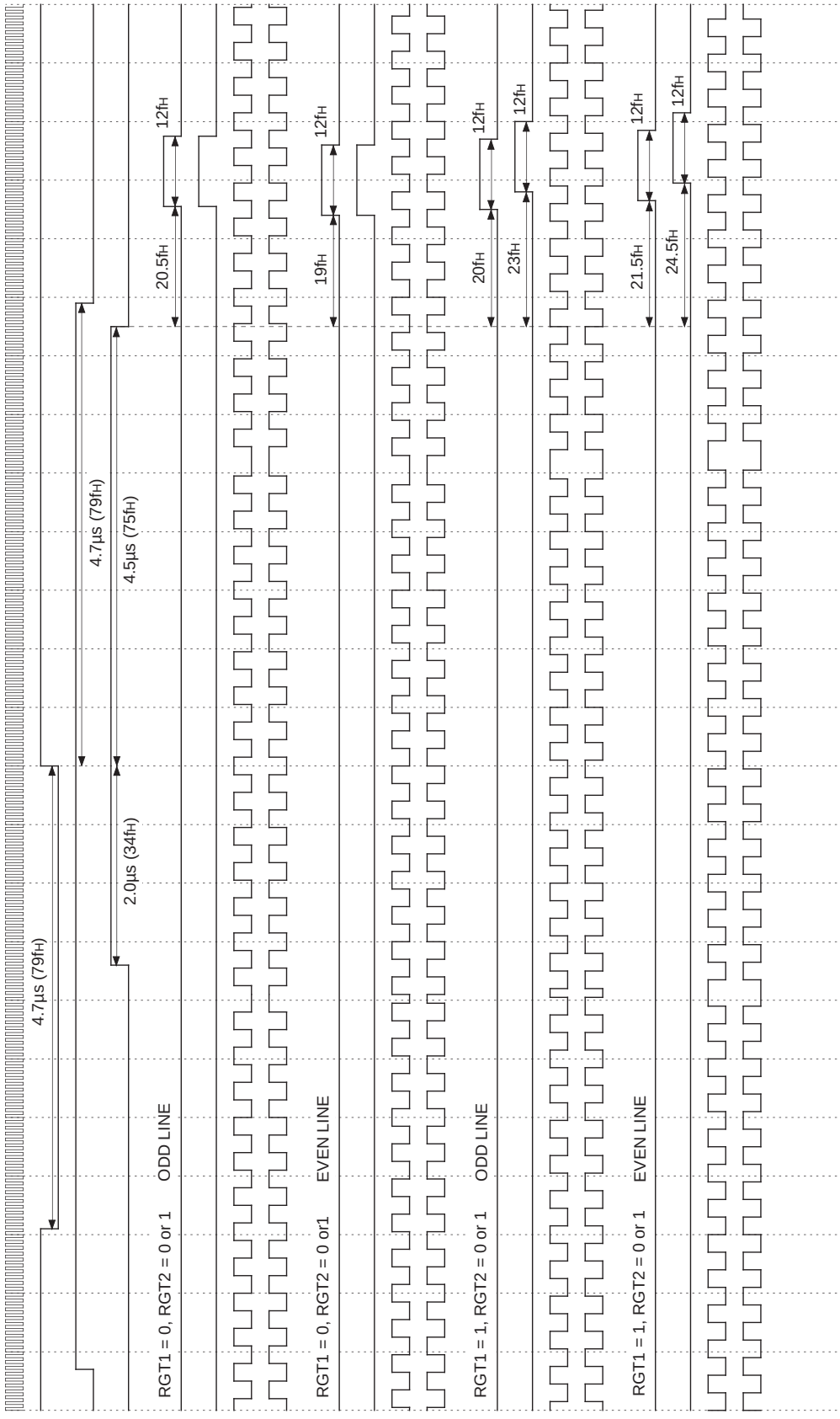
Note) The first (MCK), second (SYNC) and third (BLK) rows of the timing chart are pulses indicated as a reference and are not pulses output from pins.

HST1: DCX501 horizontal display start pulse (inverted pulse XHST1 output)

HST2: LCX009/027 horizontal display start pulse

Horizontal Direction Timing Chart — NTSC/PAL
DCX501 + (LCX005), DCX501 + (LCX024)

HST1 and HST2 during right/left inversion

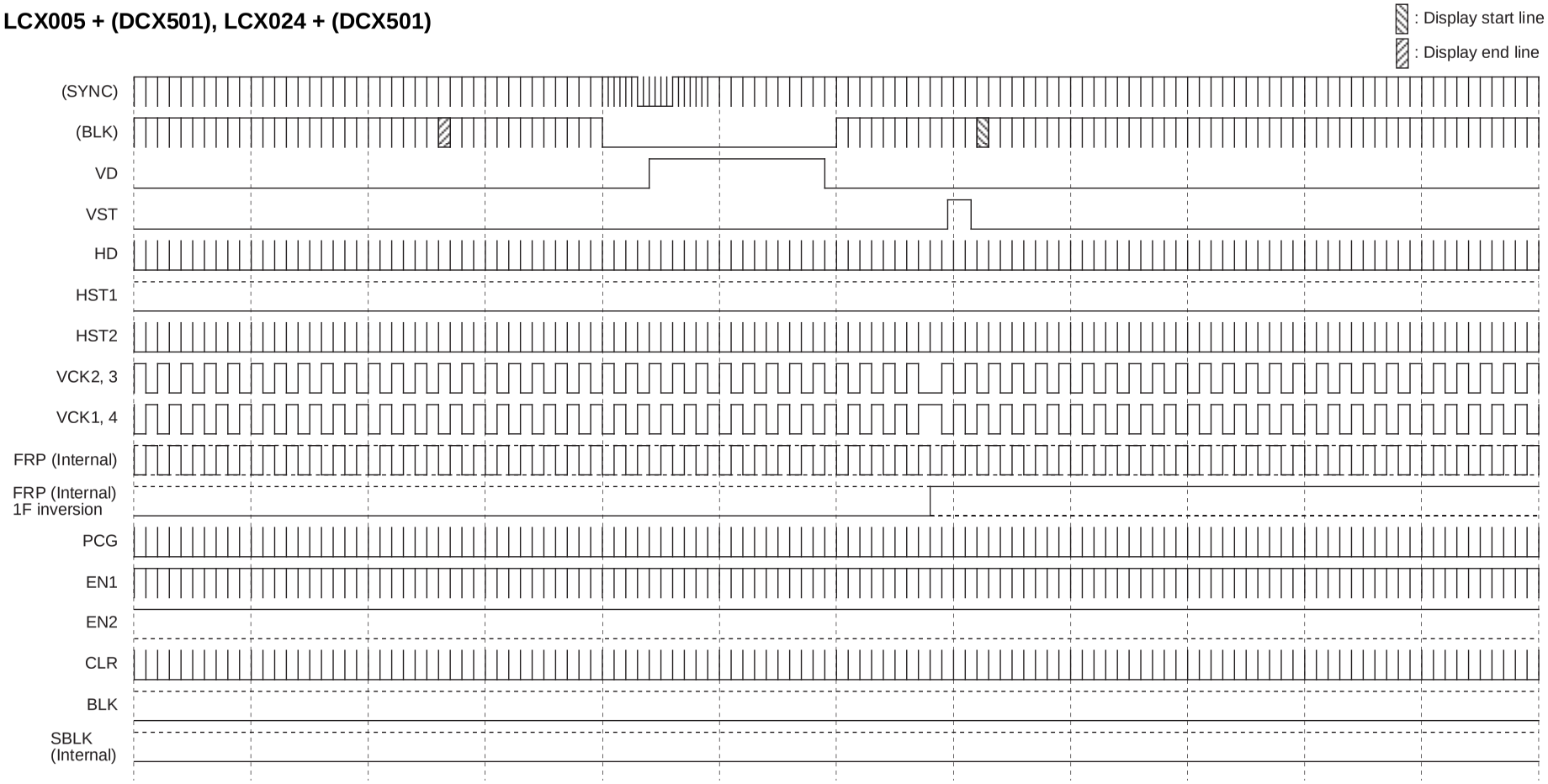


Note) The first (MCK), second (SYNC) and third (BLK) rows of the timing chart are pulses indicated as a reference and are not pulses output from pins.

HST1: DCX501 horizontal display start pulse (inverted pulse XHST1 output)

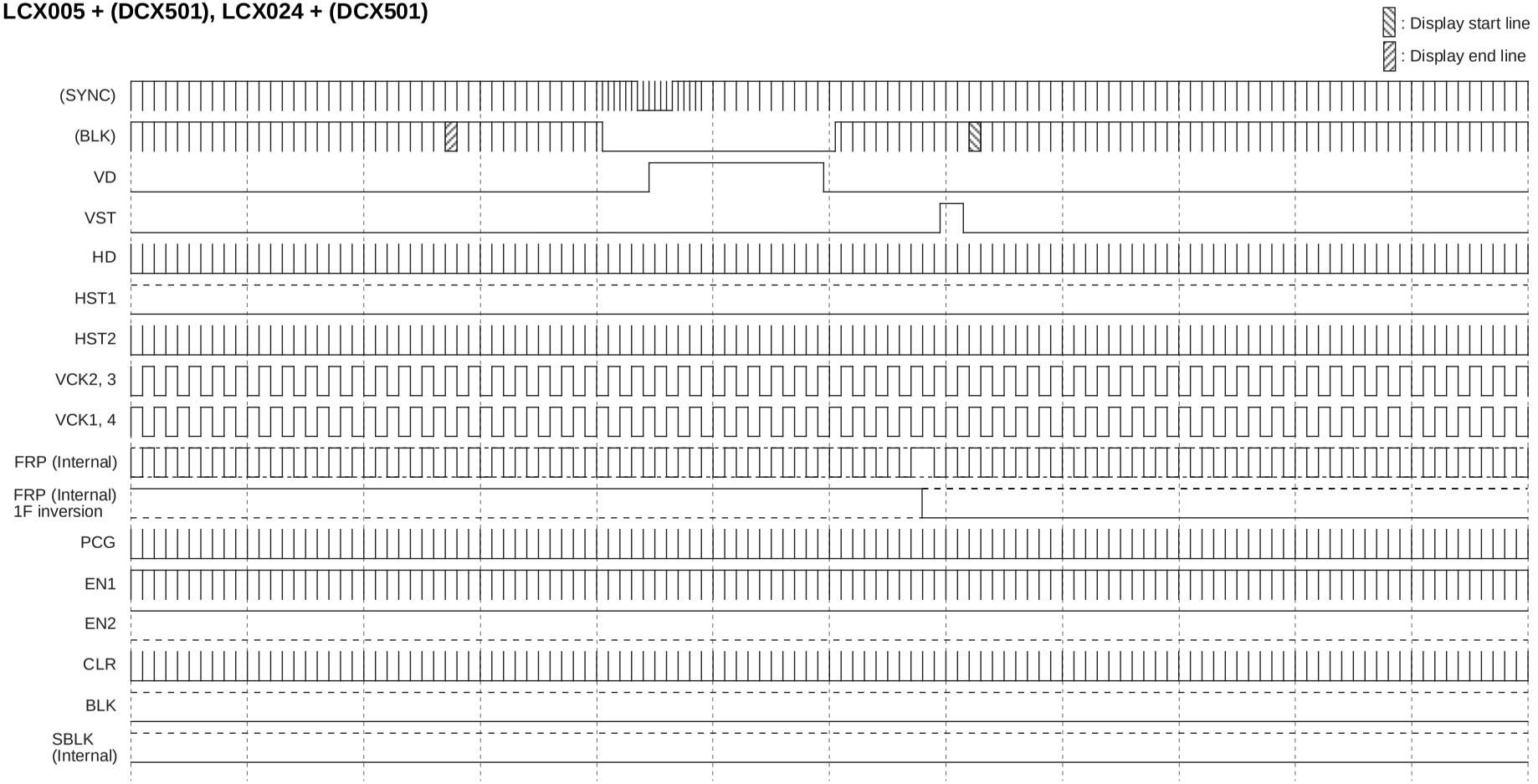
HST2: LCX005/024 horizontal display start pulse

Vertical Direction Timing Chart — NTSC
LCX005 + (DCX501), LCX024 + (DCX501)



Note) The first (SYNC) and second (BLK) rows of the timing chart are pulses indicated as a reference and are not pulses output from pins.
FRP polarity is not specified for each line and field.
LCX005/024 drive pulses: HST2, EN2, CLR, VCK3, VCK4, VST and BLK
DCX501 drive pulses: VCK1, VCK2, HST1, EN1, PCG and VST (HST1, EN1, PCG and VST output inverted pulses XHST1, XEN1, XPCG and XVST.)

Vertical Direction Timing Chart — NTSC
LCX005 + (DCX501), LCX024 + (DCX501)



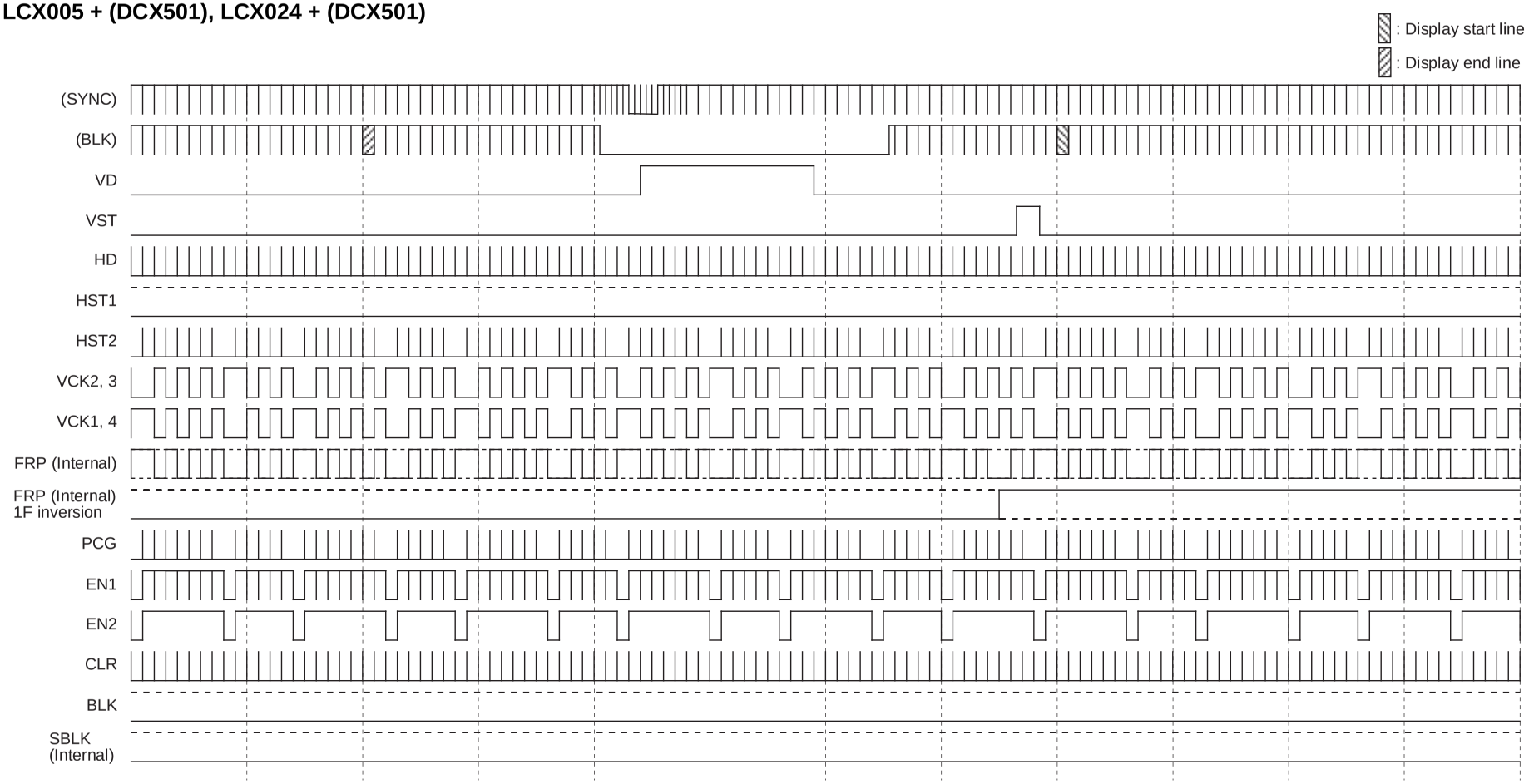
Note) The first (SYNC) and second (BLK) rows of the timing chart are pulses indicated as a reference and are not pulses output from pins.

FRP polarity is not specified for each line and field.

LCX005/024 drive pulses: HST2, EN2, CLR, VCK3, VCK4, VST and BLK

DCX501 drive pulses: VCK1, VCK2, HST1, EN1, PCG and VST (HST1, EN1, PCG and VST output inverted pulses XHST1, XEN1, XPCG and XVST.)

Vertical Direction Timing Chart — PAL
LCX005 + (DCX501), LCX024 + (DCX501)



Note) The first (SYNC) and second (BLK) rows of the timing chart are pulses indicated as a reference and are not pulses output from pins.

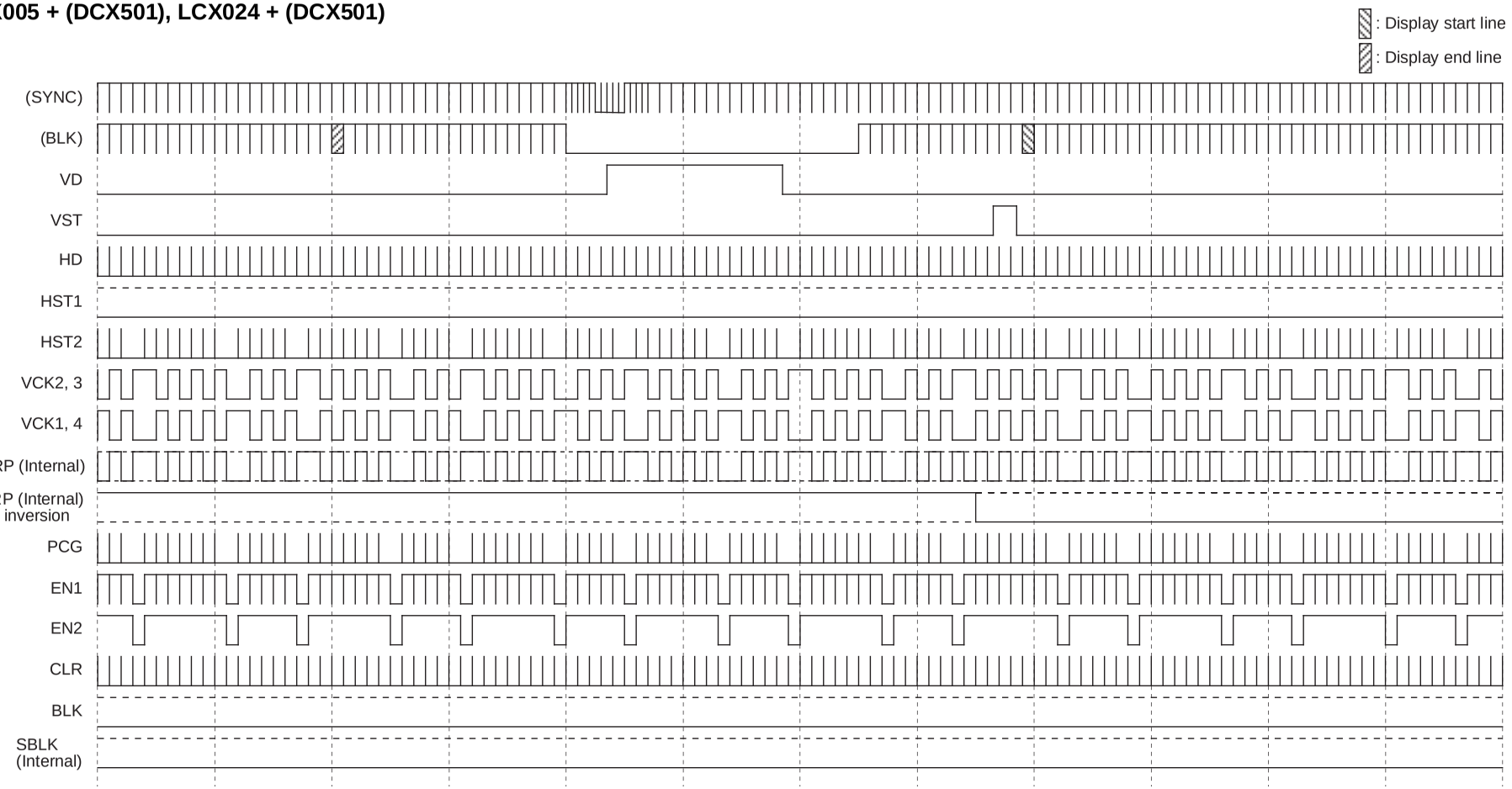
FRP polarity is not specified for each line and field.

LCX005/024 drive pulses: HST2, EN2, CLR, VCK3, VCK4, VST and BLK

DCX501 drive pulses: VCK1, VCK2, HST1, EN1, PCG and VST (HST1, EN1, PCG and VST output inverted pulses XHST1, XEN1, XPCG and XVST.)

Vertical Direction Timing Chart — PAL

LCX005 + (DCX501), LCX024 + (DCX501)



Note) The first (SYNC) and second (BLK) rows of the timing chart are pulses indicated as a reference and are not pulses output from pins.

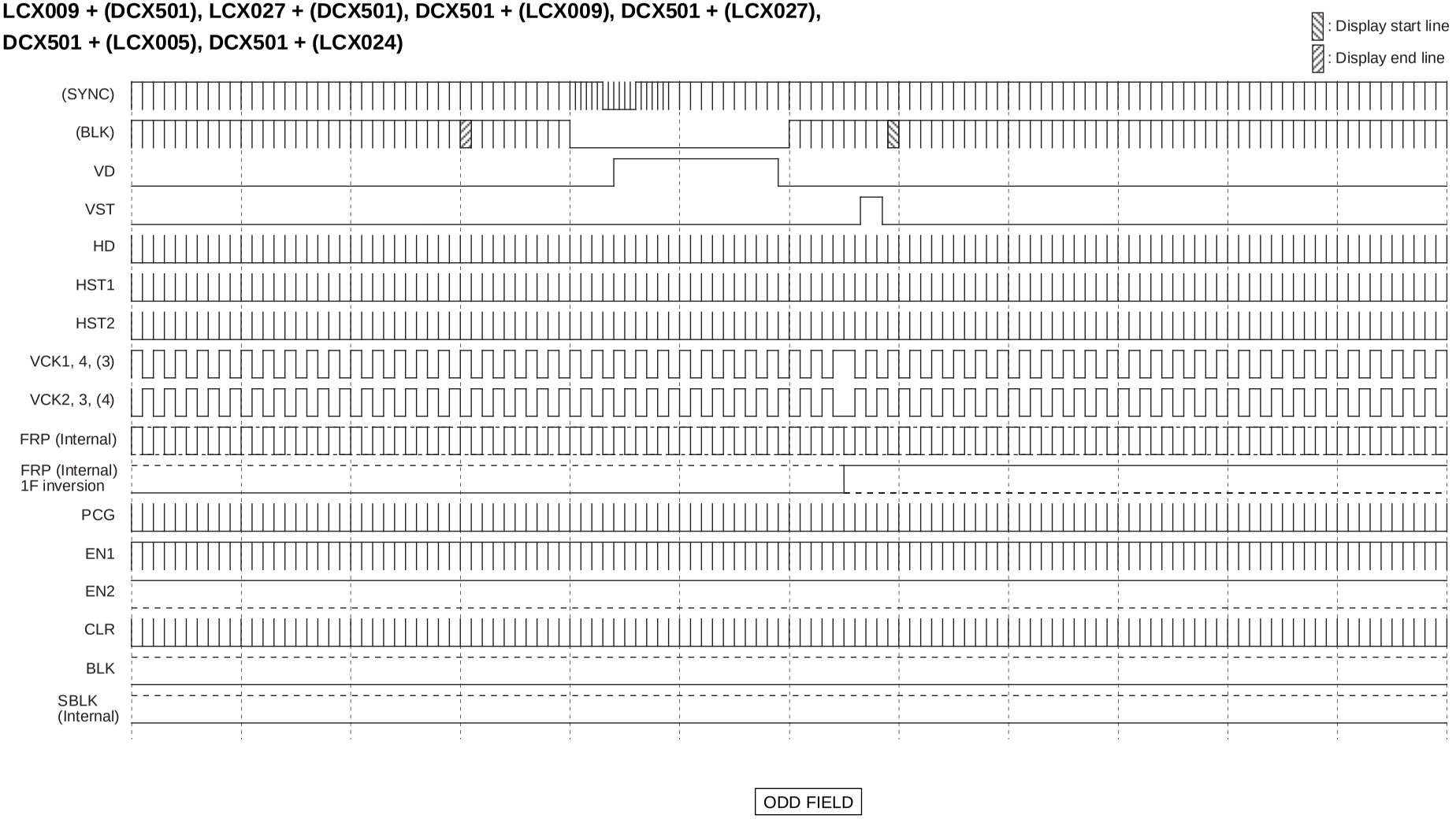
FRP polarity is not specified for each line and field.

LCX005/024 drive pulses: HST2, EN2, CLR, VCK3, VCK4, VST and BLK

DCX501 drive pulses: VCK1, VCK2, HST1, EN1, PCG and VST (HST1, EN1, PCG and VST output inverted pulses XHST1, XEN1, XPCG and XVST.)

Vertical Direction Timing Chart — NTSC

LCX009 + (DCX501), LCX027 + (DCX501), DCX501 + (LCX009), DCX501 + (LCX027), DCX501 + (LCX005), DCX501 + (LCX024)



Note) The first (SYNC) and second (BLK) rows of the timing chart are pulses indicated as a reference and are not pulses output from pins.

FRP polarity is not specified for each line and field.

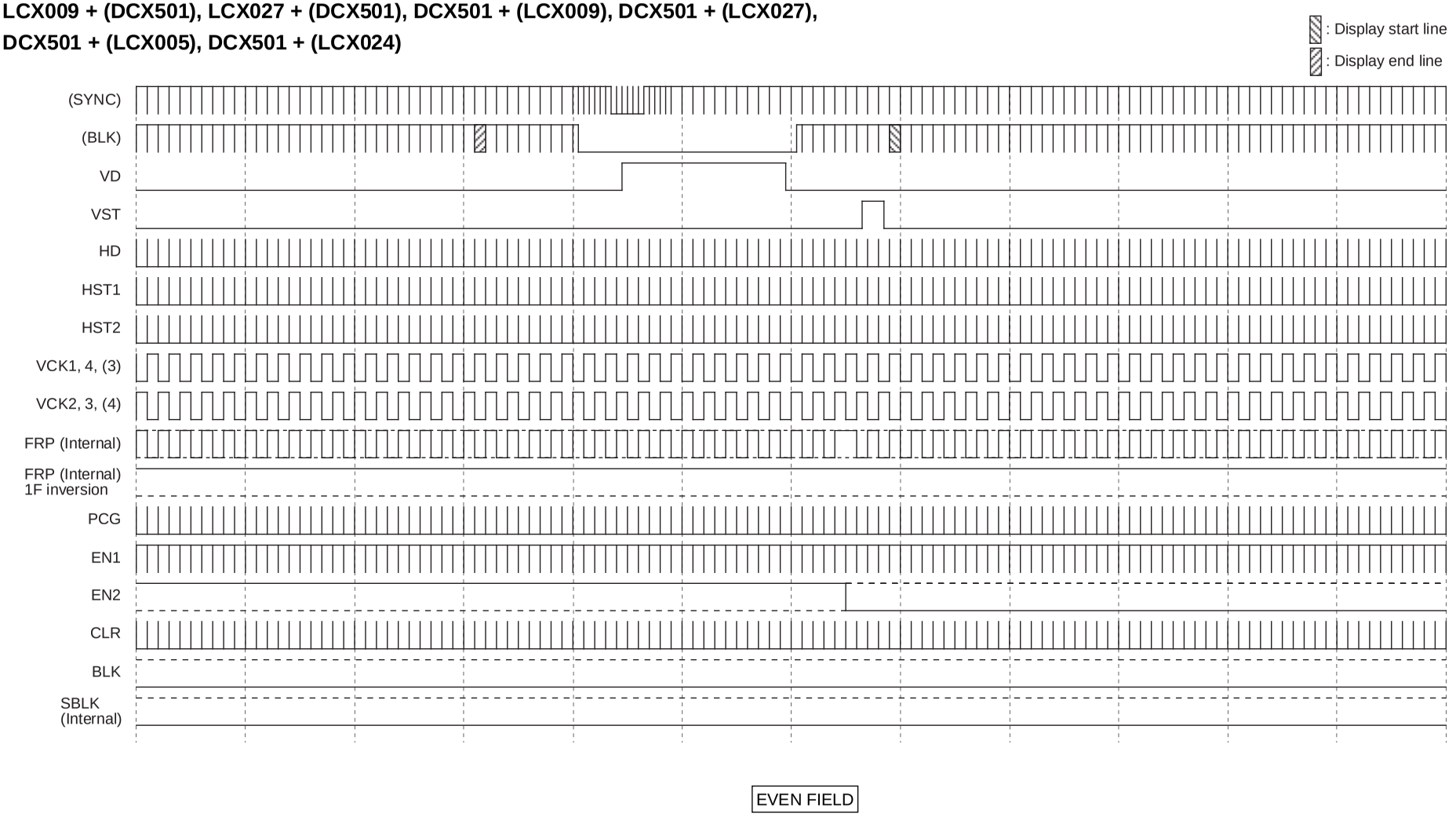
In LCX009 + (DCX501) and DCX501 + (LCX009) modes, the VCK3 and VCK4 polarities are inverted. (VCK(3) and VCK(4))

LCX009/027 drive pulses: HST2, EN2, CLR, VCK3, VCK4, VST and BLK

DCX501 drive pulses: VCK1, VCK2, HST1, EN1, PCG and VST (HST1, EN1, PCG and VST output inverted pulses XHST1, XEN1, XPCG and XVST.)

Vertical Direction Timing Chart — NTSC

LCX009 + (DCX501), LCX027 + (DCX501), DCX501 + (LCX009), DCX501 + (LCX027), DCX501 + (LCX005), DCX501 + (LCX024)



Note) The first (SYNC) and second (BLK) rows of the timing chart are pulses indicated as a reference and are not pulses output from pins.

FRP polarity is not specified for each line and field.

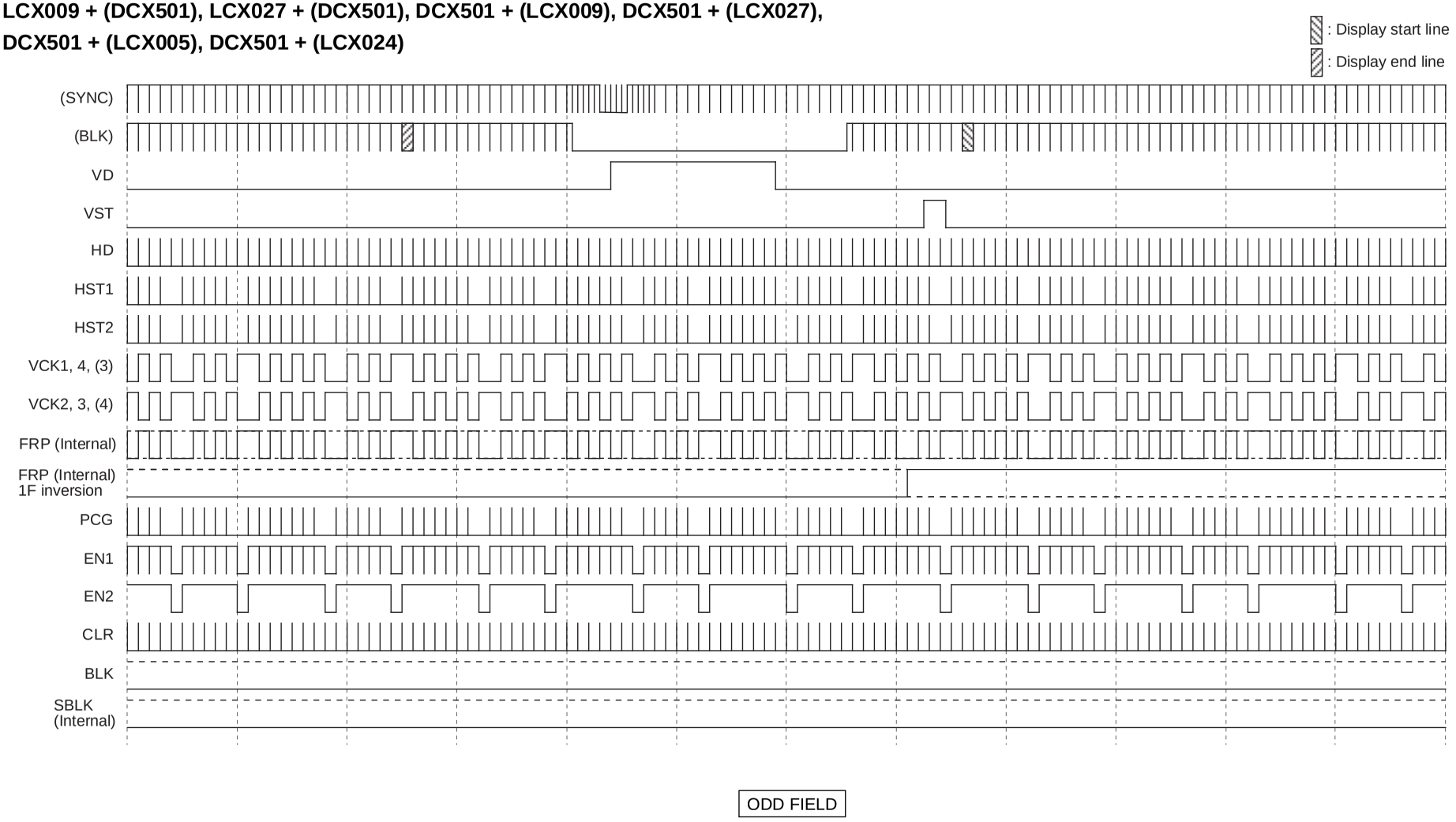
In LCX009 + (DCX501) and DCX501 + (LCX009) modes, the VCK3 and VCK4 polarities are inverted. (VCK(3) and VCK(4))

LCX009/027 drive pulses: HST2, EN2, CLR, VCK3, VCK4, VST and BLK

DCX501 drive pulses: VCK1, VCK2, HST1, EN1, PCG and VST (HST1, EN1, PCG and VST output inverted pulses XHST1, XEN1, XPCG and XVST.)

Vertical Direction Timing Chart — PAL

LCX009 + (DCX501), LCX027 + (DCX501), DCX501 + (LCX009), DCX501 + (LCX027), DCX501 + (LCX005), DCX501 + (LCX024)



Note) The first (SYNC) and second (BLK) rows of the timing chart are pulses indicated as a reference and are not pulses output from pins.

FRP polarity is not specified for each line and field.

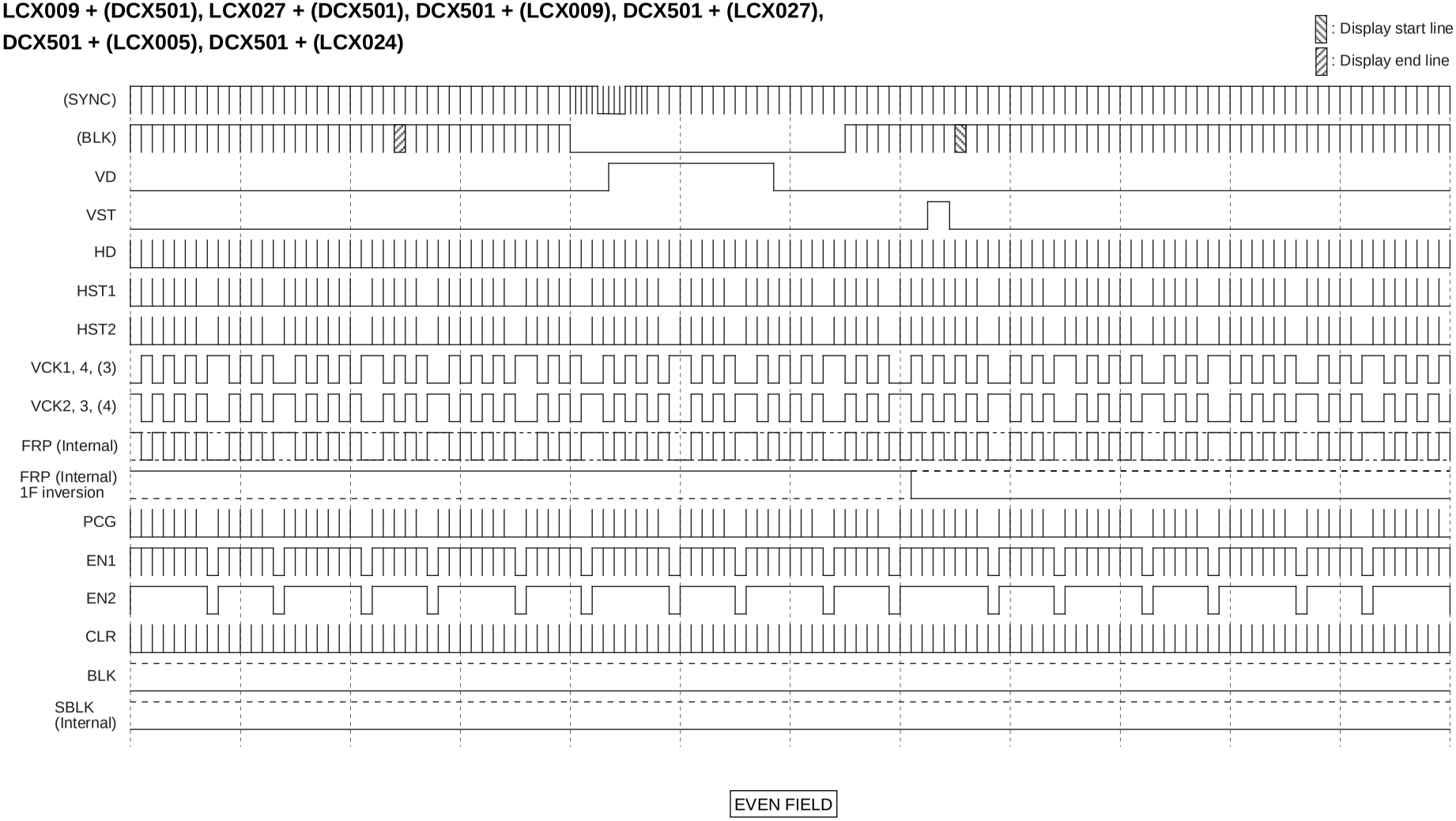
In LCX009 + (DCX501) and DCX501 + (LCX009) modes, the VCK3 and VCK4 polarities are inverted. (VCK(3) and VCK(4))

LCX009/027 drive pulses: HST2, EN2, CLR, VCK3, VCK4, VST and BLK

DCX501 drive pulses: VCK1, VCK2, HST1, EN1, PCG and VST (HST1, EN1, PCG and VST output inverted pulses XHST1, XEN1, XPCG and XVST.)

Vertical Direction Timing Chart — PAL

LCX009 + (DCX501), LCX027 + (DCX501), DCX501 + (LCX009), DCX501 + (LCX027), DCX501 + (LCX005), DCX501 + (LCX024)



Note) The first (SYNC) and second (BLK) rows of the timing chart are pulses indicated as a reference and are not pulses output from pins.

FRP polarity is not specified for each line and field.

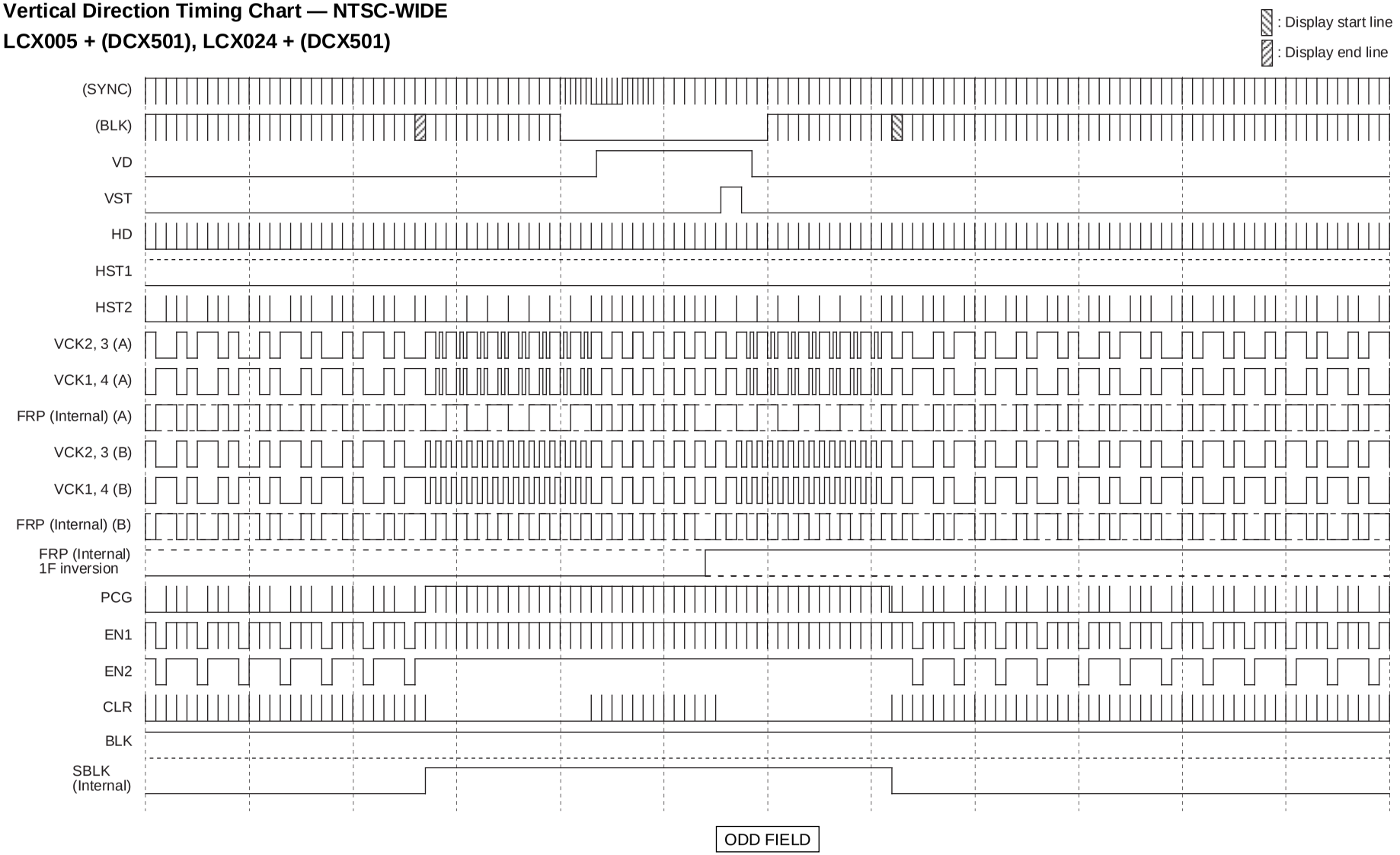
In LCX009 + (DCX501) and DCX501 + (LCX009) modes, the VCK3 and VCK4 polarities are inverted. (VCK(3) and VCK(4))

LCX009/027 drive pulses: HST2, EN2, CLR, VCK3, VCK4, VST and BLK

DCX501 drive pulses: VCK1, VCK2, HST1, EN1, PCG and VST (HST1, EN1, PCG and VST output inverted pulses XHST1, XEN1, XPCG and XVST.)

Vertical Direction Timing Chart — NTSC-WIDE

LCX005 + (DCX501), LCX024 + (DCX501)



Note) The first (SYNC) and second (BLK) rows of the timing chart are pulses indicated as a reference and are not pulses output from pins.

FRP polarity is not specified for each line and field.

LCX005 + (DCX501) mode: VCK(A) output

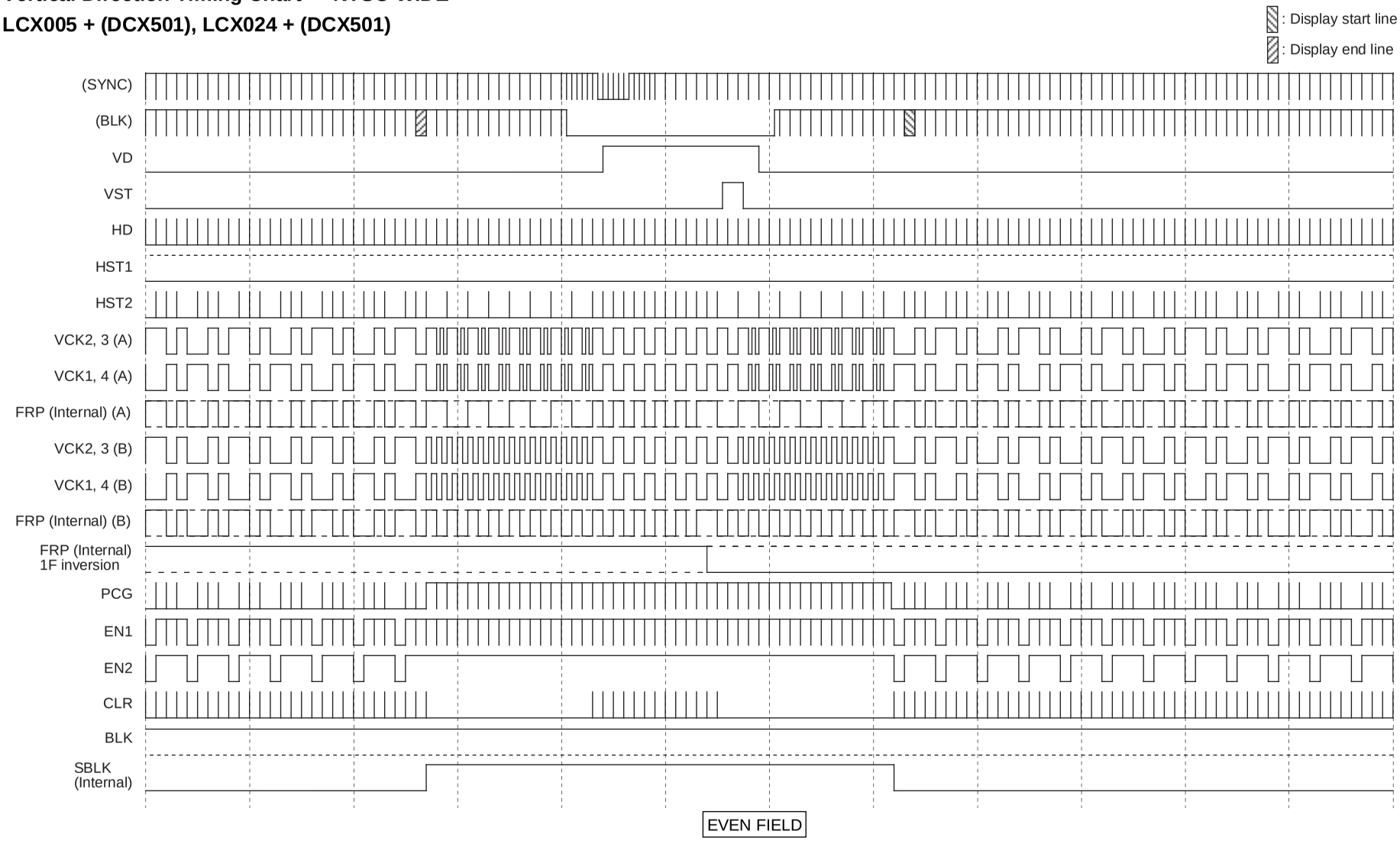
LCX024 + (DCX501) mode: VCK(B) output

LCX005/024 drive pulses: HST2, EN2, CLR, VCK3, VCK4, VST and BLK

DCX501 drive pulses: VCK1, VCK2, HST1, EN1, PCG and VST (HST1, EN1, PCG and VST output inverted pulses XHST1, XEN1, XPCG and XVST.)

Vertical Direction Timing Chart — NTSC-WIDE

LCX005 + (DCX501), LCX024 + (DCX501)



Note) The first (SYNC) and second (BLK) rows of the timing chart are pulses indicated as a reference and are not pulses output from pins.

FRP polarity is not specified for each line and field.

LCX005 + (DCX501) mode: VCK(A) output

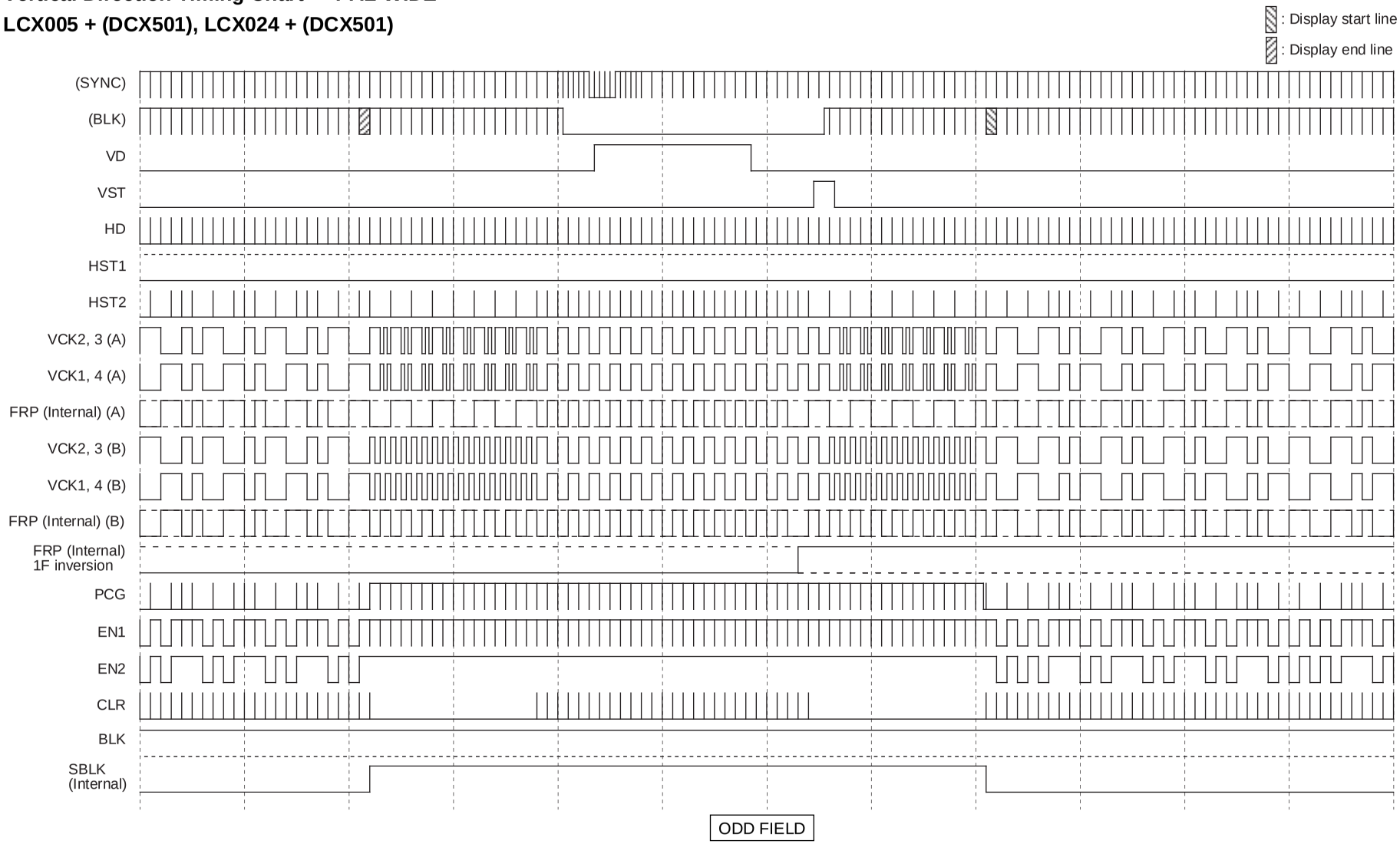
LCX024 + (DCX501) mode: VCK(B) output

LCX005/024 drive pulses: HST2, EN2, CLR, VCK3, VCK4, VST and BLK

DCX501 drive pulses: VCK1, VCK2, HST1, EN1, PCG and VST (HST1, EN1, PCG and VST output inverted pulses XHST1, XEN1, XPCG and XVST.)

Vertical Direction Timing Chart — PAL-WIDE

LCX005 + (DCX501), LCX024 + (DCX501)



Note) The first (SYNC) and second (BLK) rows of the timing chart are pulses indicated as a reference and are not pulses output from pins.

FRP polarity is not specified for each line and field.

LCX005 + (DCX501) mode: VCK(A) output

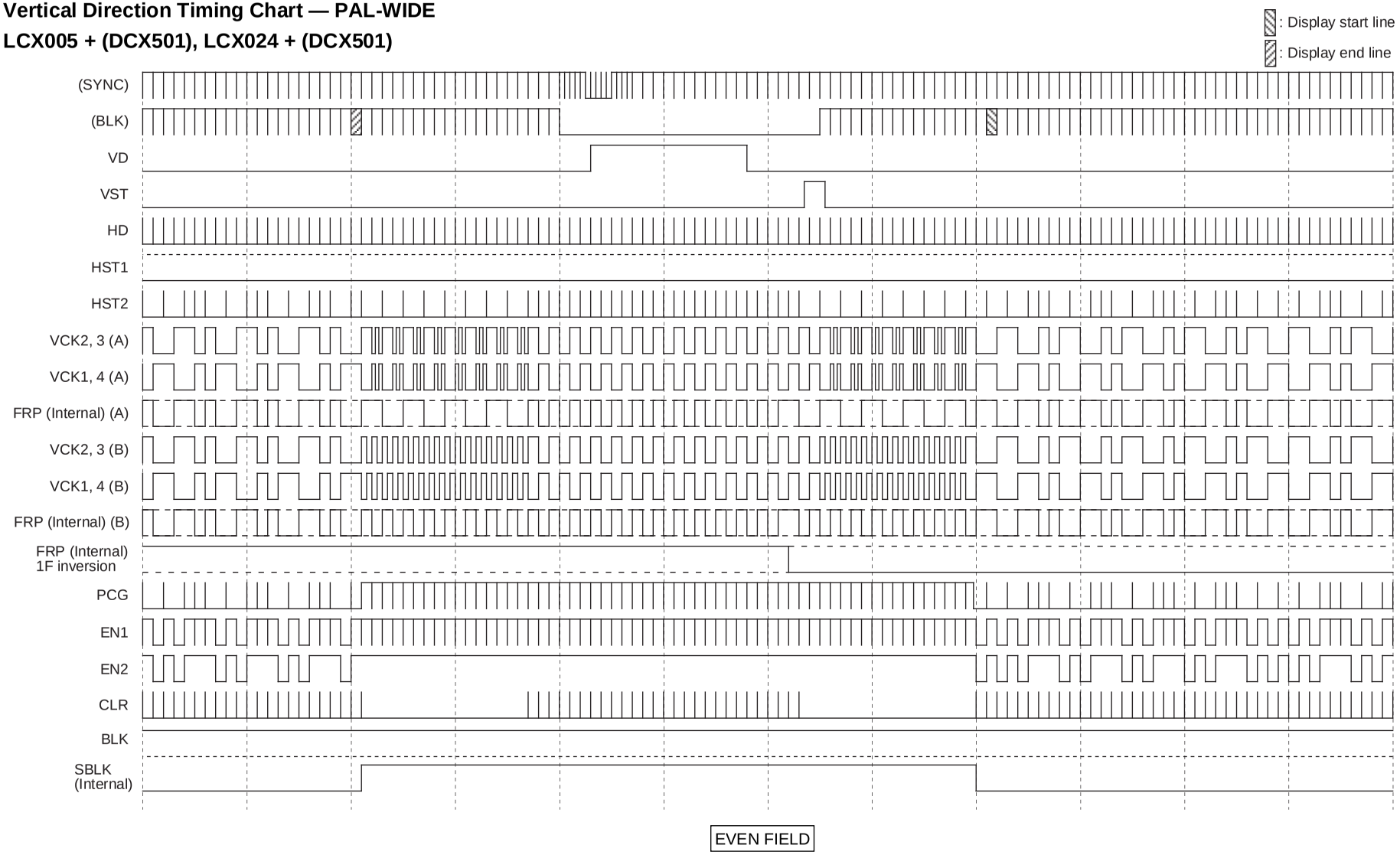
LCX024 + (DCX501) mode: VCK(B) output

LCX005/024 drive pulses: HST2, EN2, CLR, VCK3, VCK4, VST and BLK

DCX501 drive pulses: VCK1, VCK2, HST1, EN1, PCG and VST (HST1, EN1, PCG and VST output inverted pulses XHST1, XEN1, XPCG and XVST.)

Vertical Direction Timing Chart — PAL-WIDE

LCX005 + (DCX501), LCX024 + (DCX501)



Note) The first (SYNC) and second (BLK) rows of the timing chart are pulses indicated as a reference and are not pulses output from pins.

FRP polarity is not specified for each line and field.

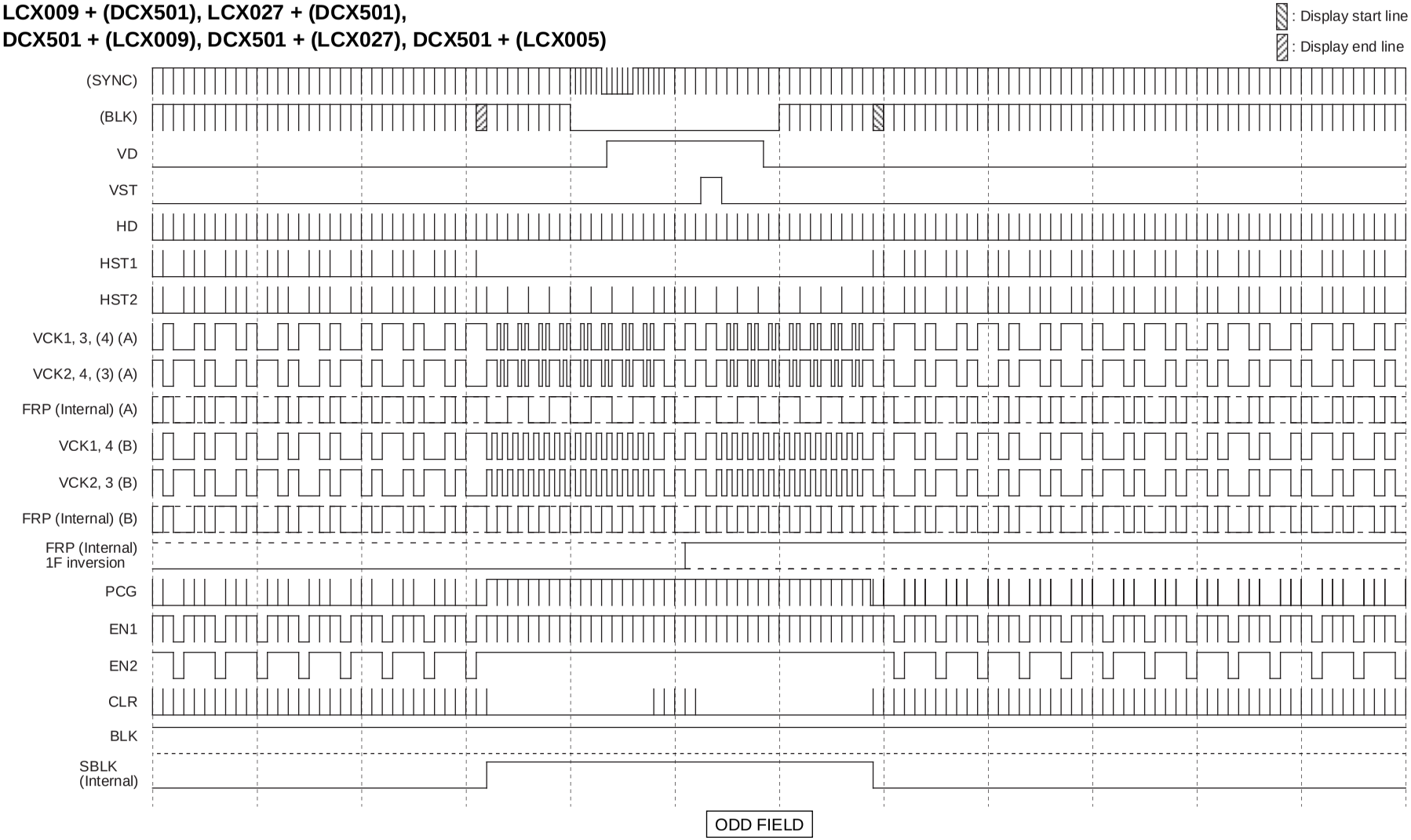
LCX005 + (DCX501) mode: VCK(A) output

LCX024 + (DCX501) mode: VCK(B) output

LCX005/024 drive pulses: HST2, EN2, CLR, VCK3, VCK4, VST and BLK

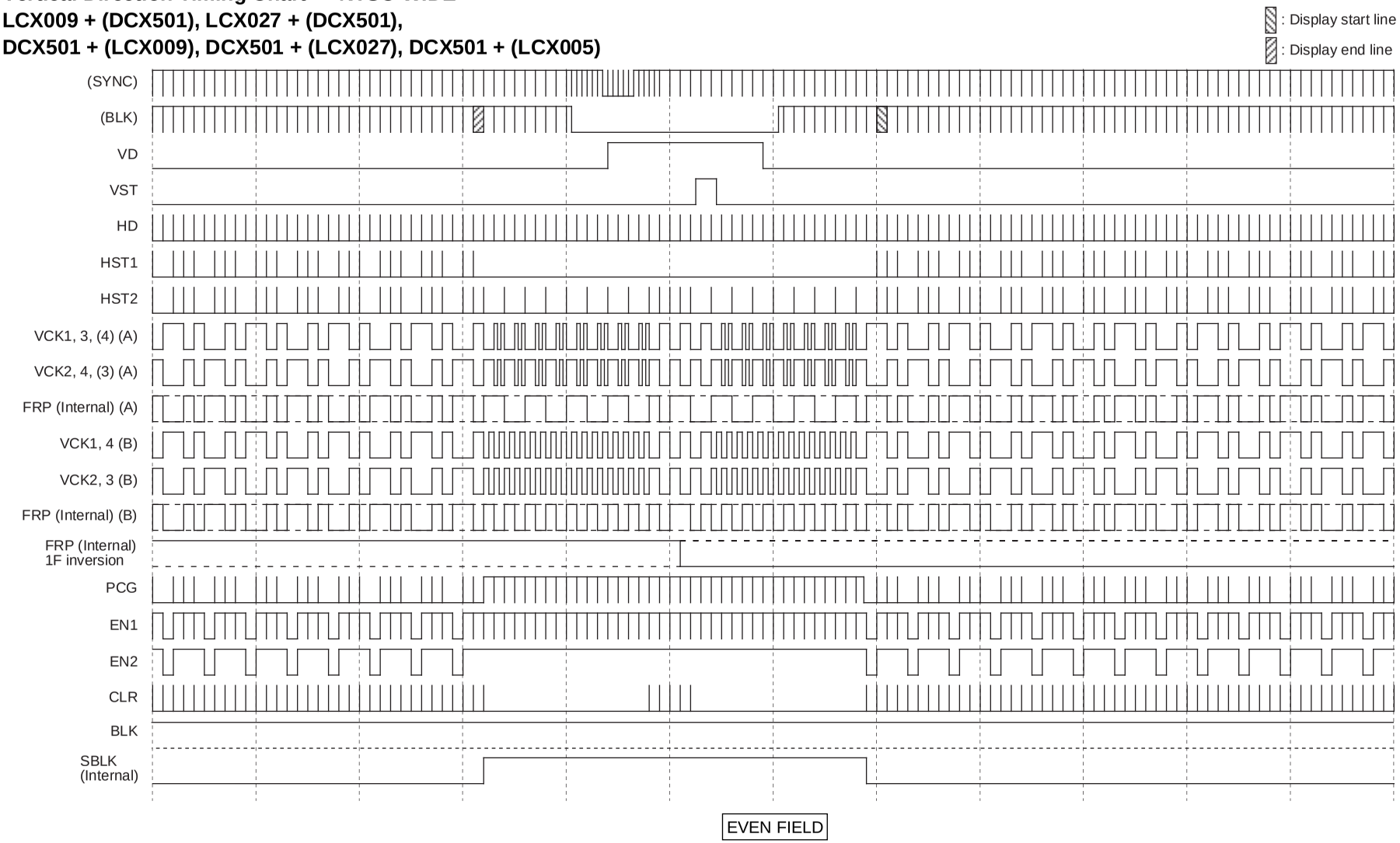
DCX501 drive pulses: VCK1, VCK2, HST1, EN1, PCG and VST (HST1, EN1, PCG and VST output inverted pulses XHST1, XEN1, XPCG and XVST.)

Vertical Direction Timing Chart — NTSC-WIDE
LCX009 + (DCX501), LCX027 + (DCX501),
DCX501 + (LCX009), DCX501 + (LCX027), DCX501 + (LCX005)



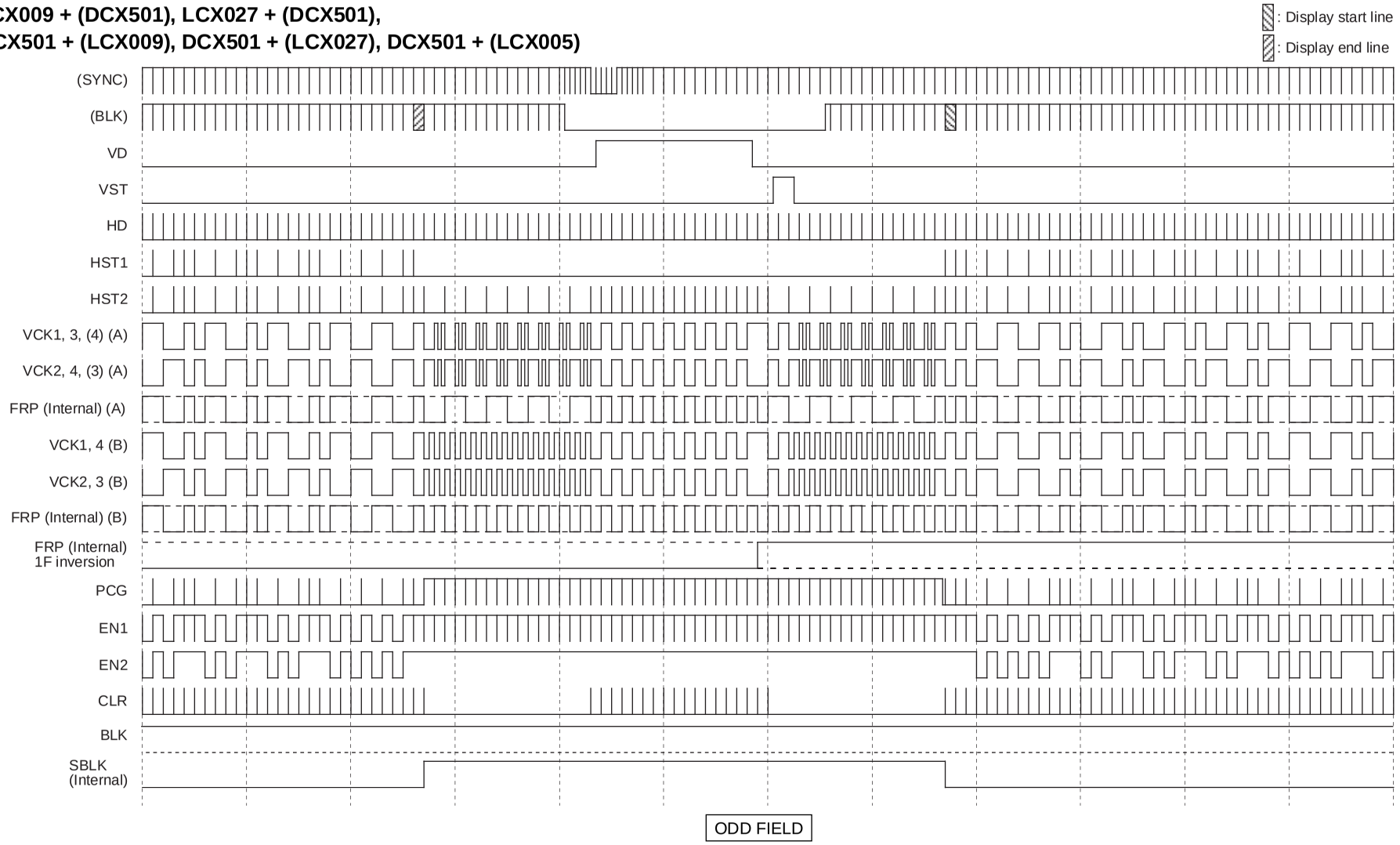
Note) The first (SYNC) and second (BLK) rows of the timing chart are pulses indicated as a reference and are not pulses output from pins.
FRP polarity is not specified for each line and field.
LCX009 + (DCX501), DCX501 + (LCX009) and DCX501 + (LCX005) modes: VCK(A) output
(In DCX501 + (LCX005) mode the polarity is inverted. (VCK(3)(A) and VCK(4)(A)))
LCX027 + (DCX501) and DCX501 + (LCX027) modes: VCK(B) output
LCX009/027 drive pulses: HST2, EN2, CLR, VCK3, VCK4, VST and BLK
DCX501 drive pulses: VCK1, VCK2, HST1, EN1, PCG and VST (HST1, EN1, PCG and VST output inverted pulses XHST1, XEN1, XPCG and XVST.)

Vertical Direction Timing Chart — NTSC-WIDE
LCX009 + (DCX501), LCX027 + (DCX501),
DCX501 + (LCX009), DCX501 + (LCX027), DCX501 + (LCX005)



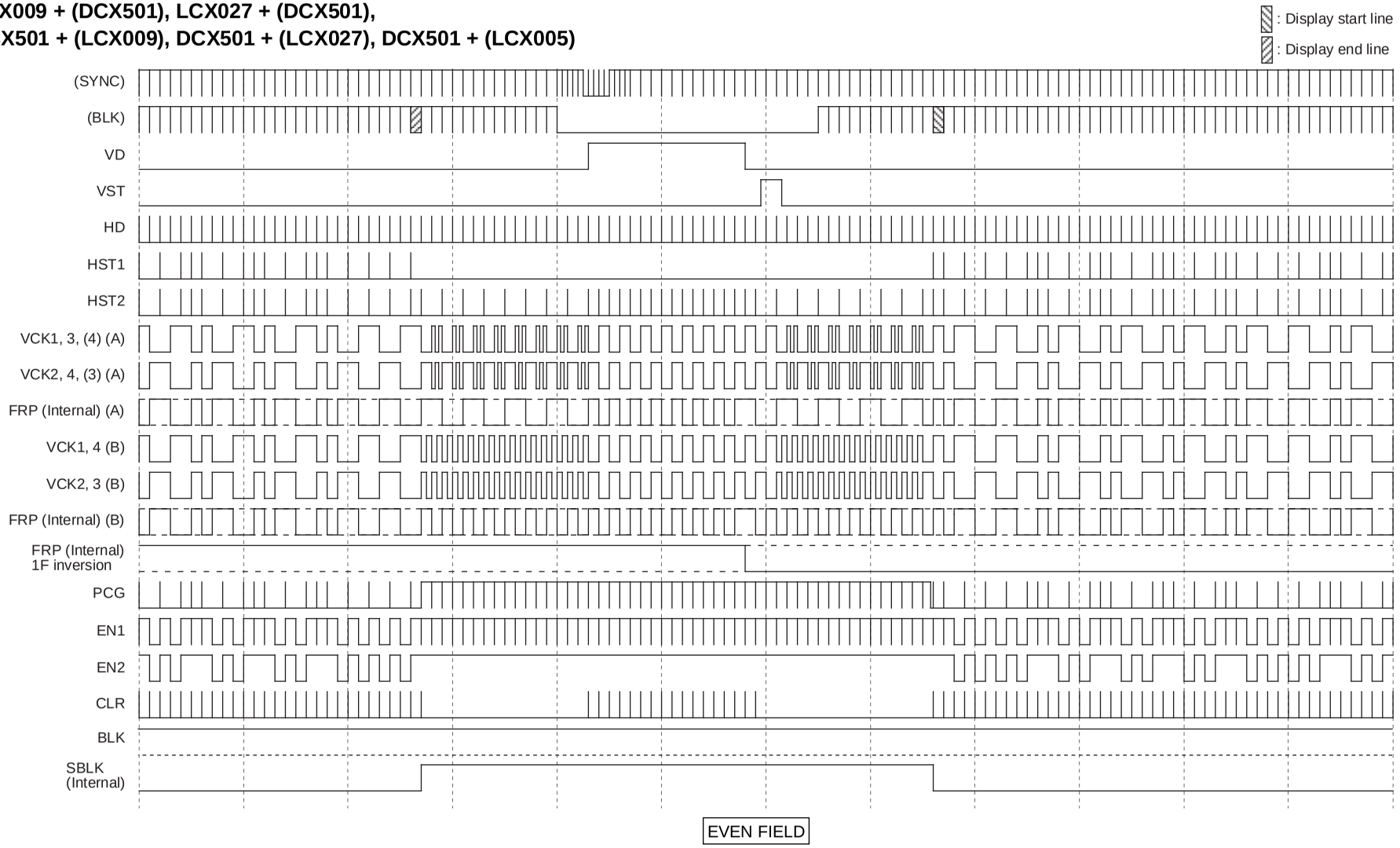
Note) The first (SYNC) and second (BLK) rows of the timing chart are pulses indicated as a reference and are not pulses output from pins.
FRP polarity is not specified for each line and field.
LCX009 + (DCX501), DCX501 + (LCX009) and DCX501 + (LCX005) modes: VCK(A) output
(In DCX501 + (LCX005) mode the polarity is inverted. (VCK(3)(A) and VCK(4)(A)))
LCX027 + (DCX501) and DCX501 + (LCX027) modes: VCK(B) output
LCX009/027 drive pulses: HST2, EN2, CLR, VCK3, VCK4, VST and BLK
DCX501 drive pulses: VCK1, VCK2, HST1, EN1, PCG and VST (HST1, EN1, PCG and VST output inverted pulses XHST1, XEN1, XPCG and XVST.)

Vertical Direction Timing Chart — PAL-WIDE
LCX009 + (DCX501), LCX027 + (DCX501),
DCX501 + (LCX009), DCX501 + (LCX027), DCX501 + (LCX005)



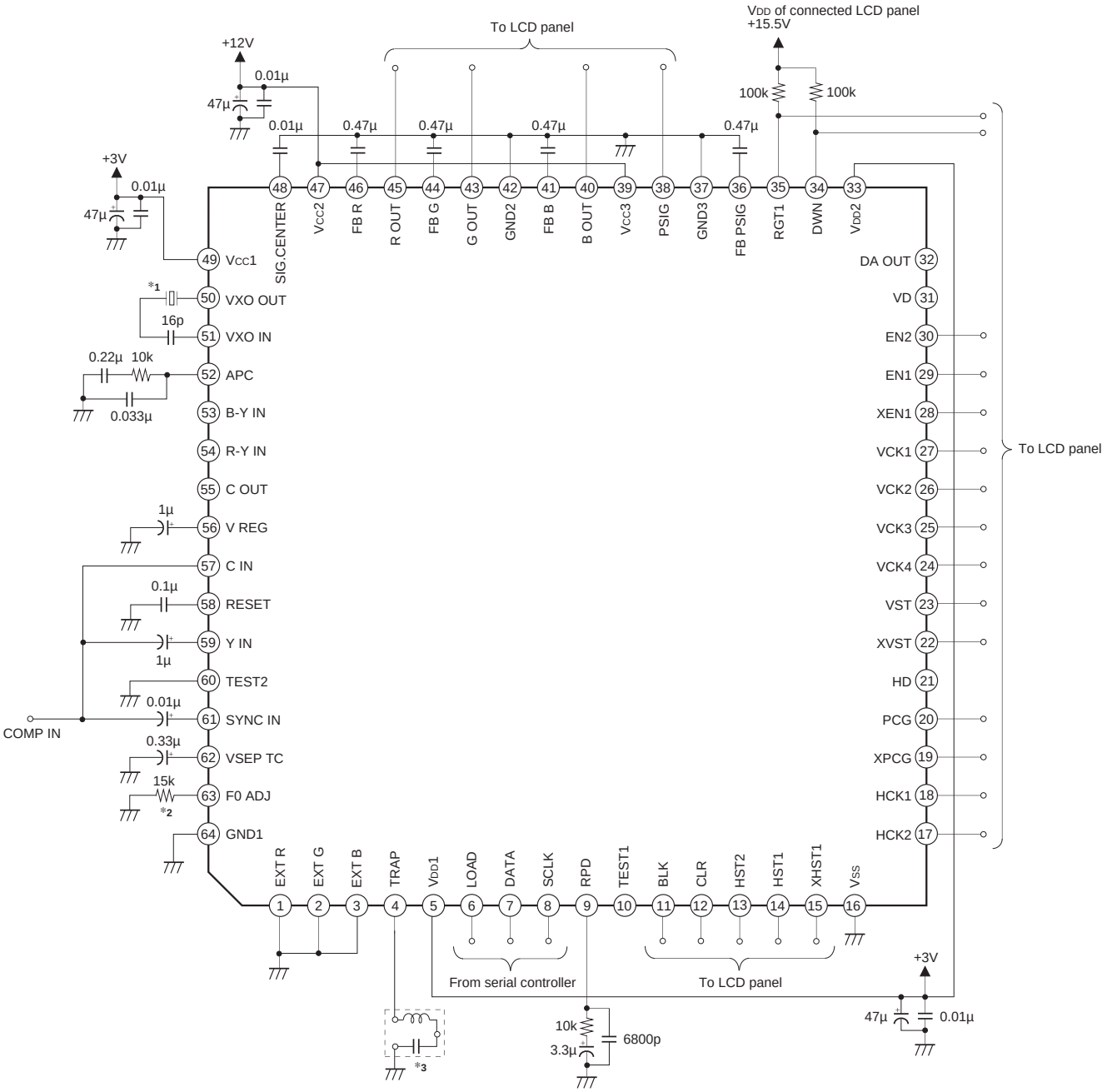
Note) The first (SYNC) and second (BLK) rows of the timing chart are pulses indicated as a reference and are not pulses output from pins.
FRP polarity is not specified for each line and field.
LCX009 + (DCX501), DCX501 + (LCX009) and DCX501 + (LCX005) modes: VCK(A) output
(In DCX501 + (LCX005) mode the polarity is inverted. (VCK(3)(A) and VCK(4)(A)))
LCX027 + (DCX501) and DCX501 + (LCX027) modes: VCK(B) output
LCX009/027 drive pulses: HST2, EN2, CLR, VCK3, VCK4, VST and BLK
DCX501 drive pulses: VCK1, VCK2, HST1, EN1, PCG and VST (HST1, EN1, PCG and VST output inverted pulses XHST1, XEN1, XPCG and XVST.)

Vertical Direction Timing Chart — PAL-WIDE
LCX009 + (DCX501), LCX027 + (DCX501),
DCX501 + (LCX009), DCX501 + (LCX027), DCX501 + (LCX005)



Note) The first (SYNC) and second (BLK) rows of the timing chart are pulses indicated as a reference and are not pulses output from pins.
FRP polarity is not specified for each line and field.
LCX009 + (DCX501), DCX501 + (LCX009) and DCX501 + (LCX005) modes: VCK(A) output
(In DCX501 + (LCX005) mode the polarity is inverted. (VCK(3)(A) and VCK(4)(A)))
LCX027 + (DCX501) and DCX501 + (LCX027) modes: VCK(B) output
LCX009/027 drive pulses: HST2, EN2, CLR, VCK3, VCK4, VST and BLK
DCX501 drive pulses: VCK1, VCK2, HST1, EN1, PCG and VST (HST1, EN1, PCG and VST output inverted pulses XHST1, XEN1, XPCG and XVST.)

Application Circuit (NTSC/PAL, COMP input)



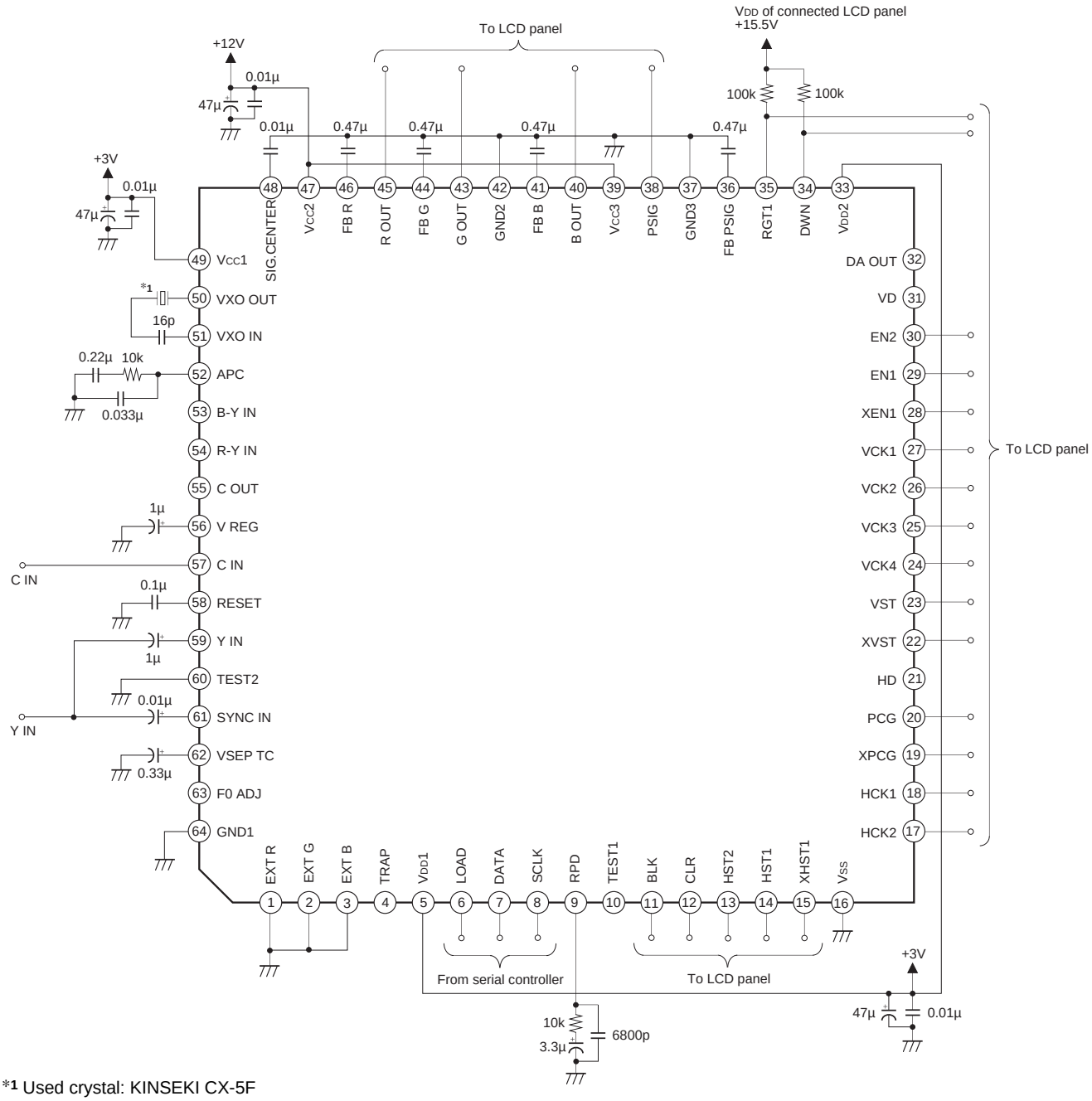
*1 Used crystal: KINSEKI CX-5F
Frequency deviation: within ±30ppm,
frequency temperature characteristics: within ±30ppm,
load capacity: 16pF
NTSC: 3.579545MHz
PAL: 4.433619MHz

*2 Resistance value variation: ±2%,
temperature coefficient: ±200ppm or less

*3 Trap (TDK)
NTSC: NLT4532-S3R6B
PAL: NLT4532-S4R4

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit (NTSC/PAL, Y/C input)



*1 Used crystal: KINSEKI CX-5F

Frequency deviation: within ±30ppm,

frequency temperature characteristics: within ±30ppm,

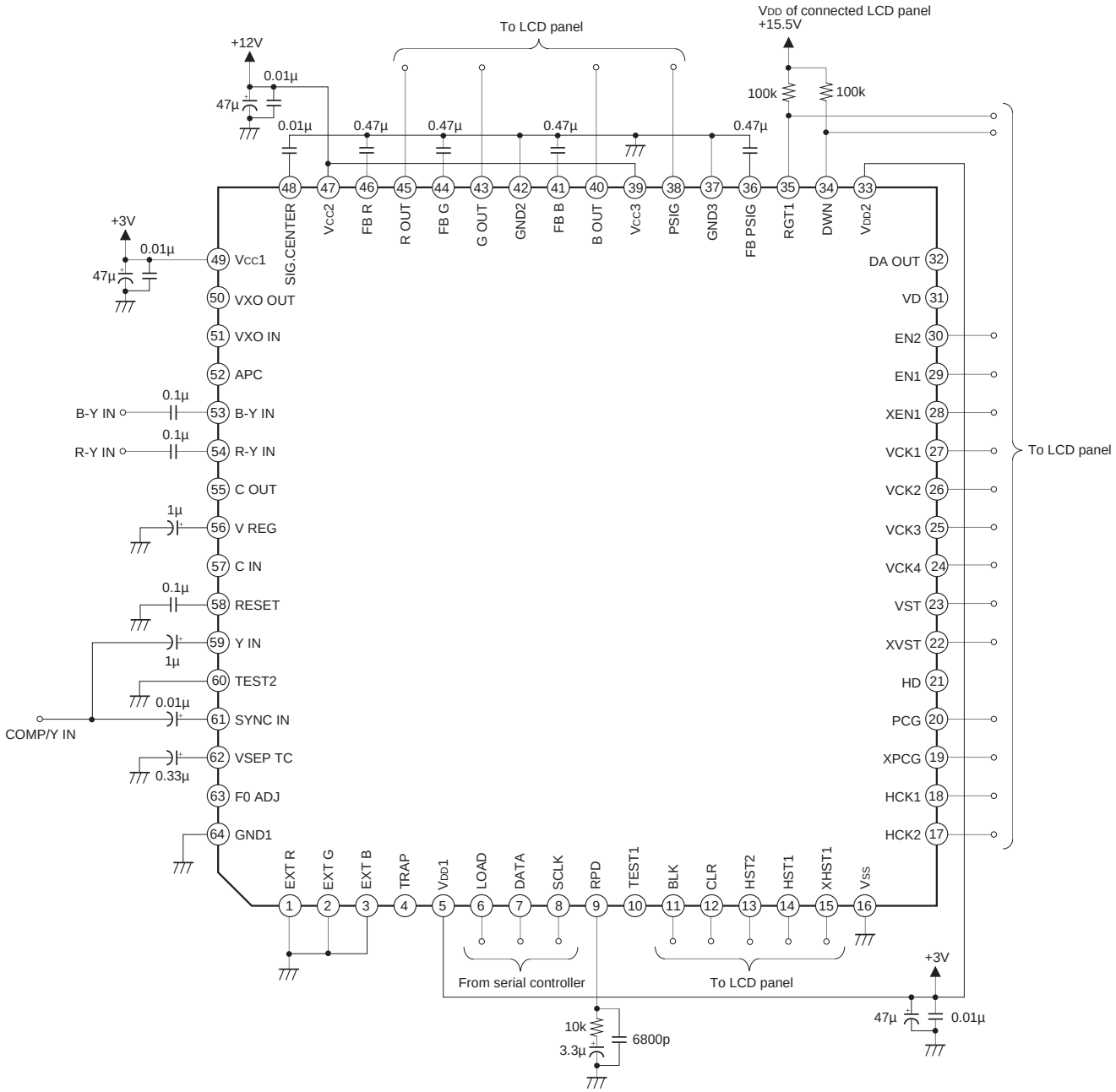
load capacity: 16pF

NTSC: 3.579545MHz

PAL: 4.433619MHz

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

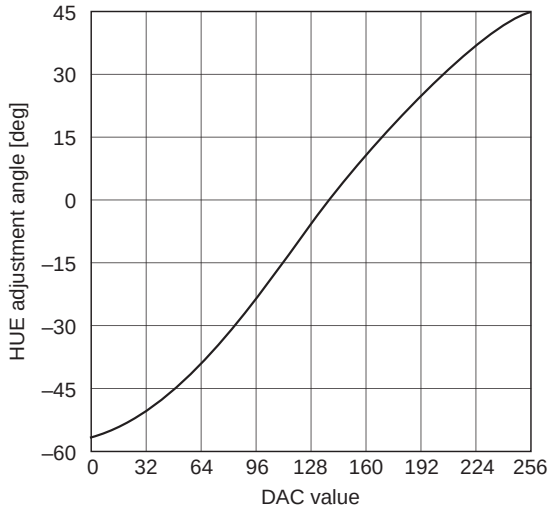
Application Circuit (NTSC/PAL, Y/color difference input)



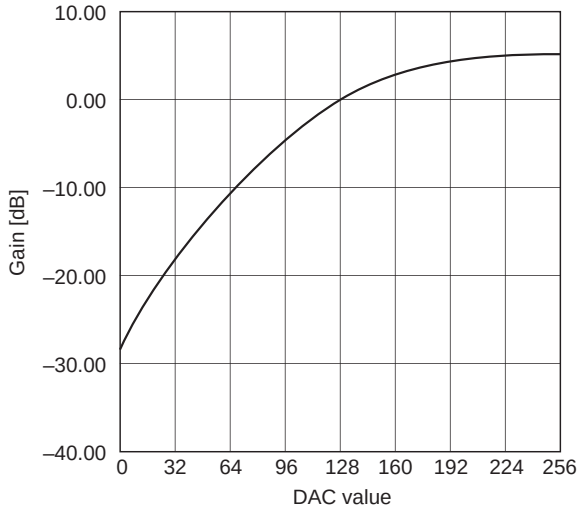
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics

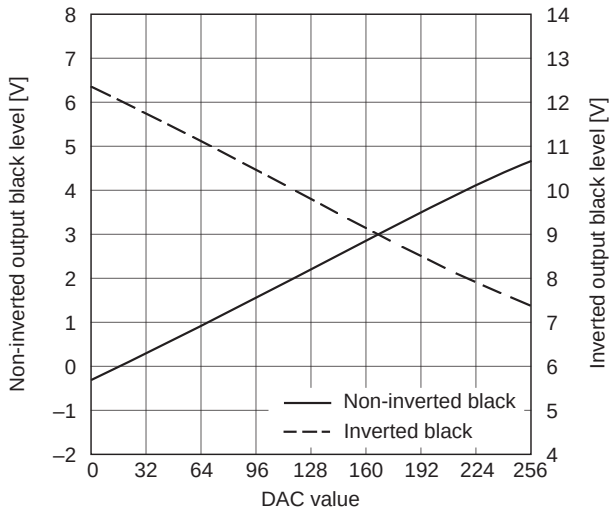
HUE adjustment characteristics



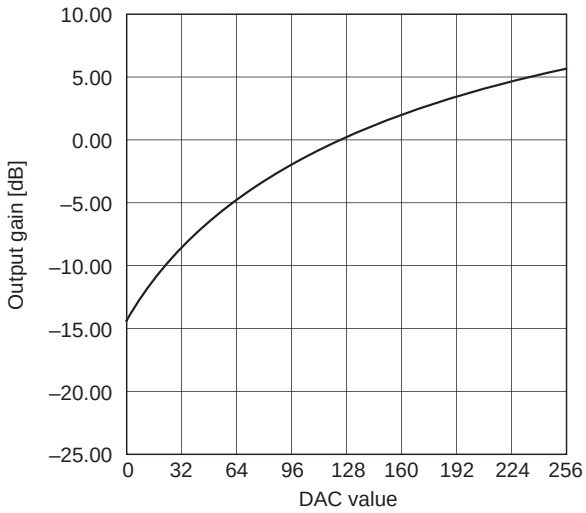
COLOR adjustment characteristics



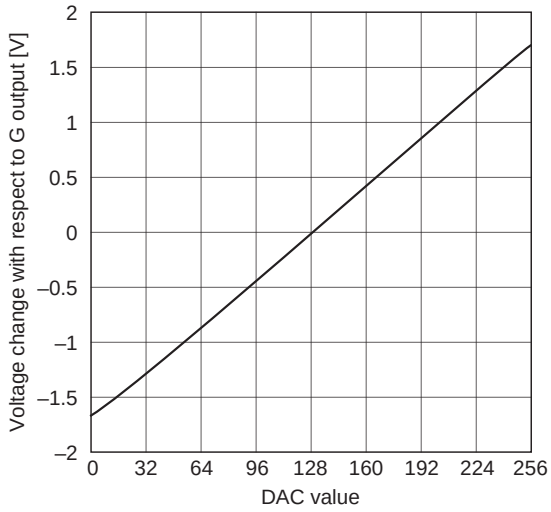
BRIGHT adjustment characteristics



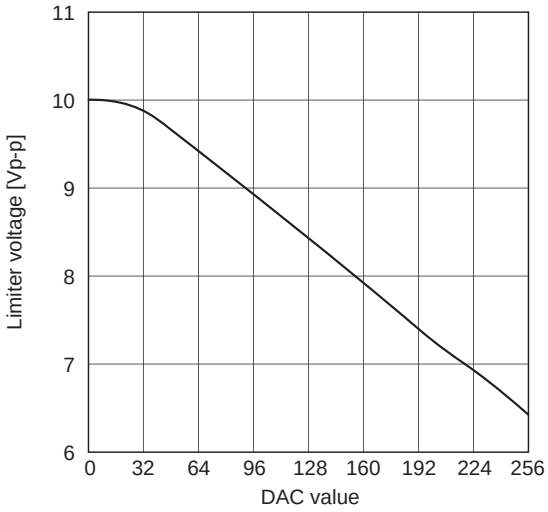
CONTRAST adjustment characteristics



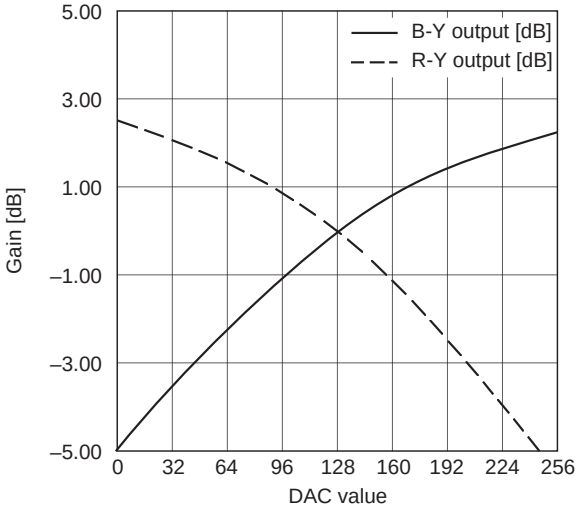
SUB-BRIGHT adjustment characteristics



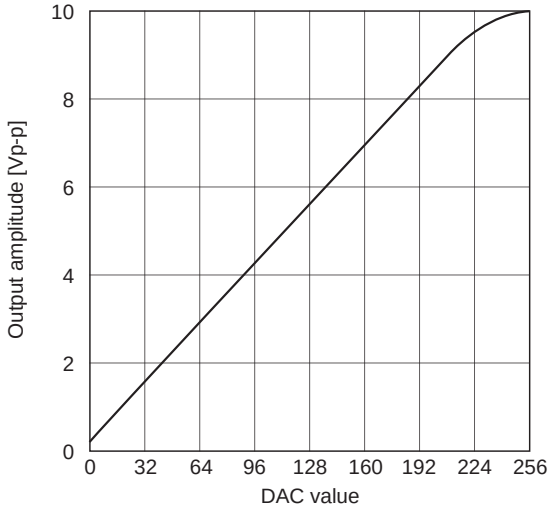
Black limiter control characteristics



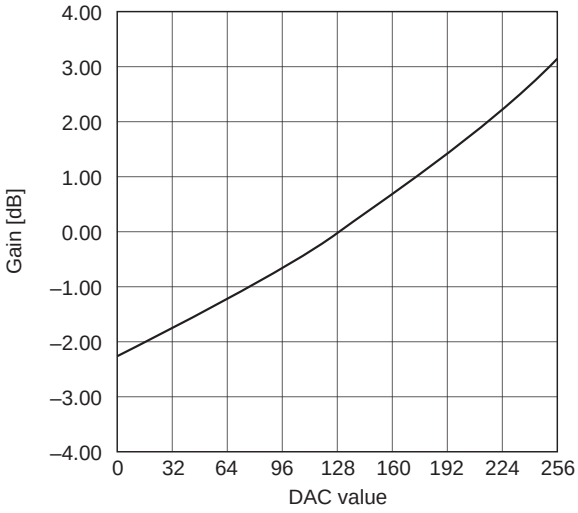
Color difference balance adjustment



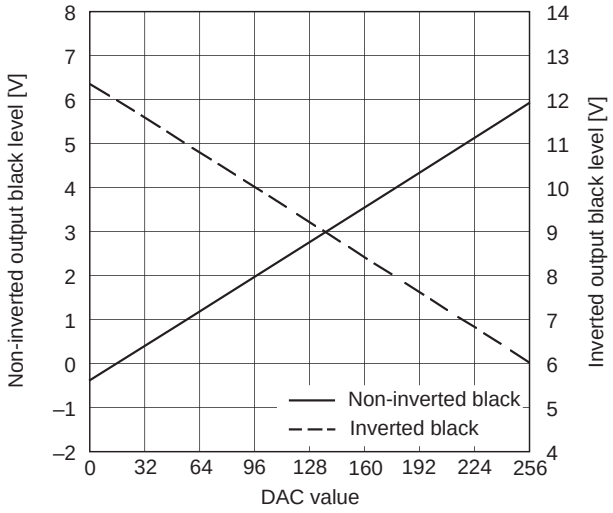
PSIG adjustment characteristics



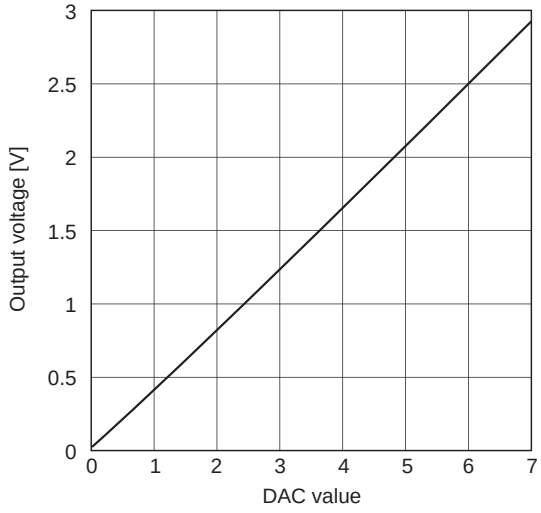
SUB-CONTRAST adjustment characteristics (γ1 = γ2 = 0)



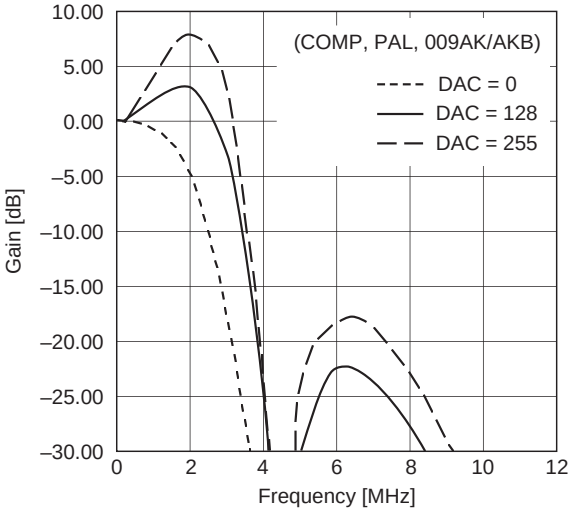
USER-BRIGHT adjustment characteristics



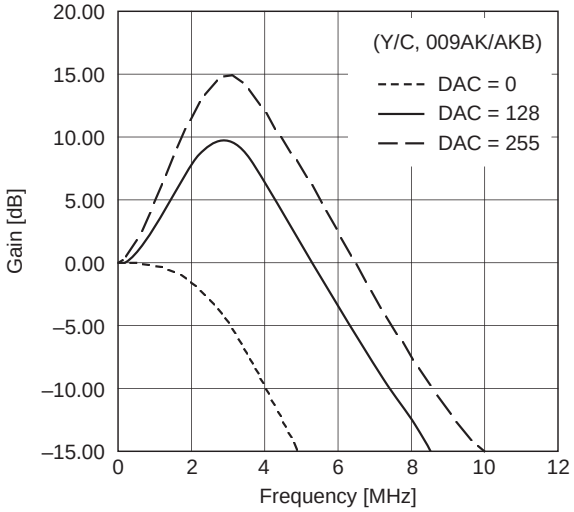
DA OUT output adjustment characteristics



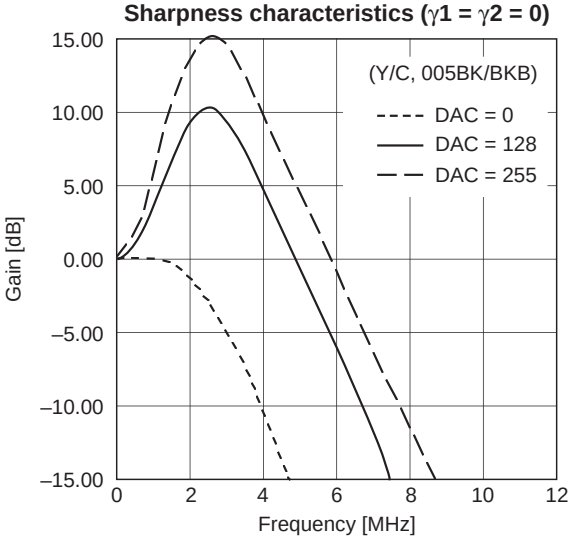
Sharpness characteristics (γ1 = γ2 = 0)



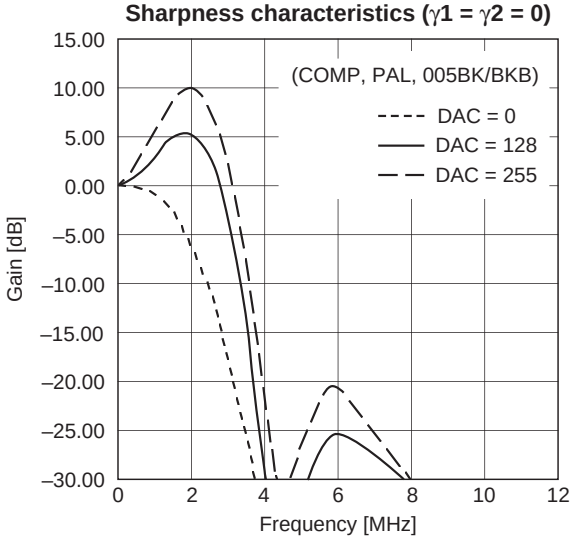
Sharpness characteristics (γ1 = γ2 = 0)



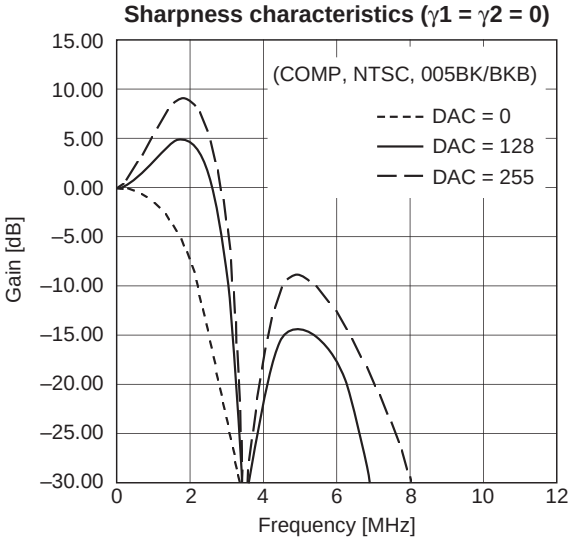
Sharpness characteristics (γ1 = γ2 = 0)



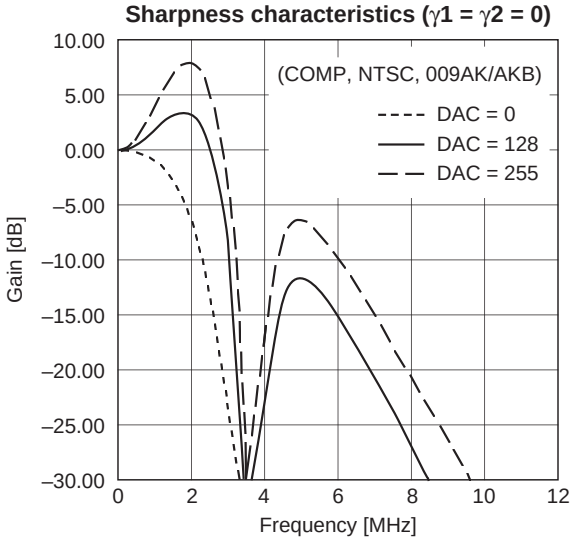
Sharpness characteristics (γ1 = γ2 = 0)



Sharpness characteristics (γ1 = γ2 = 0)



Sharpness characteristics (γ1 = γ2 = 0)



Notes on Operation

The CXA3017R contains digital circuits, so the set board pattern must be designed in consideration of undesired radiation, interference to analog circuits, etc. Care should also be taken for the following items when designing the pattern.

- Make the IC power supply and GND patterns as plain as possible. In particular, GND and Vss should not be separated and should be connected to the same GND pattern as close to the pins as possible.
- Connect the by-pass capacitors between the power supplies and GND as close to the pins as possible.
- The trap connected to Pin 4 should be located as close to the pin as possible. Also, do not pass other signal lines close to this pin or the connected trap.
- The wiring for the crystal and capacitor connected to Pins 50 and 51 should be as short as possible in order to prevent floating capacitance. Do not pass other signal lines close to these pins and wiring in order to prevent interference such as color unevenness. In addition, the APC pull-in characteristics vary significantly according to the characteristics of the used crystal and the wiring pattern, so be sure to thoroughly investigate these items before using the set.
- The resistor connected to Pin 63 should be located as close to the pin as possible. Also, do not pass other signal lines close to this pin.

The composite/Y signal and the external R-Y and B-Y signals are clamped at the inputs using the capacitors connected to the input pins, so these signals should be input at sufficiently low impedance. The C signal is received by the internal capacitor, so this signal should be input at low impedance after applying an appropriate external DC bias.

The smoothing capacitor of the DC level control feedback circuit in the output block should have a leak current with a small absolute value and variance.

A thorough study of the external buffer for PSIG output should be made before deciding on a circuit to ascertain that it sufficiently brings out the characteristics of the LCD panel.

If this IC is used in connection with a circuit other than an LCD, it may cause that circuit to malfunction depending on the order in which power is supplied to the circuits. Thoroughly study the consequences of using this IC with other circuits before deciding on its use.

Since this IC utilizes a C-MOS structure, it may latch up due to excessive noise or power surge greater than the maximum rating of the I/O pins, or due to interface with the power supply of another circuit, or due to the order in which power is supplied to circuits. Be sure to take measures against the possibility of latch up.

Do not apply a voltage higher than V_{DD} or lower than Vss to I/O pins.

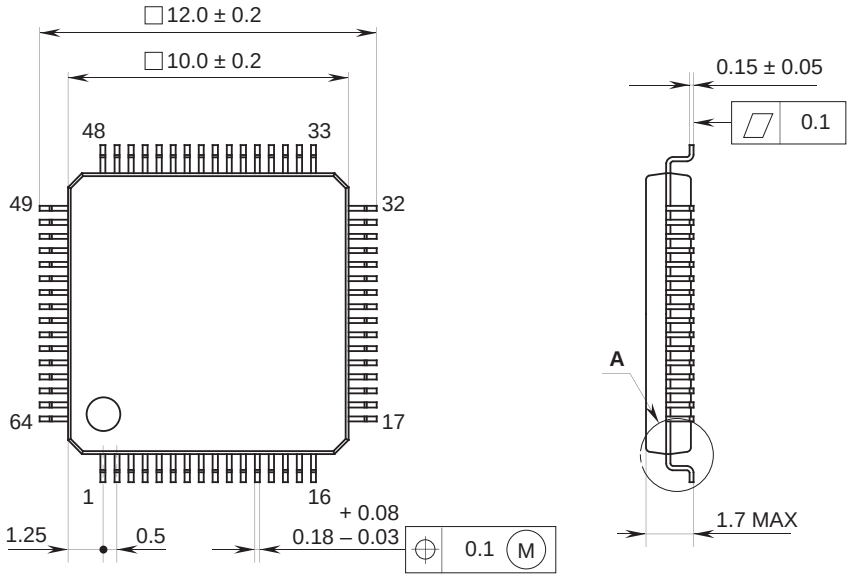
Do not use this IC under operating conditions other than those given.

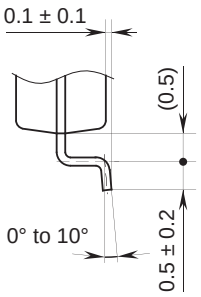
Absolute maximum rating values should not be exceeded even momentarily. Exceeding ratings may damage the device, leading to eventual breakdown.

This IC has a MOS structure which is easily damaged by static electricity, so thorough measures should be taken to prevent electrostatic discharge.

Package Outline Unit: mm

64PIN LQFP (PLASTIC)





DETAIL **A**

SONY CODE	LQFP-64P-L061
EIAJ CODE	LQFP064-P-1010-AY
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.3g