DATA SHEET

PCF8563
Real-time clock/calendar

Objective specification
File under Integrated Circuits, IC16

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Philips
Semiconductors

PHILIPS

Real-time clock/calendar PCF8563

FEATURES

- Provides year, month, day, weekday, hours, minutes, seconds based on 32.768 kHz quartz crystal
- Century flag
- Wide clock operating voltage: 1.0 - 5.5 V
- Low back-up current typical 0.25 μA @ 3.0 V, 25 °C
- 400 kHz two-wire I²C interface (1.8 - 5.5 V)
- Programmable clock output for peripheral devices (32.768 kHz, 1024 Hz, 32 Hz, 1 Hz)
- Alarm and timer functions
- Low-voltage detector
- Integrated oscillator capacitor
- Internal power-on reset
- I²C slave address: read A3h, write A2h
- Open drain interrupt pin.

GENERAL DESCRIPTION

The PCF8563 is a CMOS real-time clock/calendar optimized for low power consumption. A programmable clock output, interrupt output and voltage low detector are also provided. All address and data are transferred serially via a two-line bidirectional I²C bus. Maximum bus speed is 400 kbit/sec. The built-in word address register is incremented automatically after each written or read data byte.

APPLICATIONS

- Mobile telephones
- Portable instruments
- Fax machines
- Battery powered products.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	Supply voltage operating mode	I²C bus active –40 to +85 °C	1.8	5.5	V
		Clock operating, 25 °C	1.0	5.5	V
I_{DD}	Supply current (Timer and CLKOUT disabled)	f_{SCL} = 100 kHz	–	200	μA
		f_{SCL} = 400 kHz	–	800	μA
		f_{SCL} = 0 Hz: V_{DD} = 5 V, 25 °C	–	1.0	μA
		f_{SCL} = 0 Hz: V_{DD} = 2 V, 25 °C	–	0.75	μA
T_{AMB}	Operating ambient temperature		–40	+85	°C
T_{STG}	Storage temperature		–55	+125	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8563P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCF8563T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

BLOCK DIAGRAM

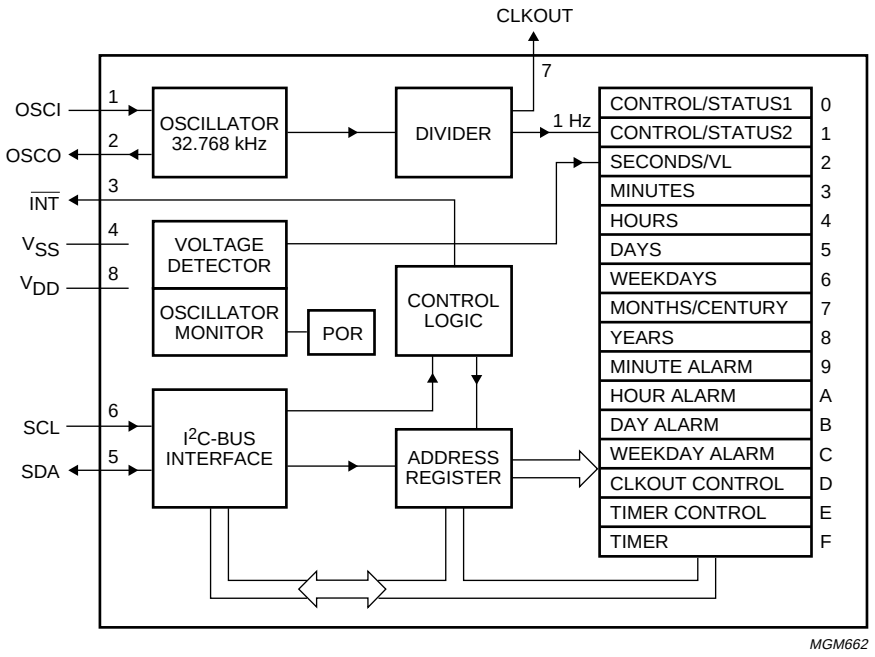


Fig.1 Block diagram PCF8563 real-time clock/calendar.

PINNING INFORMATION

Pin description

SYMBOL	PIN	DESCRIPTION
OSCI	1	Oscillator input
OSCO	2	Oscillator output
$\overline{INT}$	3	Open drain interrupt output (active LOW)
V_{SS}	4	Ground
SDA	5	Serial data I/O
SCL	6	Serial clock input
CLKOUT	7	Clock output
V_{DD}	8	Positive supply

Pinning

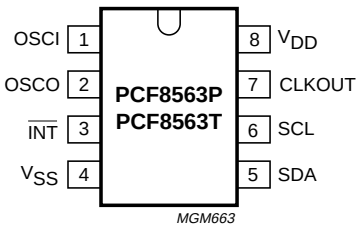


Fig.2 Pinning.

FUNCTIONAL DESCRIPTION

The PCF8563 contains sixteen 8-bit registers with an auto-incrementing address register, an on-chip 32.768 kHz oscillator with one integrated capacitor, a frequency divider which provides the source clock for the real time clock (RTC), a programmable clock output, a timer, an alarm, a voltage-low detector and a 400 kHz I^2C bus interface.

All 16 registers are designed as addressable 8-bit parallel registers although not all bits are implemented. The first two registers (memory address 00, 01) are used as control and/or status registers. The memory addresses 02 through 08 are used as counters for the clock function (seconds up to year counters). Address locations 09 through 0C contain alarm registers which define the conditions for an alarm. Address 0D controls the CLKOUT output frequency. 0E and 0F are the timer control and timer registers, respectively.

The seconds, minutes, hours, days, weekdays, months, years as well as the minute alarm, hour alarm, day alarm and weekday alarm registers are all coded in BCD format.

When one of the RTC registers is read the contents of all counters are frozen. Therefore, faulty reading of the clock/calendar during a carry condition is prevented.

Alarm function modes

By clearing the MSB of one or more of the alarm registers (AE = ‘Alarm Enable’), the corresponding alarm condition(s) will be active. In this way an alarm can be generated from once per minute up to once per week. The alarm condition sets the alarm flag, AF. The asserted AF can be used to generate an interrupt ($\overline{INT}$). The AF may only be cleared by software.

Timer

The 8-bit countdown timer at address 0F is controlled by the timer control register at address 0E. The timer control register determines one of 4 source clock frequencies for the timer (4096 Hz, 64 Hz, 1 Hz, or $^1/_{60}$ Hz), and enables/disables the timer. The timer counts down from a software-loaded 8-bit binary value. At the end of every countdown, the timer sets the timer flag TF. The TF may only be cleared by software. The asserted TF can be used to generate an interrupt ($\overline{INT}$). The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal which follows the condition of TF. TI/TP is used to control this mode selection. When reading the timer, the current countdown value is returned.

CLKOUT output

A programmable square wave is available at the CLKOUT pin. Operation is controlled by the CLKOUT register at address 0D. Frequencies of 32.768 kHz (default), 1024 Hz, 32 Hz and 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator. CLKOUT is a push-pull output and enabled at power on. If disabled it becomes logic 0.

Reset

The PCF8563 includes an internal reset circuit which is active whenever the oscillator is stopped. In the reset state the I^2C bus logic is initialized and all registers, including the address pointer, are cleared with the exception of bits FE, VL, TD1, TD0, TESTC and AE bits which are set to 1.

Voltage low detector & clock monitor

The PCF8563 has an on-chip voltage low detector. When V_{DD} drops below V_{LOW} the ‘Voltage Low’ (VL, bit 7 in the seconds register) is set to indicate that the integrity of the clock information is no longer guaranteed. The VL flag can only be cleared by software.

Register organization

Bit positions labelled as ‘x’ are not implemented, those labelled with ‘0’ should always be written with 0.

ADDRESS	FUNCTION	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00	Control/status 1	TEST1	0	STOP	0	TESTC	0	0	0
01	Control/status 2	0	0	0	TI/TP	AF	TF	AIE	TIE
02	Seconds	VL	4	2	1	8	4	2	1
03	Minutes	x	4	2	1	8	4	2	1
04	Hours	x	x	2	1	8	4	2	1
05	Days	x	x	2	1	8	4	2	1
06	Weekdays	x	x	x	x	x	4	2	1
07	Months/Century	C	x	x	1	8	4	2	1
08	Years	8	4	2	1	8	4	2	1
09	Minute alarm	AE	4	2	1	8	4	2	1
0A	Hour alarm	AE	x	2	1	8	4	2	1
0B	Day alarm	AE	x	2	1	8	4	2	1
0C	Weekday alarm	AE	x	x	x	x	4	2	1
0D	CLKOUT frequency	FE	x	x	x	x	x	FD1	FD0
0E	Timer control	TE	x	x	x	x	x	TD1	TD0
0F	Timer	128	64	32	16	8	4	2	1

Bit assignments

BIT NO.	BIT NAME	BIT VALUE	DESCRIPTION
Control/Status 1		**Address 00**	
3	TESTC	0	Power on reset override facility is disabled. Set to 0 for normal operation.
		1	Power on reset override may be enabled.
5	STOP	0	RTC source clock runs.
		1	All RTC divider chain flip flops are asynchronously set to 0; the RTC clock is stopped (CLKOUT at 32.768 kHz is still available)
7	TEST1	0	Normal mode.
		1	EXT_CLK test mode.
Control/Status 2		**Address 01**	
TIE & AIE		These bits activate or deactivate the generation of an interrupt when TF or AF is asserted, respectively. The interrupt is the logical OR of these two conditions when both AIE and TIE are set	
0	TIE	0	Timer interrupt disabled
		1	Timer interrupt enabled
1	AIE	0	Alarm interrupt disabled
		1	Alarm interrupt enabled

BIT NO.	BIT NAME	BIT VALUE	DESCRIPTION
TF & AF		When an alarm occurs, AF is set to 1. Similarly, at the end of a timer countdown, TF is set to 1.These bits maintain their value until overwritten by software. If both timer and alarm interrupts are required in the application, the source of the interrupt can be determined by reading these bits. To prevent one flag being overwritten while clearing another a logic AND is performed during a write access.	
2	TF	0 (READ)	Timer flag inactive.
		1 (READ)	Timer flag active.
		0 (WRITE)	Timer flag is cleared.
		1 (WRITE)	Timer flag remains unchanged.
3	AF	0 (READ)	Alarm flag inactive.
		1 (READ)	Alarm flag active.
		0 (WRITE)	Alarm flag is cleared.
		1 (WRITE)	Alarm flag remains unchanged.
4	TI/TP	0	$\overline{INT}$ is active when TF is active (subject to the status of TIE).
		1	$\overline{INT}$ pulses active according to table 1(subject to the status of TIE). Note that if AF and AIE are active then $\overline{INT}$ will be permanently active.
Seconds & VL		**Address 02**	
6..0	Seconds	00 - 59	This register holds the current seconds coded in BCD format. Example: seconds register contains ‘x1011001’ = 59 seconds.
7	VL	0	Clock integrity is guaranteed.
		1	Integrity of the clock information is no longer guaranteed.
Minutes		**Address 03**	
6..0	Minutes	00 - 59	This register holds the current minutes coded in BCD format.
Hours		**Address 04**	
5..0	Hours	00 - 23	This register holds the current hours coded in BCD format.
Days		**Address 05**	
5..0	Days(1)	01 - 31	This register holds the current day coded in BCD format.
Weekdays		**Address 06**	
2..0	Weekdays(2)	0 - 6	This register holds the current weekday coded in BCD format, see table 4.
Months & Century		**Address 07**	
4..0	Month	01 - 12	This register holds the current month coded in BCD format, see table 5.
7	Century(2)	0	Indicates the century is 20xx.
		1	Indicates the century is 19xx.
		This bit is toggled when the years register overflows from 99 to 00.	
Years		**Address 08**	
7..0	Years	00 - 99	This register holds the current year coded in BCD format.

BIT NO.	BIT NAME	BIT VALUE	DESCRIPTION
Alarm registers		**Address 09 to 0C**	
		When one or more of these registers is loaded with a valid minute, hour, day or weekday and its corresponding ‘Alarm Enable’ (AE) is ‘0’, then that information will be compared with the current minute, hour, day and weekday. When all enabled comparisons first match, the ‘Alarm Flag’ (AF) is set. AF will remain set until cleared by software. Once AF has been cleared it will only be set again when the time increments to match the alarm condition once more. Alarm registers which have their ‘Alarm Enable’ bit at ‘1’ will be ignored.	
Alarm: Minute		**Address 09**	
6..0	Alarm minutes	00 - 59	This register holds the minute alarm information coded in BCD format.
7	AE	0	Minute alarm is enabled.
		1	Minute alarm is disabled.
Alarm: Hour		**Address 0A**	
5..0	Alarm hours	00 - 23	This register holds the hour alarm information coded in BCD format.
7	AE	0	Hour alarm is enabled.
		1	Hour alarm is disabled.
Alarm: Day		**Address 0B**	
5..0	Alarm days	01 - 31	This register holds the day alarm information coded in BCD format.
7	AE	0	Day alarm is enabled.
		1	Day alarm is disabled.
Alarm: Weekday		**Address 0C**	
2..0	Alarm weekdays	00 - 00	This register holds the weekday alarm information coded in BCD format.
7	AE	0	Weekday alarm is enabled.
		1	Weekday alarm is disabled.
CLKOUT frequency		**Address 0D**	
1..0	FD1, FD0		These bits control the frequency output on the CLKOUT pin, see table 2.
7	FE	0	The CLKOUT output is inhibited and CLKOUT output is set to logic 0.
		1	The CLKOUT output is activated.

BIT NO.	BIT NAME	BIT VALUE	DESCRIPTION
Countdown Timer		**Address 0E and 0F**	
			The timer register is an 8-bit binary countdown timer. It is enabled and disabled via the timer control register bit TE. The source clock for the timer is also selected by the timer control register. Other timer properties such as interrupt generation are controlled via control/status 2 registers. For accurate read back of the countdown value, the I^2C clock (SDA) must be operating at a frequency of at least twice the selected timer clock.
Timer control		**Address 0E**	
1..0	TD1, TD0		Timer source clock frequency select. These bits determine the source clock for the countdown timer, see table 3. When not in use, TD1 & TD0 should be set to 1/60 Hz for power saving.
7	TE	0	Timer is disabled.
		1	Timer is enabled.
Timer countdown value		**Address 0F**	
7..0	Timer	00..FF	Countdown value, n. $CountdownPeriod = \frac{n}{SourceClockFrequency}$

Notes

1. The PCF8563 compensates for leap years by adding a 29th day to February if the year counter contains a value which is exactly divisible by 4, including the year 00.
2. These bits may be re-assigned by the user.

Table 1 $\overline{INT}$ OPERATION (TI/TP=1)

$\overline{INT}$ PERIOD		
SOURCE CLOCK	**n = 1**	**n > 1**
4096 Hz	1/8192 s	1/4096 s
64 Hz	1/128 s	1/64 s
1 Hz	1/64 s	1/64 s
1/60 Hz	1/64 s	1/64 s

Notes

1. n = Loaded countdown value.
   Timer stopped when n = 0.
2. TF and $\overline{INT}$ become active simultaneously.

Table 2 FD1, FD0: CLKOUT frequency selection.

FD1	FD0	CLKOUT FREQUENCY
0	0	32.768 kHz
0	1	1024 Hz
1	0	32 Hz
1	1	1 Hz

Table 3 TD1, TD0: Timer frequency selection.

TD1	TD0	TIMER SOURCE CLOCK FREQUENCY
0	0	4096 Hz
0	1	64 Hz
1	0	1 Hz
1	1	1/60 Hz

Table 4 Weekday assignments.

DAY	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Sunday	x	x	x	x	x	0	0	0
Monday	x	x	x	x	x	0	0	1
Tuesday	x	x	x	x	x	0	1	0
Wednesday	x	x	x	x	x	0	1	1
Thursday	x	x	x	x	x	1	0	0
Friday	x	x	x	x	x	1	0	1
Saturday	x	x	x	x	x	1	1	0

Table 5 Month assignments

MONTH	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
January	C	x	x	0	0	0	0	1
February	C	x	x	0	0	0	1	0
March	C	x	x	0	0	0	1	1
April	C	x	x	0	0	1	0	0
May	C	x	x	0	0	1	0	1
June	C	x	x	0	0	1	1	0
July	C	x	x	0	0	1	1	1
August	C	x	x	0	1	0	0	0
September	C	x	x	0	1	0	0	1
October	C	x	x	1	0	0	0	0
November	C	x	x	1	0	0	0	1
December	C	x	x	1	0	0	1	0

EXT_CLK test mode.

A test mode is available which allows for on board testing. In such a mode it is possible to set up test conditions and control the operation of the RTC.

The test mode is entered by setting the TEST1 bit in Control/Status1. The CLKOUT pin then becomes an input. The test mode replaces the internal 64 Hz signal with that applied to the CLKOUT pin. Every 64 positive edges applied to CLKOUT will then generate an increment of one second.

The signal applied to the CLKOUT pin should have a minimum pulse width of 300ns and a minimum period of 1000ns. The internal 64 Hz clock, now sourced from CLKOUT, is divide down to 1 Hz by a 2^6 divide chain called a pre-scaler. The pre-scaler can be set into a known state by using the STOP bit. When the STOP bit is set, the pre-scaler is reset to 0. (STOP must be cleared before the pre-scaler can operate again).

From a STOP condition, the first 1 second increment will take place after 32 positive edges on CLKOUT. Thereafter, every 64 positive edges will cause a 1 second increment.

Note. Entry into EXT_CLK test mode is not synchronized to the internal 64 Hz clock. When entering the test mode, no assumption as to the state of the pre-scaler can be made.

OPERATION EXAMPLE.

1. Set EXT_CLK test mode (Bit7 Control/Status1 = 1).
2. Set STOP (Bit5 Control/Status1 = 1).
3. Clear STOP (Bit5 Control/Status1 = 0).
4. Set time registers to desired value.
5. Apply 32 clock pulses to CLKOUT.
6. Read time registers to see the first change.
7. Apply 64 clock pulses to CLKOUT.
8. Read time registers to see the second change.

Repeat 7 & 8 for additional increments.

Power On Reset override.

The POR duration is directly related to the crystal oscillator start-up time. Due to the long start-up times experienced by these types of circuits, a mechanism has been built in to disable the POR and hence speed up on board test of the device. The setting of this mode requires that the I^2C pins, SDA and SCL, be toggled in a specific order as shown in figure 3. All timings are required minimums.

Once the override mode has been entered, the chip immediately stops being reset and normal operation may commence i.e. entry into the EXT_CLK test mode via I^2C access. The override mode may be cleared by writing a 0 to TESTC. TESTC must be set to 1 before re-entry into the override mode is possible. Setting TESTC to 0 during normal operation has no effect except to prevent entry into the POR override mode.

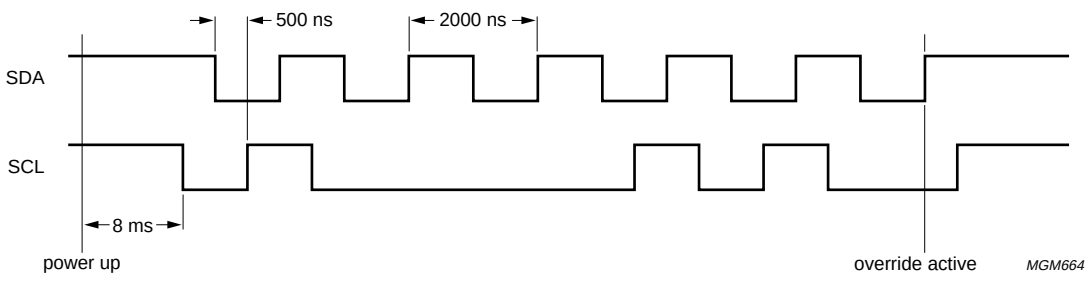


Fig.3 POR override sequence.

LIMITING VALUES.

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+6.5	V
V_I	input voltage	–0.5	V_{DD} + 0.5	V
I_I	DC input current	–10	+10	mA
I_O	DC output current	–10	+10	mA
I_{DD}	Supply current	–50	+50	mA
I_{SS}	Supply current	–50	+50	mA
P_{TOT}	total power dissipation	–	300	mW
T_{AMB}	operating ambient temperature	–40	+85	°C
T_{STG}	storage temperature	–65	+150	°C

CHARACTERISTICS OF THE I²C-BUS.

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

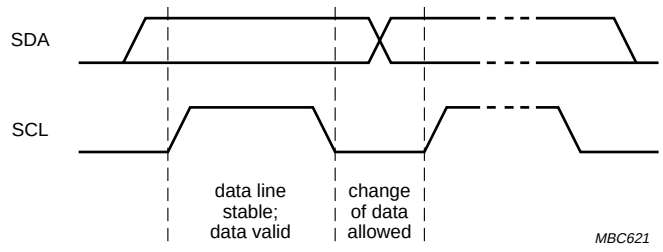


Fig.4 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

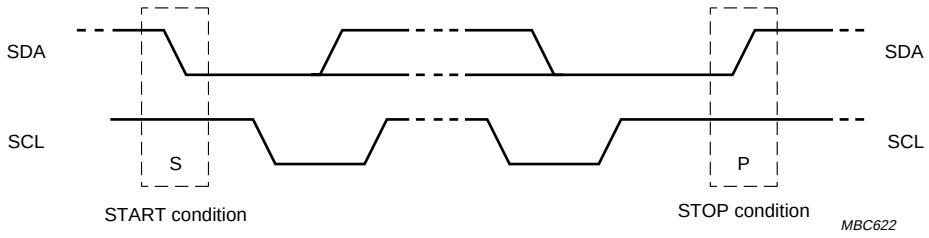


Fig.5 Definition of start and stop conditions.

System configuration (see Fig.6)

A device generating a message is a ‘transmitter’, a device receiving a message is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’.

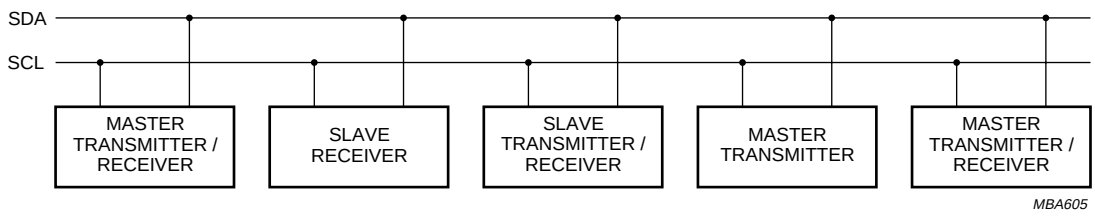


Fig.6 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

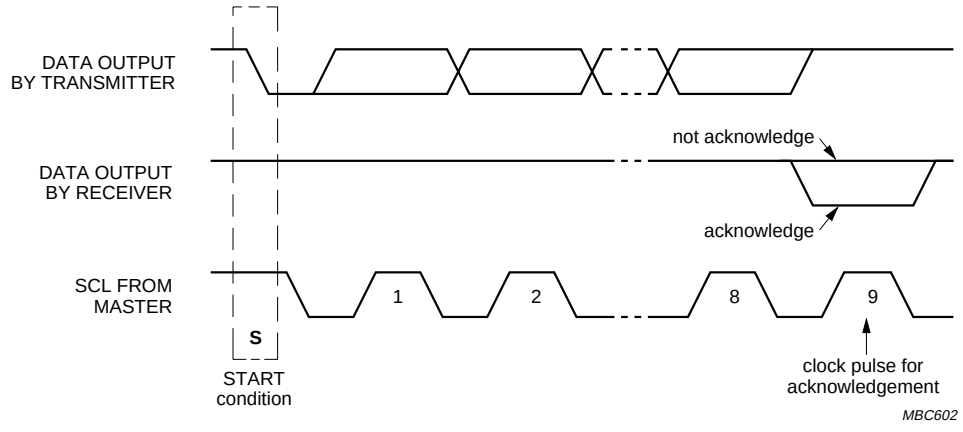


Fig.7 Acknowledgment on the I^2C-bus.

I²C-BUS PROTOCOL.

Addressing

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure.

The PCF8563 acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line.

The PCF8563 slave address is shown in Fig.8.

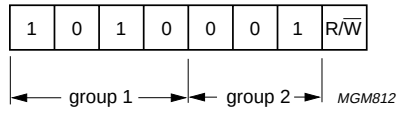


Fig.8 Slave address.

Clock/calendar READ/WRITE cycles

The I²C-bus configuration for the different PCF8563 READ and WRITE cycles is shown below. The word address is four bit value that defines which register is to be accessed next. The upper four bits of the word address are not used.

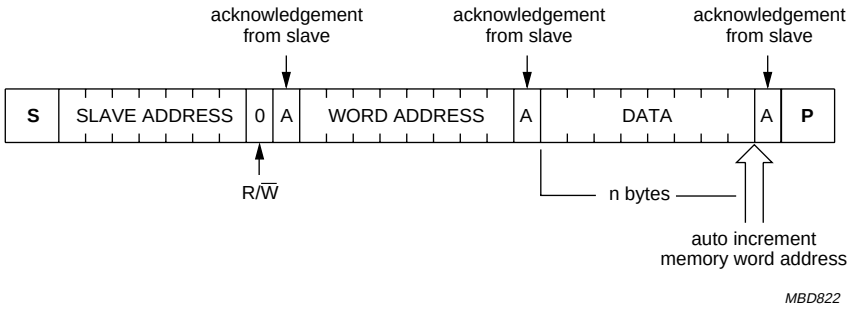


Fig.9 Master transmits to slave receiver (WRITE) mode.

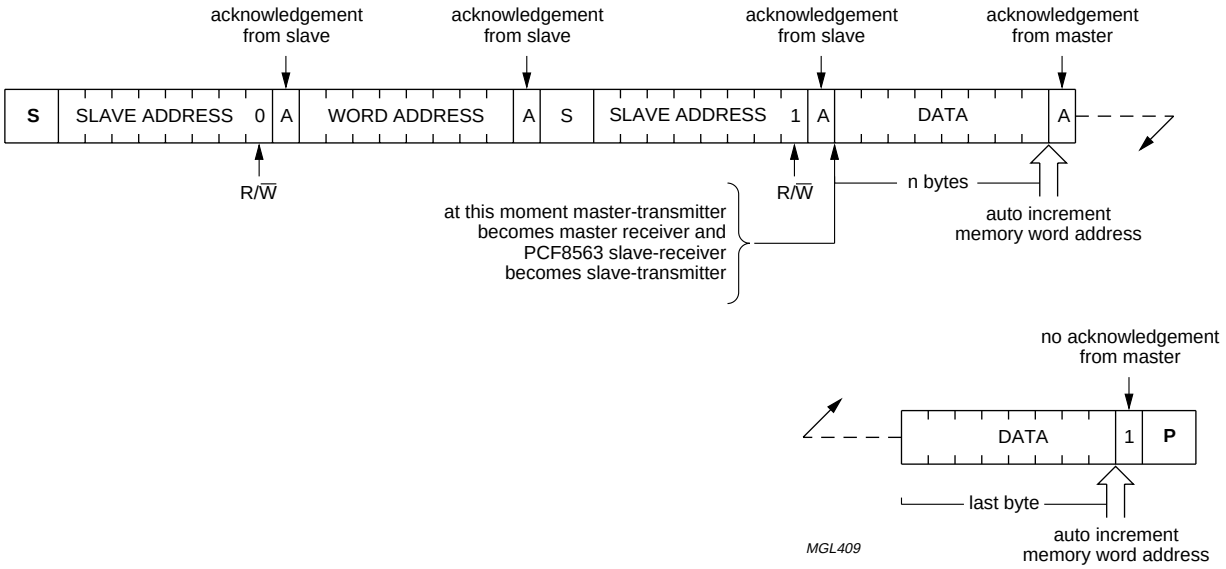


Fig.10 Master reads after setting word address (write word address; READ data).

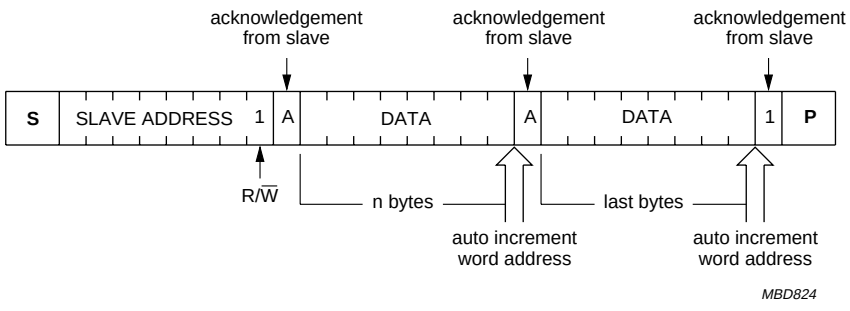


Fig.11 Master reads slave immediately after first byte (READ mode).

DC CHARACTERISTICS.

V_{DD} = 1.8 to 5.5 V; V_{SS} = 0 V; T_{AMB} = –40 to +85 °C; f_{OSC} = 32.768 kHz; quartz R_S = 40 kΩ, C_L = 8 pF unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage (1)	I^2C bus inactive, 25 °C	1.0	–	5.5	V
		400 kHz I^2C bus activity	1.8	–	5.5	V
	clock data integrity	25 °C	V_{LOW}	–	5.5	V
I_{DD}	supply current (2)	f_{SCL} = 400 kHz	–	–	800	µA
		f_{SCL} = 100 kHz	–	–	200	µA
		f_{SCL} = 0 Hz V_{DD} = 5.0 V 25 °C	–	0.3	1.0	µA
		f_{SCL} = 0 Hz V_{DD} = 2.0 V 25 °C	–	0.25	0.75	µA
Inputs						
V_{IL}	LOW level input voltage		V_{SS}	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage	$V_I = V_{DD}$ or V_{SS}	–1	–	1	µA
C_I	input capacitance	(note 3)	–	–	7	pF
Outputs						
$I_{OL(SDA)}$	SDA LOW output current	V_{OL} = 0.4 V, V_{DD} = 5 V	–3	–	–	mA
$I_{OL(\overline{INT})}$	$\overline{INT}$ LOW output current	V_{OL} = 0.4 V, V_{DD} = 5 V	–1	–	–	mA
$I_{OL(CLKOUT)}$	CLKOUT LOW output current	V_{OL} = 0.4 V, V_{DD} = 5 V	–1	–	–	mA
$I_{OH(CLKOUT)}$	CLKOUT HIGH output current	V_{OH} = 4.6 V, V_{DD} = 5 V	1	–	–	mA
I_{LO}	output leakage	$V_O = V_{DD}$ or V_{SS}	–1	–	1	µA
Voltage detector						
V_{LOW}	Low voltage detection	25 °C	–	0.9	1.0	V

Notes

1. When powering up the device, V_{DD} must exceed the specified minimum value by 300 mV to guarantee correct start-up of the oscillator.
2. CLKOUT disabled, (FE = 0). Timer source clock = $^1/_{60}$ Hz.
3. Tested on sample basis.

AC CHARACTERISTICS.

V_{DD} = 1.8 to 5.5 V; V_{SS} = 0 V; T_{AMB} = –40 to +85 °C; f_{OSC} = 32.768 kHz; quartz R_S = 40 kΩ, C_L = 8 pF unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator						
C_L	integrated load capacitance		19	25	31	pF
f/f_{OSC}	oscillator stability	for ΔV_{DD} = 200 mV; 25 °C	–	$2x10^{-7}$	–	–
Quartz crystal parameters (f = 32.768 kHz)						
R_s	series resistance		–	–	40	kΩ
C_L	parallel load capacitance		–	10	–	pF
C_T	trimmer capacitance		5	–	25	pF
CLKOUT output						
T_{CLKOUT}	CLKOUT duty cycle	note 1	–	50	–	%
Timing characteristics: I^2C-bus; notes 5 & 6						
f_{SCL}	SCL clock frequency	note 4	–	–	400	kHz
$t_{HD;STA}$	START condition hold time		0.6	–	–	µs
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	–	–	µs
t_{LOW}	SCL LOW time		1.3	–	–	µs
t_{HIGH}	SCL HIGH time		0.6	–	–	µs
t_r	SCL and SDA rise time		–	–	0.3	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
C_B	capacitive bus line load		–	–	400	pF
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;STO}$	set-up time for STOP condition		4.0	–	–	µs
t_{SW}	tolerable spike width on bus		–	–	50	ns

Notes

1. Unspecified for f_{CLKOUT} = 32.768 kHz.
2. All timing values are valid within the operating supply voltage at ambient temperature and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
3. A detailed description of the I^2C bus specification, with applications, is given in brochure “The I^2C bus and how to use it”. This brochure may be ordered using the code 9398 393 40011.
4. I^2C access time between two STARTs or between a START and a STOP condition to this device must be less than one second.

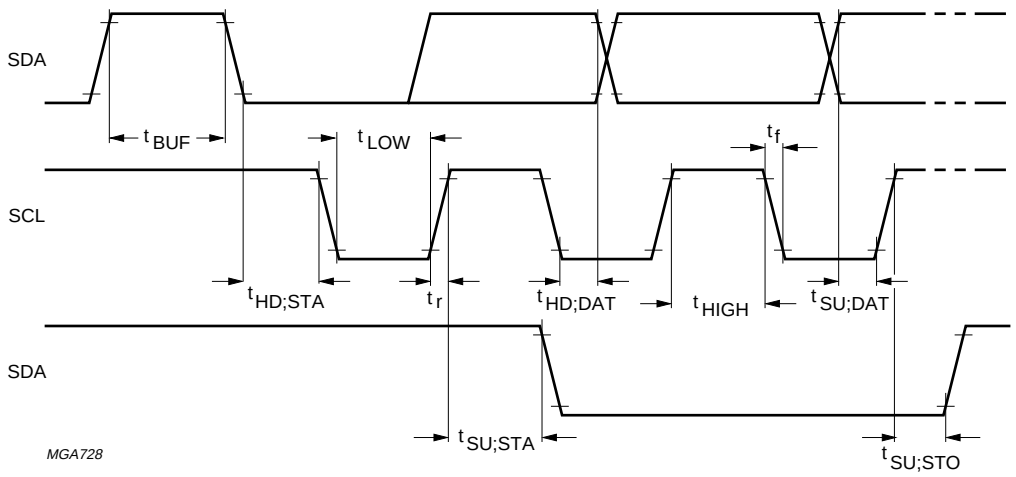


Fig.12 I²C-bus timing waveforms.

APPLICATION INFORMATION

Quartz frequency adjustment

METHOD 1: FIXED OSCI CAPACITOR

By evaluating the average capacitance necessary for the application layout a fixed capacitor can be used. The frequency is best measured via the 32.768 kHz signal available after power-on at the CLKOUT pin. The frequency tolerance depends on the quartz crystal tolerance, the capacitor tolerance and the device-to-device tolerance (on average $\pm 5 \times 10^{-6}$). Average deviations of ±5 minutes per year can be easily achieved.

METHOD 2: OSCI TRIMMER

Using the 32.768 kHz signal available after power-on at the CLKOUT pin fast setting of a trimmer is possible.

METHOD 3:

Direct measurement of OSCO out (accounting for test probe capacitance).

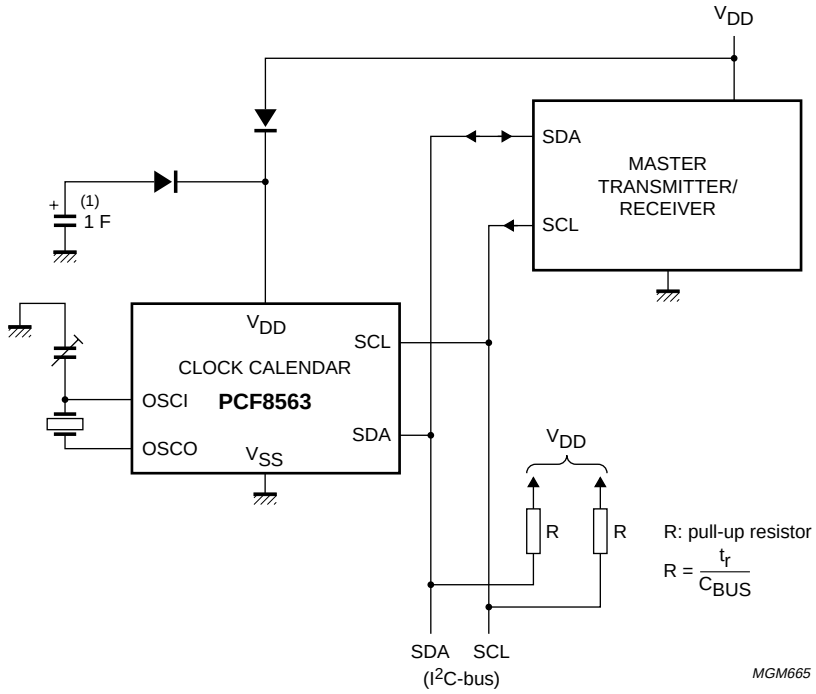
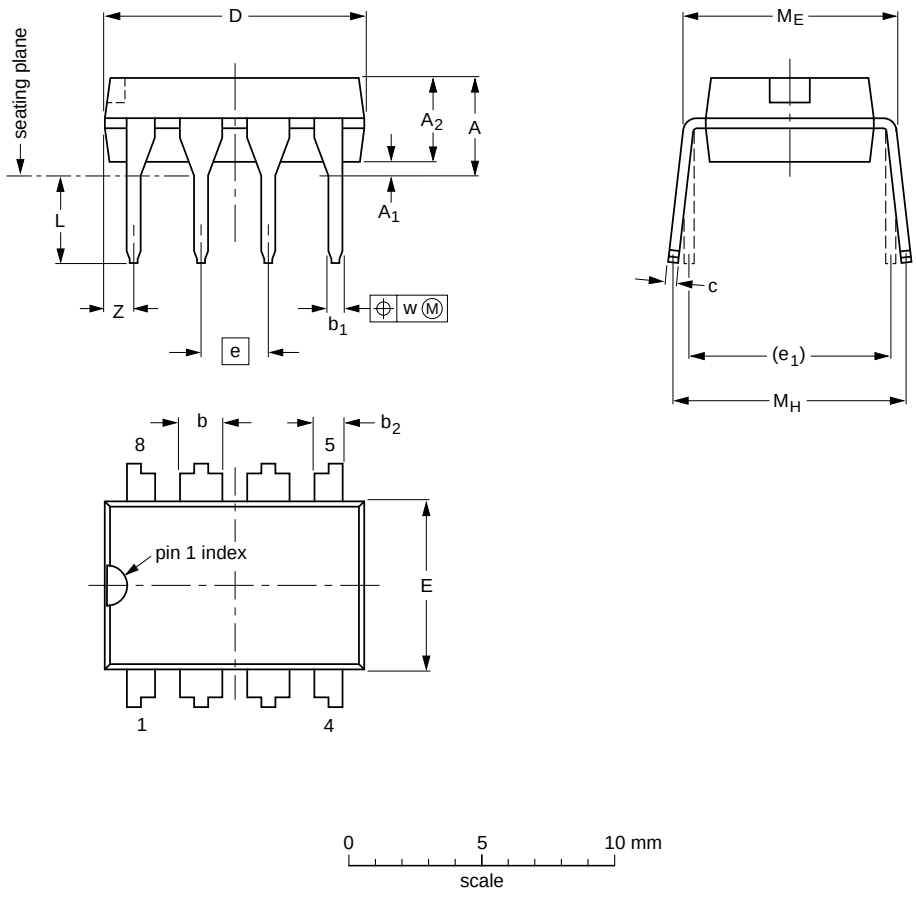


Fig.13 Application diagram.

PACKAGE OUTLINES

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

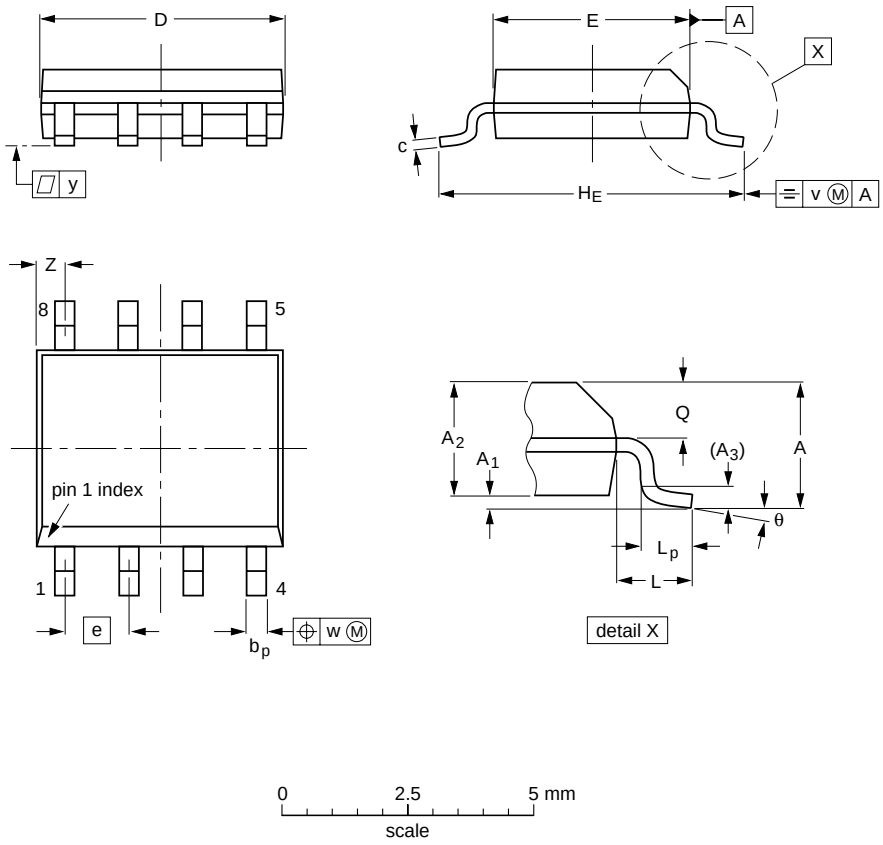
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001AN				~~92-11-17~~ 95-02-04

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~95-02-04~~ 97-05-22

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

DIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
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