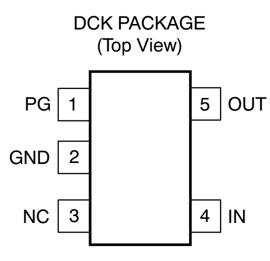
# Ultralow-Power SC70/SOT-323 Packaged 50mA LDO Linear Regulators with Power Good Output

## FEATURES

- **50mA Low-Dropout Regulator**
- **Ultralow 1.2μA Quiescent Current at 10mA**
- **5-Pin SC70/SOT-323 (DCK) Package**
- **Integrated Power Good Output**
- **Stable With Any Capacitor (> 0.47μF)**
- **Dropout Voltage Typically 105mV at 10mA (TPS79733)**
- **Over Current Limitation**
- **–40°C to +85°C Operating Junction Temperature Range**

## APPLICATIONS

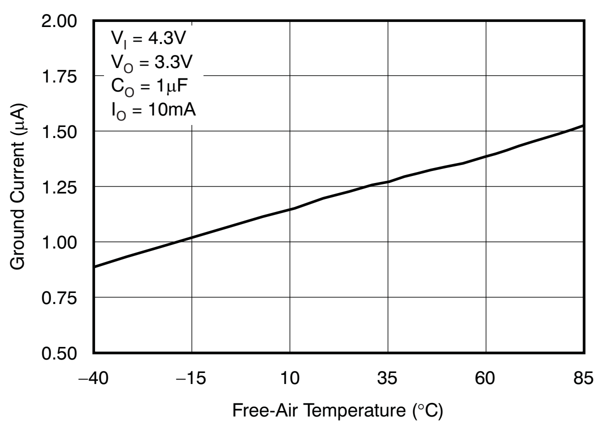
- **Battery-Powered Microcontrollers and Microprocessors**




## DESCRIPTION

The TPS797xx family of low-dropout (LDO) voltage regulators offers the benefits of low-dropout voltage and ultralow-power operation. The device is stable with any capacitor (> 0.47μF). Therefore, implementations of this device require very little board space due to the miniaturized packaging and potentially small output capacitor. In addition, the family includes an integrated open drain active-high power good (PG) output. Intended for use in microcontroller-based, battery-powered applications, the TPS797xx family's low dropout and ultralow-powered operation results in a significant increase in system battery operating life. The small packaging minimizes consumption of board space.

The device is enabled when the applied voltage exceeds the minimum input voltage. The usual PNP pass transistor has been replaced by a PMOS pass element. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage is very low, typically 105mV at 10mA of load current, and is directly proportional to the load current. The quiescent current is ultralow (1.2μA typically) and is stable over the entire range of output load current (0mA to 50mA). When properly configured with a pull-up resistor, the PG output can be used to implement a power-on reset or low battery indicator. The TPS797xx is offered in 1.8V, 3V, and 3.3V fixed options.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION[1]

| PRODUCT | $V_{OUT}$[2] |
|---|---|
| TPS797***xxyyyz*** | **XX** is nominal output voltage (for example, 25 = 2.5V, 01 = Adjustable[3]).<br>**YYY** is package designator.<br>**Z** is package quantity. |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Output voltages from 1.25V to 4.9V in 50mV increments are available through the use of probe level programming; minimum order quantities may apply. Contact factory for details and availability.
(3) For fixed 1.2V operation, tie FB to OUT.

## ABSOLUTE MAXIMUM RATINGS

Over operating junction temperature range, unless otherwise noted.[1]

| | |
|---|---|
| Input voltage range[2] | –0.3V to 6V |
| Maximum dc output voltage | 4.9V |
| Peak output current | Internally limited |
| ESD rating, HBM | 2kV |
| ESD rating, CDM | 500V |
| Continuous total power dissipation | See Dissipation Ratings Table |
| Operating virtual junction temperature range, $T_J$ | –40°C to +85°C |
| Storage temperature range, $T_{STG}$ | –65°C to +150°C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

## PACKAGE DISSIPATION RATINGS

| BOARD | PACKAGE | $R_{\theta JC}$ °C/W | $R_{\theta JA}$ °C/W | DERATING FACTOR ABOVE $T_A$ = +25°C | $T_A \leq$ +25°C POWER RATING | $T_A$ = +70°C POWER RATING | $T_A$ = +85°C POWER RATING |
|---|---|---|---|---|---|---|---|
| Low K[1] | DCK | 165.39 | 396.24 | 2.52mW/°C | 252mW | 139mW | 101mW |
| High K[2] | DCK | 165.39 | 314.74 | 3.18mW/°C | 318mW | 175mW | 127mW |

(1) The JEDEC low K (1s) board design used to derive this data was a 3-inch × 3-inch, two layer board with 2 ounce copper traces on top of the board.
(2) The JEDEC high K (2s2p) board design used to derive this data was a 3-inch × 3-inch, multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.

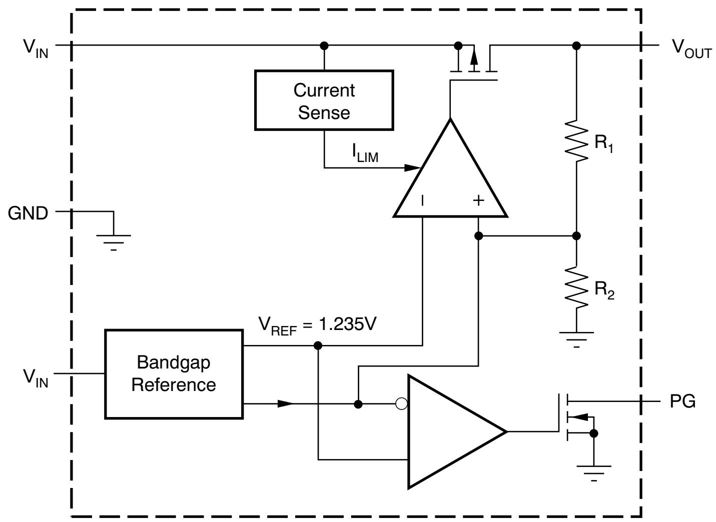
## ELECTRICAL CHARACTERISTICS

Over operating temperature range $T_J$ = –40°C to +125°C, $V_{IN}$ = $V_{OUT}$ (typ) +0.5V or 2.0V, whichever is greater; $I_{OUT}$ = 0.5mA, $V_{SET}$, $V_{EN}$ = $V_{IN}$, and $C_{OUT}$ = 1.0µF, unless otherwise noted. Typical values are at $T_A$ = +25°C.

| PARAMETER | | TEST CONDITIONS | TPS797xx MIN | TPS797xx TYP | TPS797xx MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage(1) | $I_{OUT}$ = 3mA | 1.8 | | 5.5 | V |
| | | $I_{OUT}$ = 10mA | 2 | | 5.5 | |
| $I_{OUT}$ | Continuous output current(2) | | 0 | | 50 | mA |
| $V_{OUT}$ | Output voltage accuracy(3) | $V_{OUT}$ + 1V ≤ $V_{IN}$ ≤ 5.5V<br>10µA < $I_{OUT}$ < 10mA | –4 | | 4 | % |
| $\Delta V_{OUT}\%$ / $\Delta V_{IN}$ | Line regulation(3) | $V_{OUT}$ + 1V ≤ $V_{IN}$ ≤ 5.5V | | 0.15 | 0.8 | %/V |
| $\Delta V_{OUT}\%$ / $\Delta I_{OUT}$ | Load regulation | 1µA < $I_{OUT}$ < 10mA | | 5 | | mV |
| $V_{DO}$ | Dropout voltage(4), $I_{OUT}$ = 10mA<br>$V_{IN}$ = $V_{OUT\ (NOM)}$ – 0.1V | TPS79730 | | 110 | 200 | mV |
| | | TPS79733 | | 105 | 200 | |
| $I_{SC}$ | Output current limit | $V_{OUT}$ = 0V | | 190 | 300 | mA |
| $I_{GND}$ | Ground pin current(3) | $I_{OUT}$ = 10mA | | 1.2 | 2 | µA |
| PSRR | Power-supply rejection ratio (ripple rejection) | f = 100Hz, $C_{OUT}$ = 10µF,<br>$I_{OUT}$ = 10mA | | 50 | | dB |
| $V_N$ | Output noise voltage (TPS79718) | BW = 200kHz to 100kHz,<br>$C_{OUT}$ = 10µF, $I_{OUT}$ = 10mA | | 600 | | $\mu V_{RMS}$ |
| $V_{PG(MIN)}$ | Minimum input voltage for valid PG | $V_{(PG)}$ ≥ 0.8V, $I_{PG}$ = 100µA | | 1.2 | | V |
| $V_{IT}$ | PG trip threshold voltage | $V_{OUT}$ decreasing | 82 | 90 | 96 | $\%/V_{OUT}$ |
| $V_{PG,LO}$ | PG output low voltage | $V_{IN}$ = 1.5V, $I_{PG}$ = 90µA | | 0.14 | 0.225 | V |
| $I_{PG,LKG}$ | PG leakage current | $V_{(PG)}$ = 5V, | 0.1 | | | nA |
| $T_J$ | Operating junction temperature, $T_J$ | | –40 | | +85 | °C |

(1) Minimum $V_{IN}$ = $V_{OUT}$ + $V_{DO}$ or the minimum value specified here, whichever is greater.
(2) Continuous output current is limited by internal protection circuitry, but it is not recommended that the device operate above this maximum for extended periods of time.
(3) Minimum $V_{IN}$ is specified in note (1).
(4) $V_{DO}$ is not measured for the TPS79718 because minimum $V_{IN}$ > 1.7V.

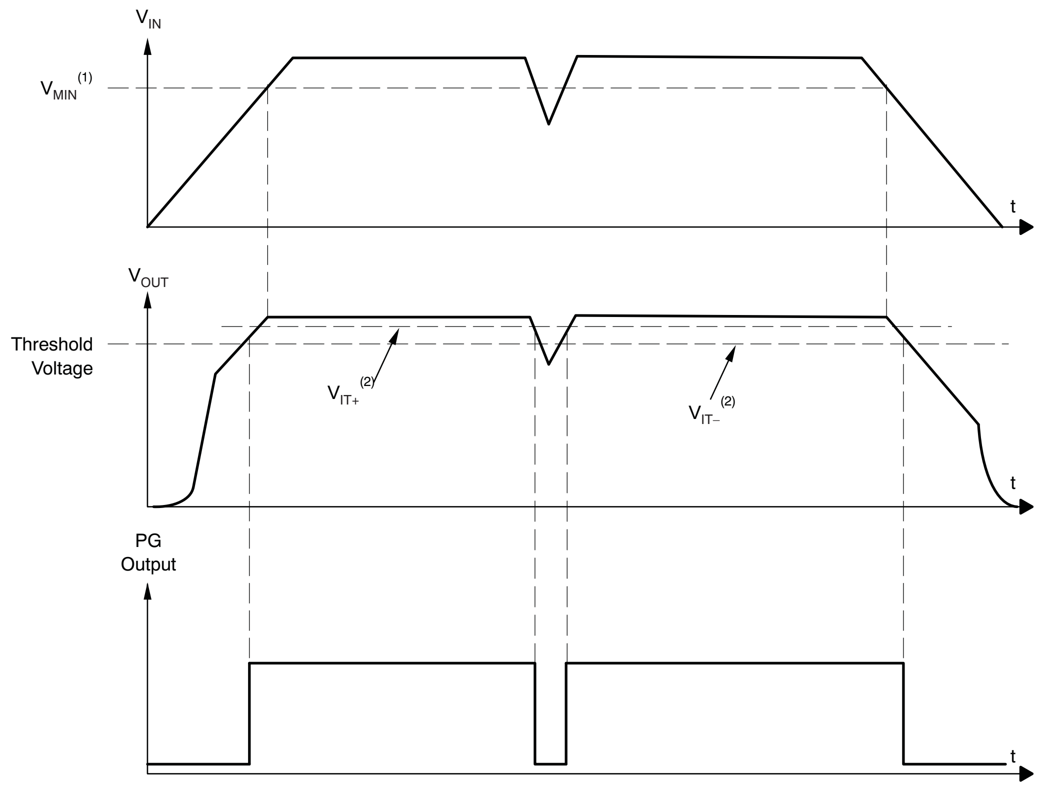
## FUNCTIONAL BLOCK DIAGRAM




### Table 1. TERMINAL FUNCTIONS

| TERMINAL | | DESCRIPTION |
|---|---|---|
| NAME | NO. | |
| GND | 2 | Ground |
| NC | 3 | No connection |
| OUT | 5 | The OUT terminal provides the regulated output voltage of the device. |
| PG | 1 | The PG terminal for the fixed voltage option devices is an open drain, active-high output that indicates the status of $V_O$ (output of the LDO). When $V_O$ exceeds approximately 90% of the regulated voltage, PG goes to a high-impedance state. It goes to a low-impedance state when $V_O$ falls below approximately 90% (that is, overload condition) of the regulated voltage. The open drain output of the PG terminal requires a pull-up resistor. |
| IN | 4 | The IN terminal is the power supply input to the device. |

## TPS797xx PG Timing Diagram




NOTES: (1) $V_{MIN} = V_{OUT} + V_{DO}$.

(2) The PG trip voltage is typically 10% lower than the output voltage (90% $V_O$). $V_{IT+}$ to $V_{IT-}$ is the hysteresis voltage.

## TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

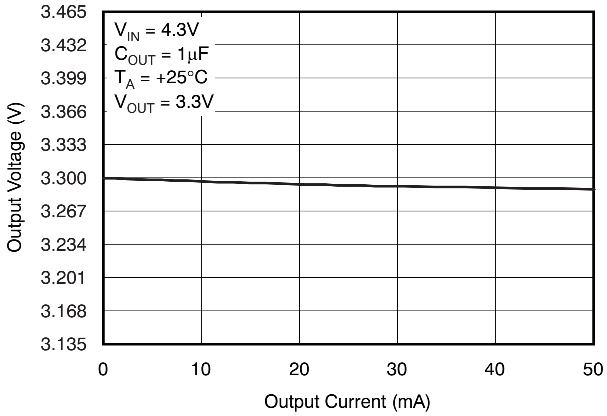



**Figure 1.**

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

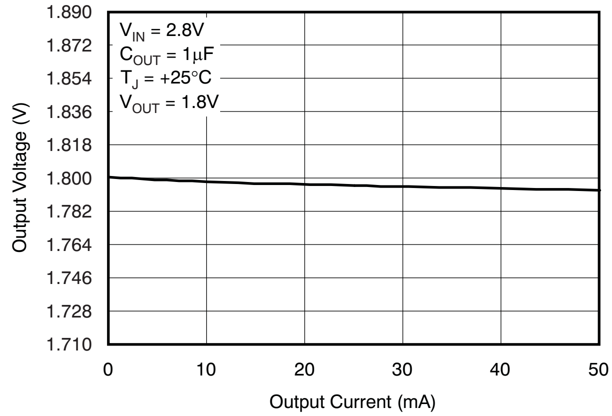



**Figure 2.**

OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

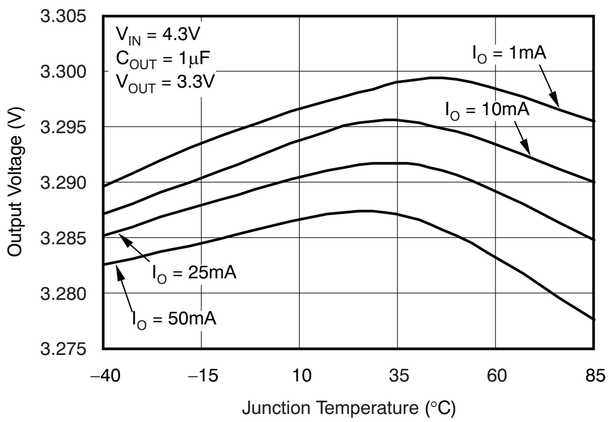



**Figure 3.**

OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

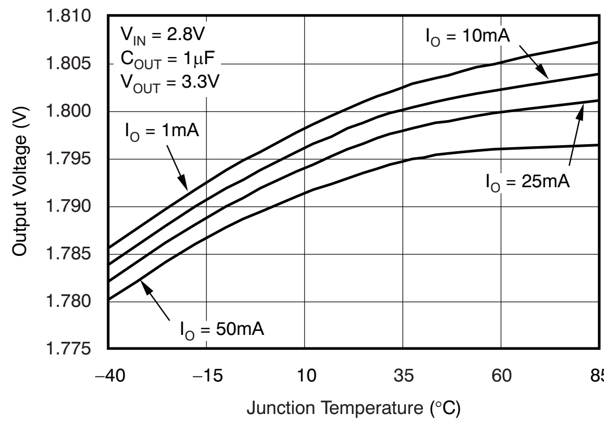



**Figure 4.**

GROUND CURRENT
vs
JUNCTION TEMPERATURE

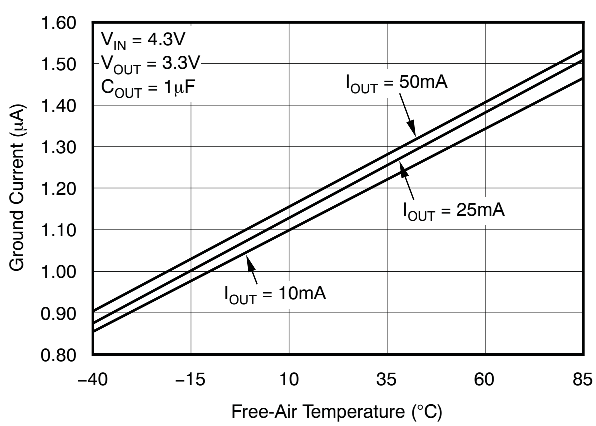



**Figure 5.**

OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

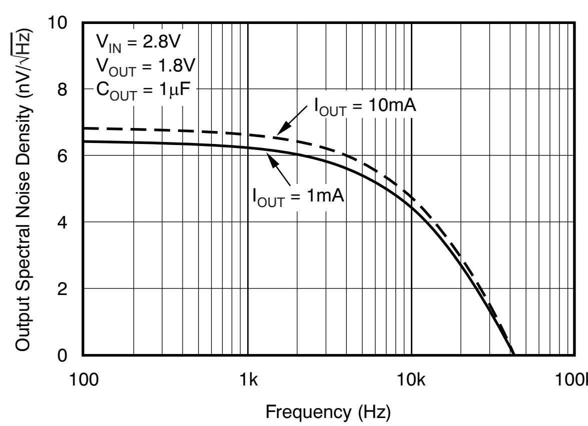



**Figure 6.**

## TYPICAL CHARACTERISTICS (continued)

**OUTPUT IMPEDANCE vs FREQUENCY**

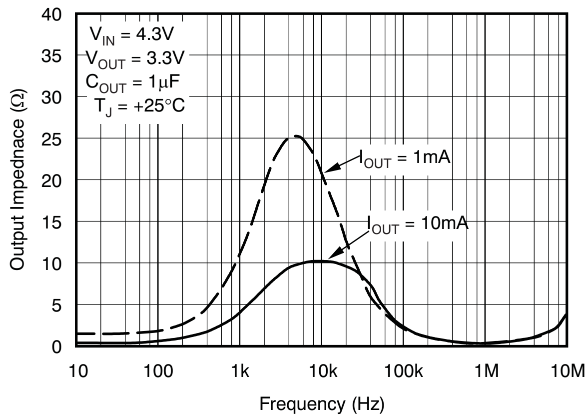



**Figure 7.**

**DROPOUT VOLTAGE vs JUNCTION TEMPERATURE**

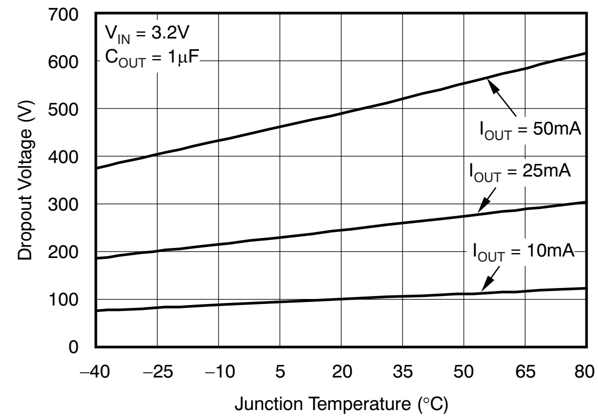



**Figure 8.**

**POWER-UP/POWER-DOWN**

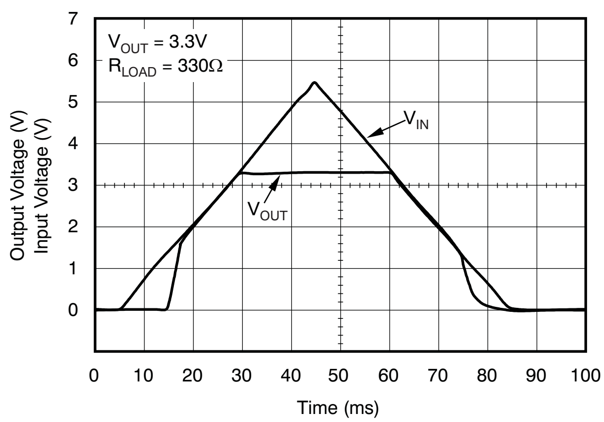



**Figure 9.**

**TPS79718 LINE TRANSIENT RESPONSE**

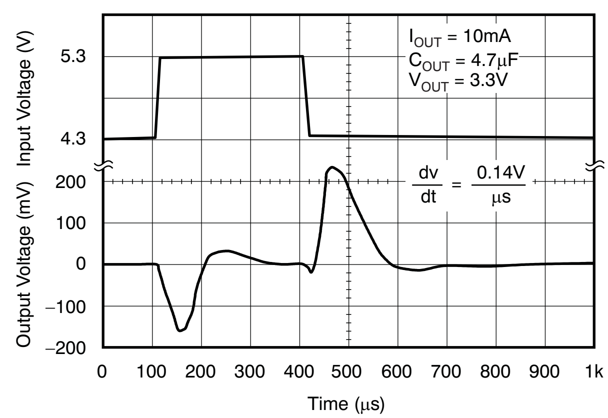



**Figure 10.**

**TPS79718 LOAD TRANSIENT RESPONSE**

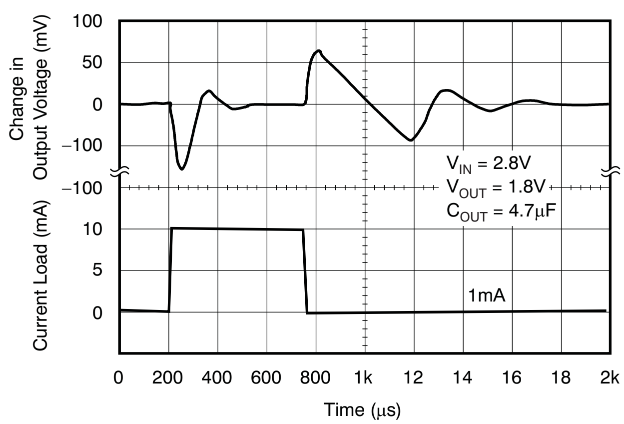



**Figure 11.**

**TPS79733 LINE TRANSIENT RESPONSE**

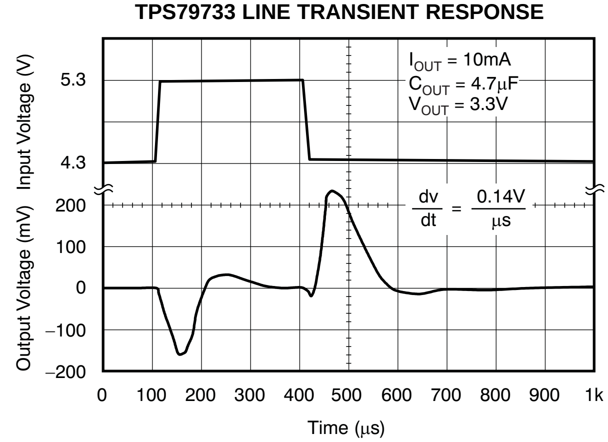



**Figure 12.**

## TYPICAL CHARACTERISTICS (continued)

**TPS79733 LOAD TRANSIENT RESPONSE**

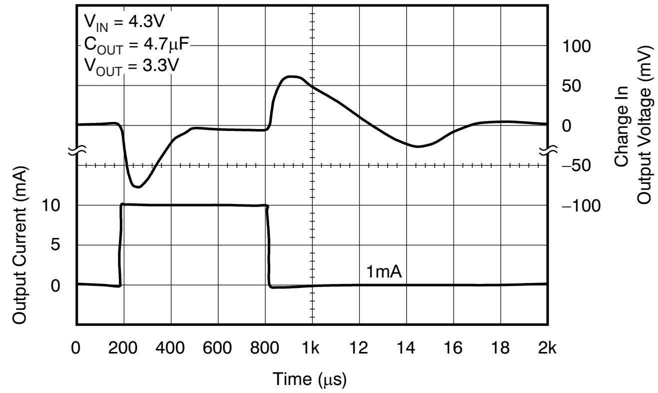



**Figure 13.**

## APPLICATION INFORMATION

The TPS797xx family of low-dropout (LDO) regulators have been optimized for use in micropower applications. They feature extremely low dropout voltages and ultralow quiescent current (1.2μA typically).

A typical application circuit is shown in Figure 14.

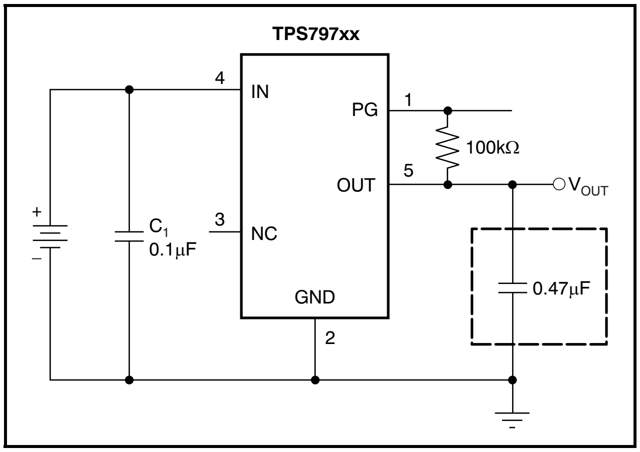



**Figure 14. Typical Application Circuit**

### External Capacitor Requirements

Although not required, a 0.1μF or larger input bypass capacitor, connected between IN and GND and located close to the TPS797xx, is recommended, especially when a highly resistive power supply is powering the LDO in addition to other devices. Like all low-dropout regulators, the TPS797xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 0.47μF. Any 0.47μF capacitor is suitable. Capacitor values larger than 0.47μF are acceptable.

### Power Dissipation and Junction Temperature

Specified regulator operation is assured to a junction temperature of +85°C; restrict the maximum junction temperature to +85°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(MAX)}$, and the actual dissipation, $P_D$, which must be less than or equal to $P_{D(MAX)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}} \quad (1)$$

Where:

$T_J$max is the maximum allowable junction temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package (see Package Dissipation Ratings).

$T_A$ is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \times I_O \quad (2)$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

### Regulator Protection

The TPS797xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS797xx features internal current limiting. During normal operation, the TPS797xx limits output current to approximately 190mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. Take care not to exceed the power dissipation ratings of the package.

### Microcontroller Application

One application for which this device is particularly suited is providing a regulated input voltage and power good (PG) supervisory signal to low-power devices such as mixed-signal microcontrollers. The quiescent or ground current of the TPS797xx family is typically 1.2μA even at full load; therefore, the reduction in battery life by including the TPS797xx in the system is negligible.

The primary benefits of using the TPS797xx to power low-power digital devices include:

- Regulated output voltage that protects the device from battery droop and noise on the line (for example, switch bounce)
- Smooth, monotonic power up
- PG signal for controlled device $\overline{\text{RESET}}$
- Potential to use an existing 5V power rail to power a 3.3V or lower device
- Potential to provide separate digital and analog power and ground supplies for a system with only one power source

Figure 15 shows an application in which the TPS79718 is used to power TI's MSP430 mixed signal microcontroller.

Minimal board space is needed to accommodate the DCK (SC70/SOT-323) packaged TPS79718, the 0.1μF output capacitor, the 0.47μF input capacitor, and the pull-up resistor on the PG pin.

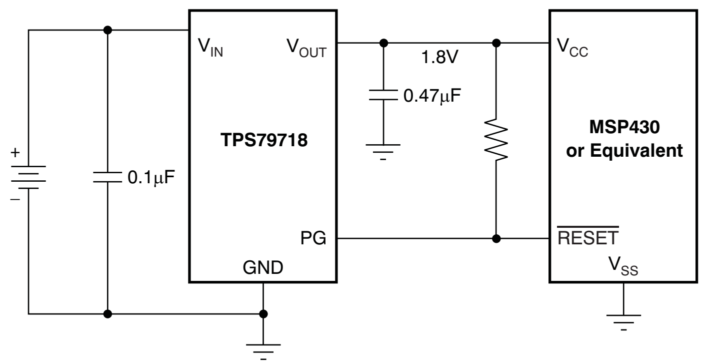



**Figure 15. MSP430 Microcontroller Powered by the TPS79718 Regulator**

## PACKAGING INFORMATION

| Orderable Device | Status [(1)] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [(2)] | Lead/Ball Finish | MSL Peak Temp [(3)] |
|---|---|---|---|---|---|---|---|---|
| TPS79718DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS79718DCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS79718DCKT | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS79718DCKTG4 | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS79730DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS79730DCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS79730DCKT | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS79730DCKTG4 | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS79733DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS79733DCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS79733DCKT | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS79733DCKTG4 | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

[(1)] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[(2)] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[(3)] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS79718, TPS79730, TPS79733 :**

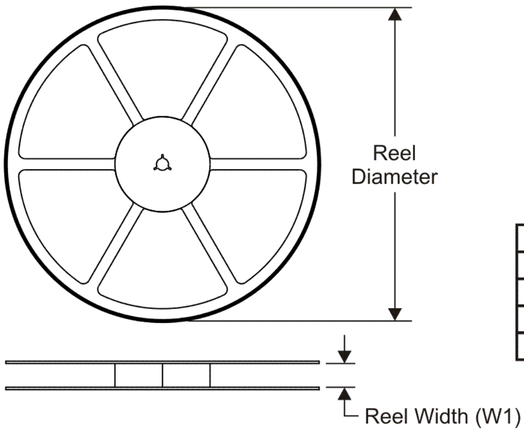
- Automotive: TPS79718-Q1, TPS79730-Q1, TPS79733-Q1
- Enhanced Product: TPS79718-EP, TPS79730-EP, TPS79733-EP

NOTE: Qualified Version Definitions:

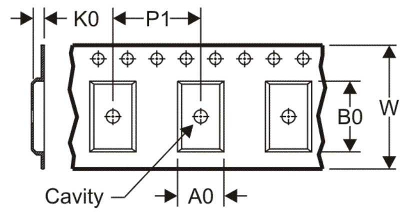
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

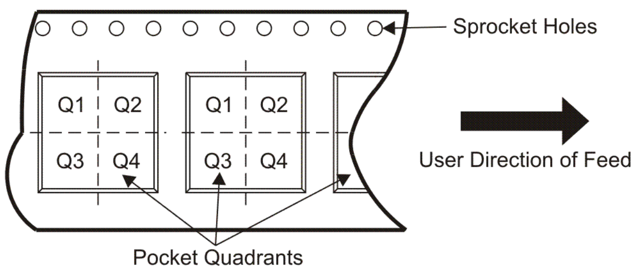



### TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

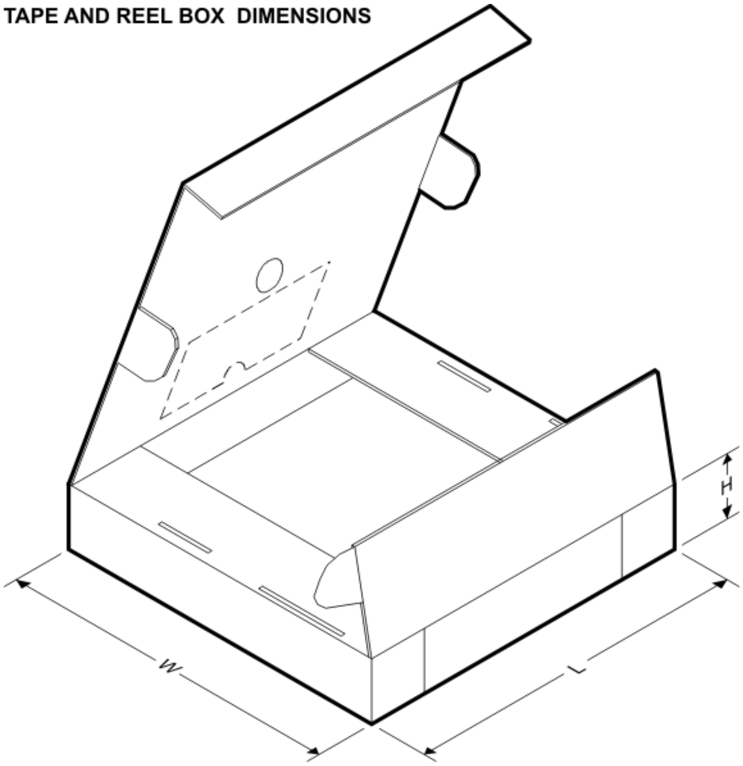
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS79718DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 9.2 | 2.24 | 1.22 | 2.34 | 4.0 | 8.0 | Q3 |
| TPS79718DCKT | SC70 | DCK | 5 | 250 | 180.0 | 9.2 | 2.24 | 1.22 | 2.34 | 4.0 | 8.0 | Q3 |
| TPS79730DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 9.2 | 2.24 | 1.22 | 2.34 | 4.0 | 8.0 | Q3 |
| TPS79730DCKT | SC70 | DCK | 5 | 250 | 180.0 | 9.2 | 2.24 | 1.22 | 2.34 | 4.0 | 8.0 | Q3 |
| TPS79733DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 9.2 | 2.24 | 1.22 | 2.34 | 4.0 | 8.0 | Q3 |
| TPS79733DCKT | SC70 | DCK | 5 | 250 | 180.0 | 9.2 | 2.24 | 1.22 | 2.34 | 4.0 | 8.0 | Q3 |

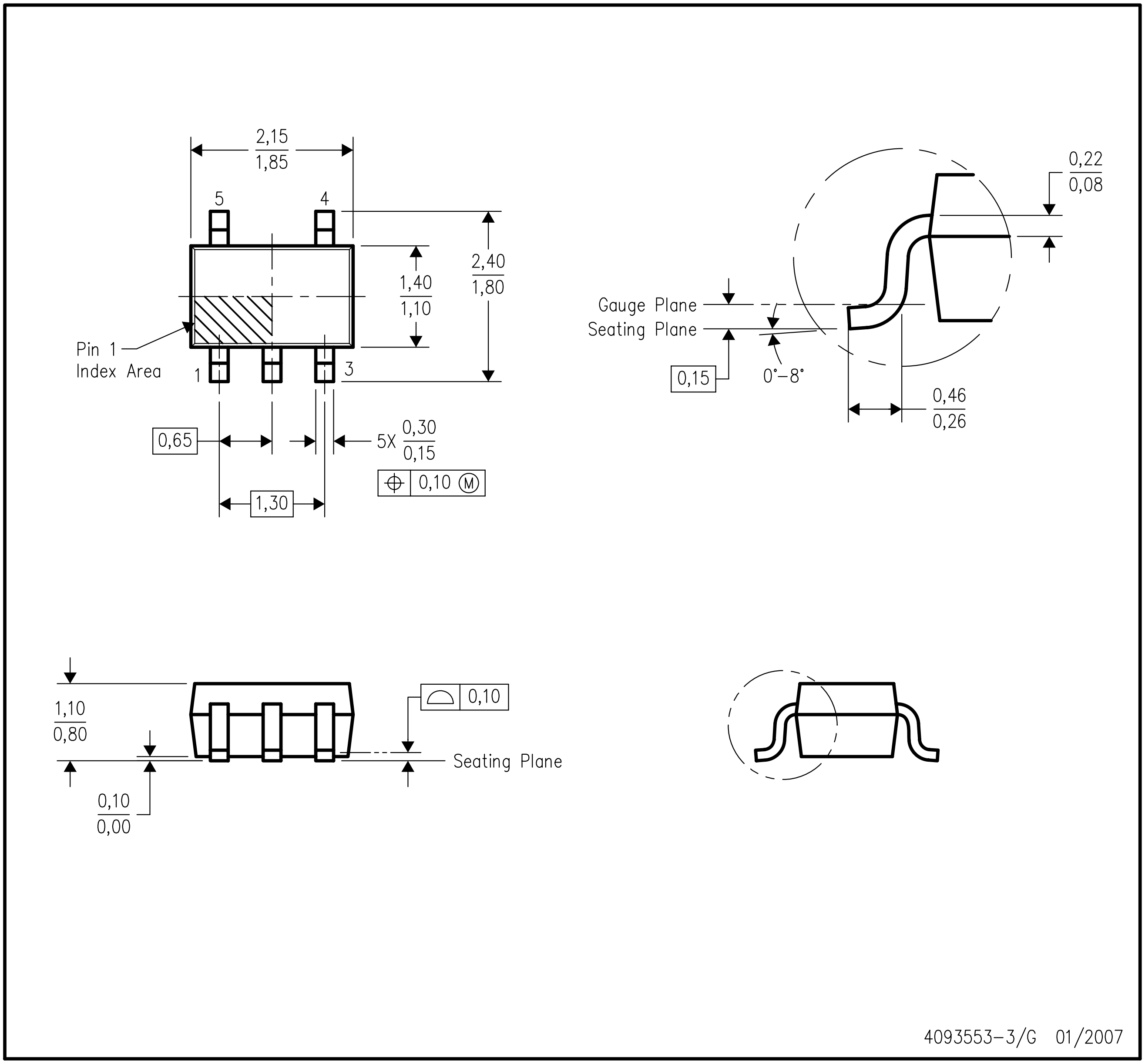
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS79718DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 85.0 |
| TPS79718DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 85.0 |
| TPS79730DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 85.0 |
| TPS79730DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 85.0 |
| TPS79733DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 85.0 |
| TPS79733DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 85.0 |

DCK (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AA.