PC910X

Ultra-high Speed Response OPIC Photocoupler

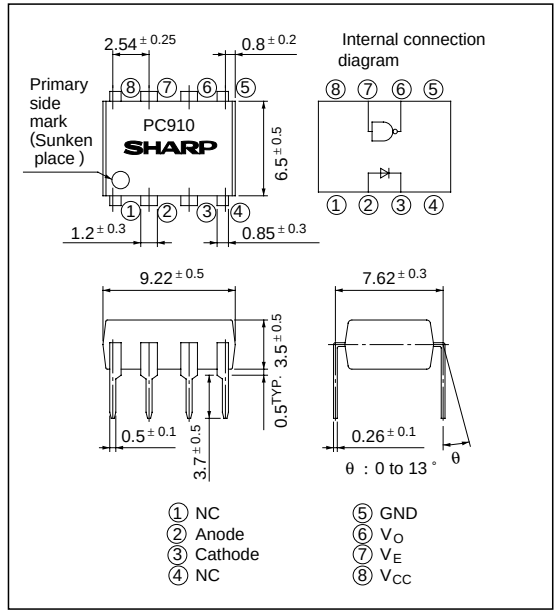
■ Features

1. Ultra-high speed response
   (t_{PHL}, t_{PLH} : TYP. 50ns at R_L = 350Ω)
2. Isolation voltage between input and output
   (Viso : 2 500 V_{rms})
3. Low input current drive(I_{FHL} : MAX. 5mA)
4. Instantaneous common mode rejection voltage(CM_H : TYP. 500V/μs)
5. TTL and LSTTL compatible output
6. Recognized by UL, file No. E64380

■ Applications

1. High speed interfaces for computer peripherals and microcomputer systems
2. High speed line receivers
3. Noise-cut
4. Interfaces with various data transmission equipment

■ Outline Dimensions (Unit : mm)



* "OPIC" (Optical IC) is a trademark of the SHARP Corporation. An OPIC consists of a light-detecting element and signal-processing circuit integrated onto a single chip.

■ Absolute Maximum Ratings (Ta= 25°C)

Parameter		Symbol	Rating	Unit
Input	*1 Forward current	I_F	20	mA
	Reverse voltage	V_R	5	V
	Power dissipation	P	40	mW
Output	*2 Supply voltage	V_{CC}	7	V
	*3 Enable voltage	V_E	5.5	V
	High level output voltage	V_{OH}	7	V
	Low level output current	I_{OL}	50	mA
	Collector power dissipation	P_C	85	mW
*4 Isolation voltage		V_{iso}	2 500	V_{rms}
Operating temperature		T_{opr}	0 to + 70	°C
Storage temperature		T_{stg}	- 55 to + 125	°C
*5 Soldering temperature		T_{sol}	260	°C

*1 Ta= 0 to 70°C
*2 For 1 minute max.
*3 Shall not exceed 500mV from supply voltage(V_{CC}).
*4 AC for 1minute, 40 to 60% RH. Apply the specified voltage between the whole of the electrode pins on the input side and the whole of the electrode pins on the output side.
*5 For 10 seconds at the position of 2mm or more from lead pins.

■ Electro-optical Characteristics

(Unless otherwise specified, Ta = 0 to 70˚C)

Parameter			Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input		Forward voltage	V_F	Ta = 25˚C, I_F = 10mA	-	1.6	1.9	V
		Reverse current	I_R	Ta = 25˚C, V_R = 5V	-	-	10	μA
		Terminal capacitance	C_t	Ta = 25˚C, V = 0, f = 1MHz	-	60	150	pF
Output		High level output current	I_{OH}	V_{CC} = V_O = 5.5V, V_E = 2.0V, I_F = 250μA	-	2	250	μA
		Low level output voltage	V_{OL}	V_{CC} = 5.5V, V_E = 2.0V, I_F = 5mA, I_{OL} = 13mA	-	0.4	0.6	V
		High level enable current	I_{EH}	V_{CC} = 5.5V, V_E = 2.0V	-	- 0.8	- 1.8	mA
		Low level enable current	I_{EL}	V_{CC} = 5.5V, V_E = 0.5V	-	- 1.2	- 2.0	mA
		High level supply current	I_{CCH}	V_{CC} = 5.5V, I_F = 0, V_E = 0.5V	-	7	15	mA
		Low level supply current	I_{CCL}	V_{CC} = 5.5V, I_F = 10mA, V_E = 0.5V	-	13	18	mA
Transfer characteristics		"High→Low" threshold input current	I_{FHL}	V_{CC} = 5V, V_E = 2.0V, V_O = 0.8V, R_L = 350Ω	-	2.5	5	mA
		Isolation resistance	R_{iso}	Ta = 25˚C, DC500V, 40 to 60% RH	5×10^{10}	10^{10}	-	Ω
		Floating capacitance	C_f	Ta = 25˚C, V = 0, f = 1MHz	-	0.6	5	pF
	Response time	"High→Low" propagation delay time	t_{PHL}	Fig. 1 Ta = 25˚C, V_{CC} = 5V, R_L = 350Ω, C_L = 15pF, I_F = 7.5mA	-	50	120	ns
		"Low→High" propagation delay time	t_{PLH}		-	50	120	ns
		Rise time, Fall time	t_r, t_f		-	30	60	ns
		"High→Low" enable propagation delay time	t_{EHL}	Fig. 2 Ta = 25˚C, V_{CC} = 5V, R_L = 350Ω, C_L = 15pF, I_F = 7.5mA, V_{EH} = 3V, V_{EL} = 0.5V	-	15	50	ns
		"Low→High" enable propagation delay time	t_{ELH}		-	65	100	ns
	CMR	Instantaneous common mode rejection voltage "Output: High level"	CM_H	Fig. 3 Ta = 25˚C, V_{CC} = 5V, V_{CM} = 10V(peak), R_L = 350Ω, I_F = 0, $V_{O(MIN)}$ = 2V	100	500	-	V/μs
		Instantaneous common mode rejection voltage "Output: Low level"	CM_L	Fig. 3 Ta = 25˚C, V_{CC} = 5V, V_{CM} = 10V(peak), R_L = 350Ω, I_F = 5mA $V_{O(MAX)}$ = 0.8V	- 100	- 500	-	V/μs

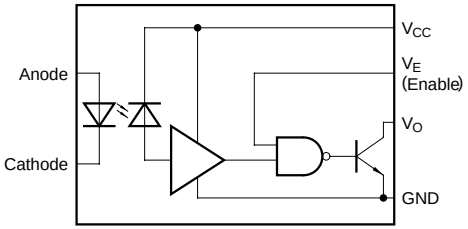
All typical values : at Ta = 25˚C, V_{CC} = 5V

■ Recommended Operating Conditions

Parameter	Symbol	MIN.	MAX.	Unit
Low level input current	I_{FL}	0	250	μA
High level input current	I_{FH}	7	15	mA
High level enable voltage	V_{EH}	2.0	V_{CC}	V
Low level enable voltage	V_{EL}	0	0.8	V
Supply voltage	V_{CC}	4.5	5.5	V
Fanout (TTL load)	N	-	8	-
Operating temperature	T_{opr}	0	70	˚C

1. When the enable input is in high level state, extemal pull-up resistor is unnecessary.
2. Connect a by-pass ceramic capacitor (0.01 to 0.1μF) between V_{CC} and GND at the position within 1cm from pin.

Circuit Block Diagram

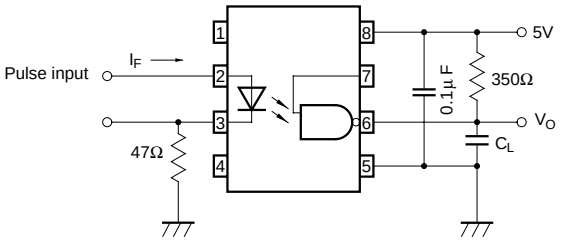


Truth Table

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H

L : Logic (0)
H : Logic (1)

Fig. 1 Test Circuit for t_{PHL}, t_{PLH}, t_r and t_f



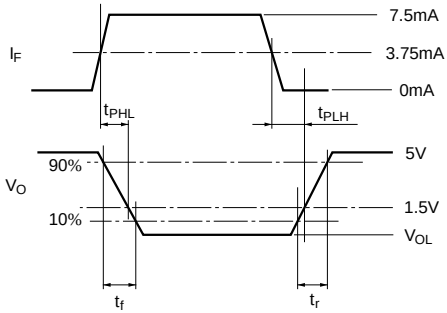
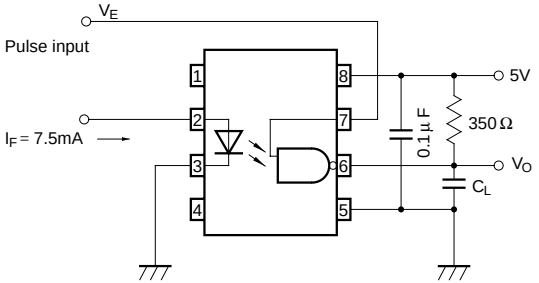


Fig. 2 Test Circuit for t_{EHL} and t_{ELH}



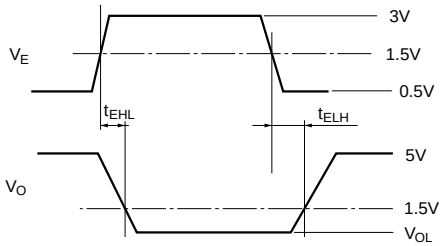
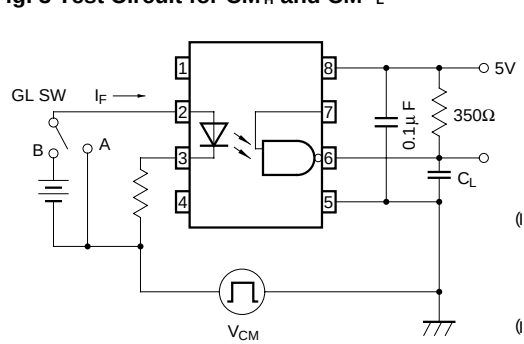


Fig. 3 Test Circuit for CM_H and CM_L



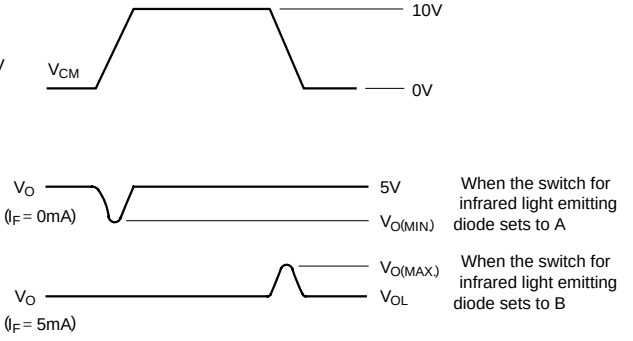


Fig. 4 Collector Power Dissipation vs. Ambient Temperature

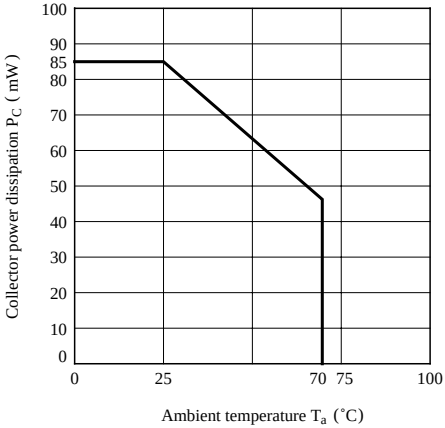


Fig. 5 Forward Current vs. Forward Voltage

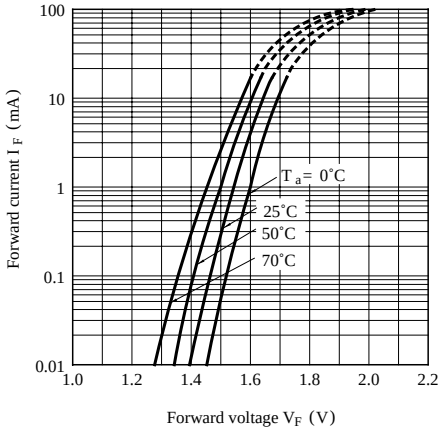


Fig. 6 High Level Output Current vs. Ambient Temperature

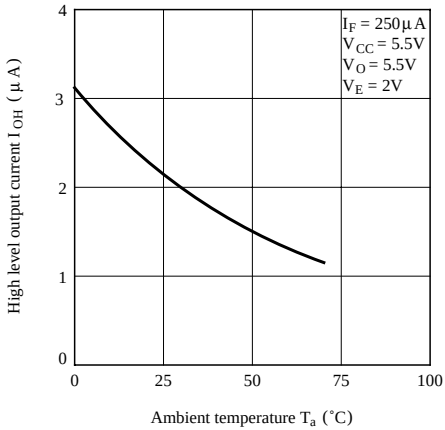


Fig. 7 Low Level Output Voltage vs. Ambient Temperature

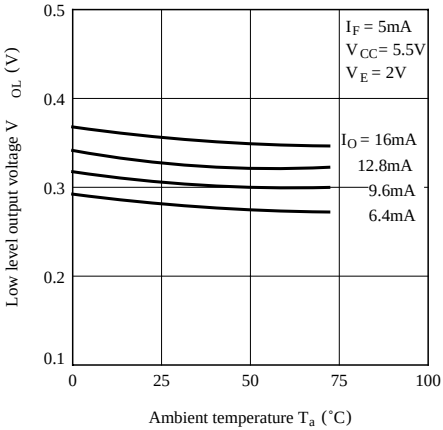


Fig. 8-a Output Voltage vs. Forward Current

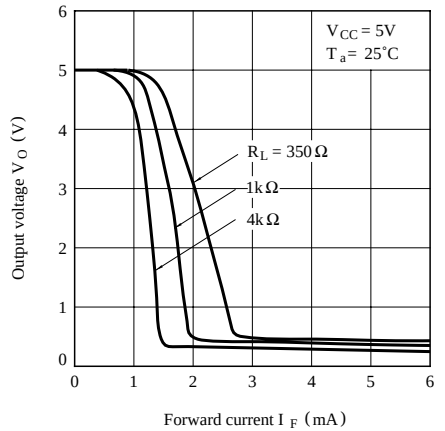


Fig. 8-b Output Voltage vs. Forward Current (Ambient Temp. Characteristics)

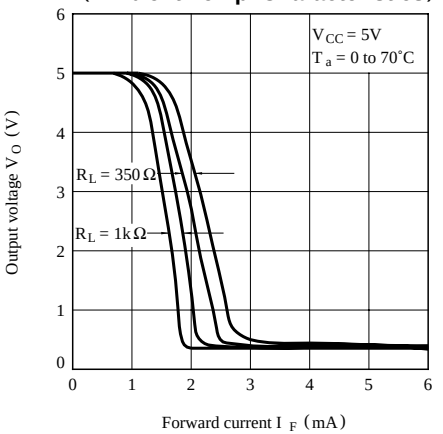


Fig. 9 Propagation Delay Time vs. Forward Current

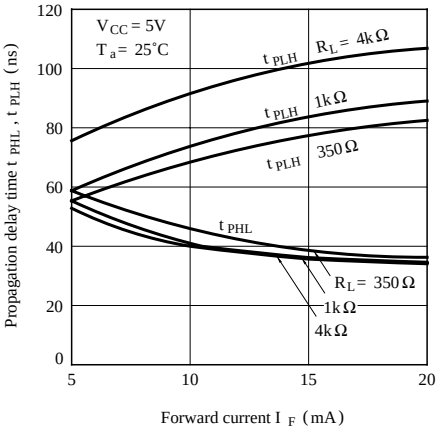


Fig.10 Propagation Delay Time vs. Ambient Temperature

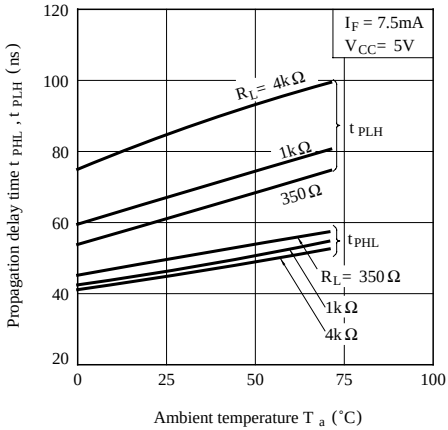


Fig.11 Rise Time, Fall Time vs. Ambient Temperature

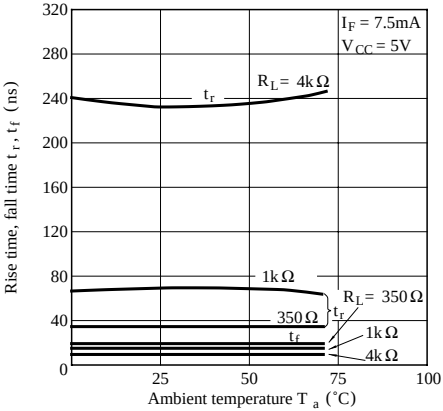
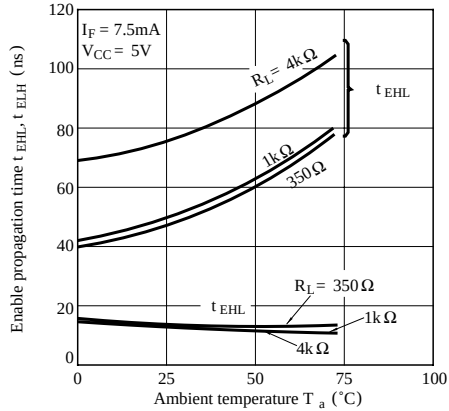


Fig.12 Enable Propagation Time vs. Ambient Temperature



■ Precautions for Use

(1) Handle this product the same as with other integrated circuits against static electricity.

(2) As for other general cautions, refer to the chapter "Precautions for Use"