DATA SHEET

BSS84
P-channel enhancement mode vertical D-MOS transistor

Product specification
Supersedes data of 1995 Apr 07
File under Discrete Semiconductors, SC13b

1997 Jun 18

Philips Semiconductors

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P-channel enhancement mode vertical D-MOS transistor

BSS84

FEATURES

- Low threshold voltage
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

APPLICATIONS

- Line current interrupter in telephone sets
- Relay, high speed and line transformer drivers.

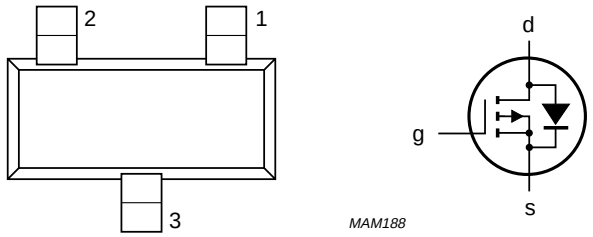
DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a SOT23 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain



Top view

Marking code: SP

Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–50	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = –1 mA; V_{DS} = V_{GS}	–0.8	–2	V
I_D	drain current (DC)		–	–130	mA
R_{DSon}	drain-source on-state resistance	I_D = –130 mA; V_{GS} = –10 V	–	10	Ω
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	250	mW

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–50	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	–130	mA
I_{DM}	peak drain current		–	–520	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	250	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	500	K/W

Note to the Limiting values and Thermal characteristics

1. Device mounted on a printed-circuit board.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = –10 μA	–50	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = V_{GS}$; I_D = –1 mA	–0.8	–	–2	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = –40 V	–	–	–100	nA
		V_{GS} = 0; V_{DS} = –50 V	–	–	–10	μA
		V_{GS} = 0; V_{DS} = –50 V; T_j = 125 °C	–	–	–60	μA
I_{GSS}	gate leakage current	V_{DS} = 0; V_{GS} = ±20 V	–	–	±10	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = –10 V; I_D = –130 mA	–	–	10	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = –25 V; I_D = –130 mA	50	–	–	mS
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = –25 V; f = 1 MHz	–	25	45	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = –25 V; f = 1 MHz	–	15	25	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = –25 V; f = 1 MHz	–	3.5	12	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	V_{GS} = 0 to –10 V; V_{DD} = –40 V; I_D = –200 mA	–	3	–	ns
t_{off}	turn-off time	V_{GS} = –10 to 0 V; V_{DD} = –40 V; I_D = –200 mA	–	7	–	ns

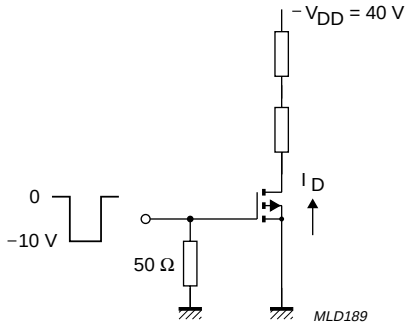


Fig.2 Switching time test circuit.

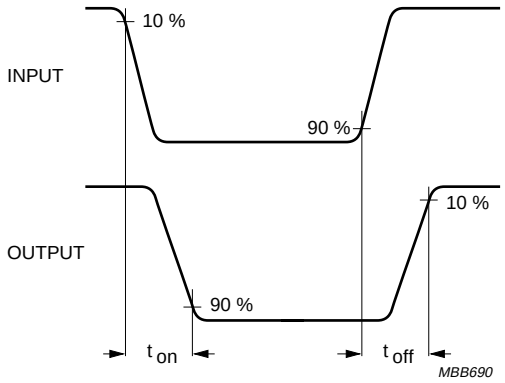


Fig.3 Input and output waveforms.

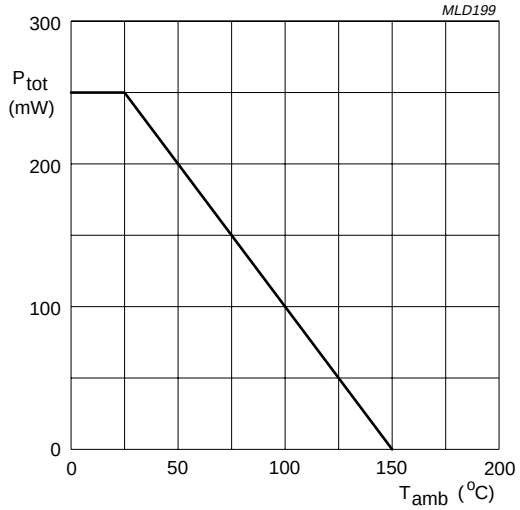
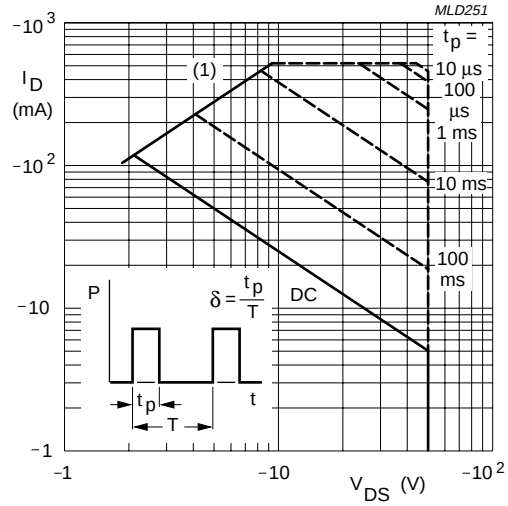
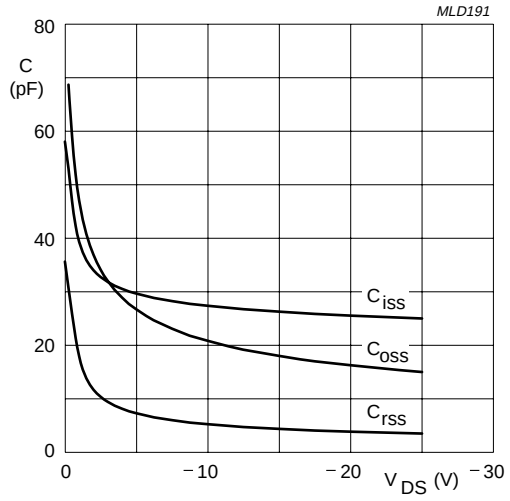


Fig.4 Power derating curve.



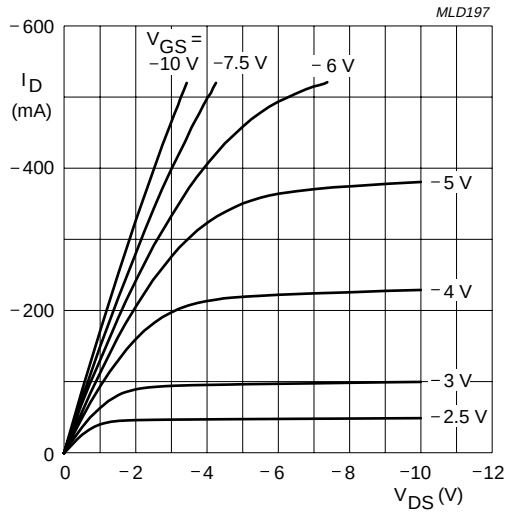
δ = 0.01.
T_{amb} = 25 °C.
(1) R_{DSon} limitation.

Fig.5 DC SOAR.



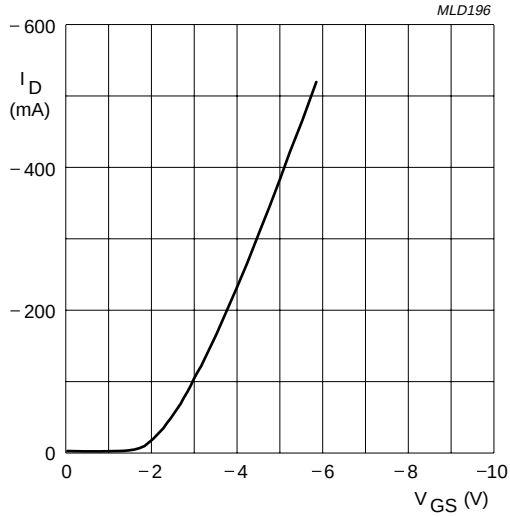
V_{GS} = 0; T_j = 25 °C; f = 1 MHz.

Fig.6 Capacitance as a function of drain source voltage; typical values.



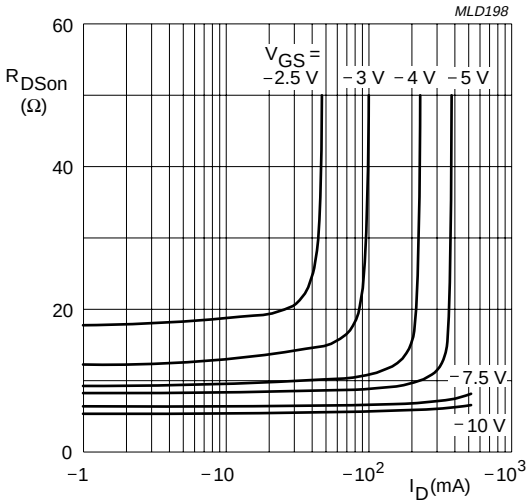
T_j = 25 °C.

Fig.7 Typical output characteristics.



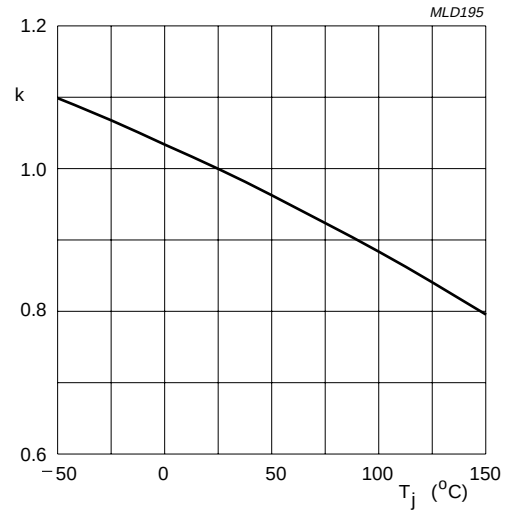
V_{DS} = –10 V; T_j = 25 °C.

Fig.8 Typical transfer characteristics.



T_j = 25 °C.

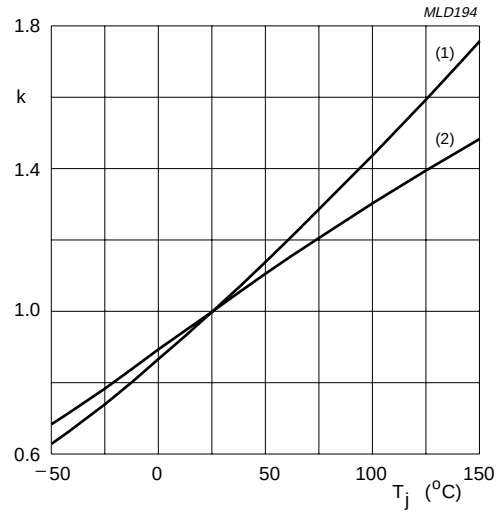
Fig.9 Drain-source on-state resistance as a function of drain current; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

$I_D = -1$ mA; $V_{DS} = V_{GS}$.

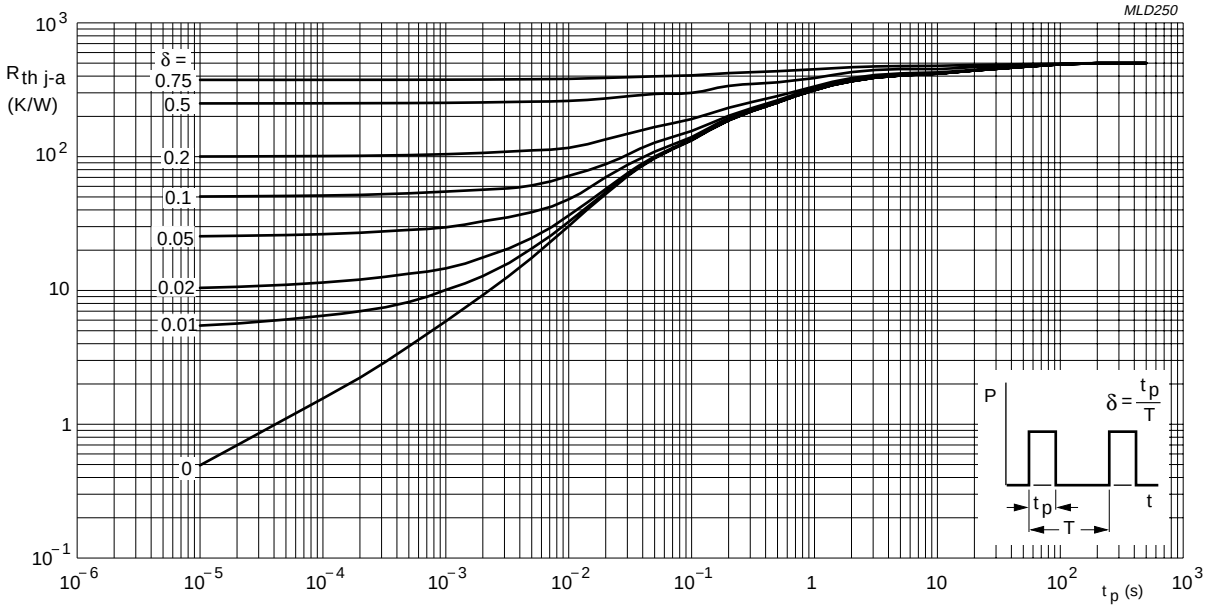
Fig.10 Temperature coefficient of gate-source threshold voltage.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

(1) $I_D = -130$ mA; $V_{GS} = -10$ V.
(2) $I_D = -20$ mA; $V_{GS} = -2.4$ V.

Fig.11 Temperature coefficient of drain-source on-state resistance.

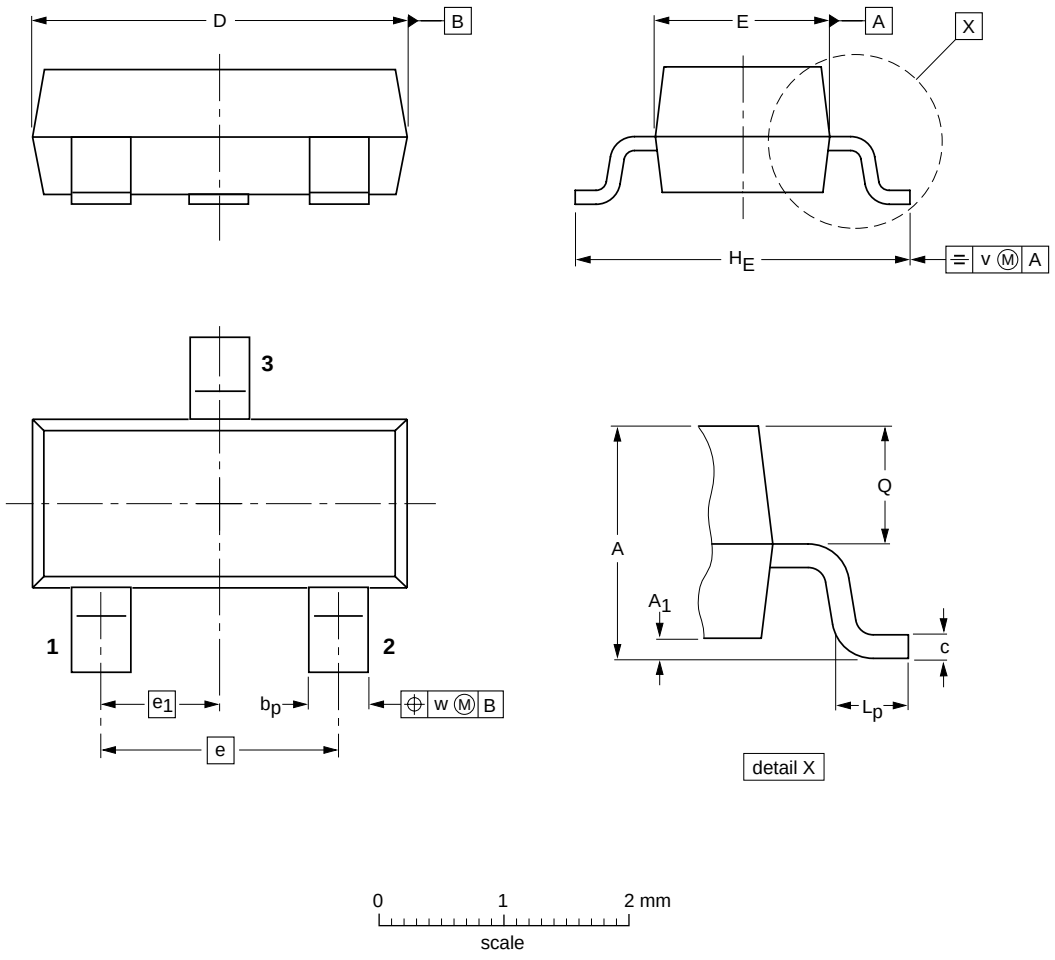


$T_{amb} = 25$ °C.

Fig.12 Thermal resistance from junction to ambient as a function of pulse time; typical values.

PACKAGE OUTLINE

Plastic surface mounted package; 3 leads **SOT23**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max.	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT23						97-02-28

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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