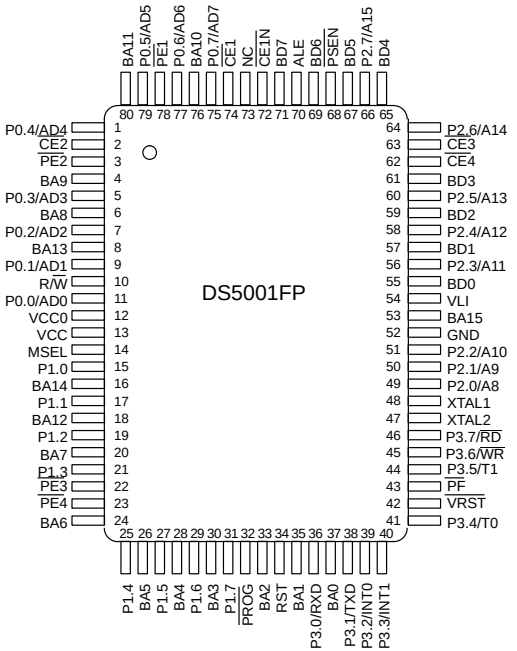
DALLAS SEMICONDUCTOR

DS5001FP
128K Soft Microprocessor Chip

FEATURES

- 8051 compatible microprocessor adapts to its task
  - Accesses up to 128K bytes of nonvolatile SRAM
  - In–system programming via on–chip serial port
  - Can modify its own program or data memory
  - Accesses memory on a separate Byte–wide bus
  - Performs CRC–16 check of NV RAM memory
  - Decodes memory and peripheral chip enables
- Crashproof Operation
  - Maintains all nonvolatile resources for over 10 years
  - Power–fail Reset
  - Early Warning Power–fail Interrupt
  - Watchdog Timer
  - Lithium backs user SRAM for program/data storage
  - Precision band–gap reference for power monitor
- Fully 8051 Compatible
  - 128K bytes scratchpad RAM
  - Two timer/counters
  - On–chip serial port
  - 32 parallel I/O port pins
- Software Security Available with DS5002FP Secure Microprocessor

PIN ASSIGNMENT



DESCRIPTION

The DS5001FP is an 8051 compatible microprocessor based on nonvolatile RAM technology. It is designed for systems that need large quantities of nonvolatile memory. Like its predecessor the DS5000(T), the DS5001FP is substantially more flexible than a standard 8051. It provides full compatibility with the 8051 instruction set, timers, serial port, and parallel I/O ports. By using NV RAM instead of ROM, the user can program, then reprogram the microprocessor while in–system. The application software can even change its own operation. This allows frequent software upgrades, adaptive programs, customized systems, etc. In addition, by using NV SRAM, the DS5001FP is ideal for data logging applications. It also connects easily to a Dallas Real Time Clock for time stamp and date.

The DS5001FP provides the benefits of NV RAM without using I/O resources. It uses a non–multiplexed Byte–wide address and data bus for memory access. This bus can perform all memory access and provides decoded chip enables for SRAM. This leaves the 32 I/O port pins free for application use. The DS5001FP uses ordinary SRAM and battery backs the memory contents with an external lithium cell. Data is maintained for over 10 years at room temperature with a very small lithium cell. A DS5001FP also provides crashproof operation in portable systems or systems with unreliable power. These features include the ability to save the operating state, Power–fail Reset, Power–fail Interrupt, and Watchdog Timer.

A user loads programs into the DS5001FP via its on–chip Serial Bootstrap Loader. This function supervises the loading of software into NV RAM, validates it, then becomes transparent to the user. Software can be stored in multiple 32K or one 128K byte CMOS SRAM(s). Using its internal Partitioning, the DS5001FP can divide a common RAM into user selectable program and data segments. This Partition can be selected at program loading time, but can be modified anytime later. The microprocessor will decode memory access to the SRAM, access memory via its Byte–wide bus and write–protect the memory portion designated as ROM. Combining program and data storage in one device saves board space and cost.

The DS5001FP offers several bank switches for access to even more memory. In addition to the primary data area of 64K bytes, a peripheral selector creates a second 64K byte data space with four accompanying chip enables. This area can be used for memory mapped peripherals or more data storage. The DS5001FP can also use its Expanded bus on Ports 0 and 2 (like an 8051) to access an additional 64K bytes of data space. Lastly, the DS5001FP provides one additional bank switch that changes up to 60K bytes of the NV RAM program space into data memory. Thus with a small amount of logic, the DS5001 accesses up to 252K bytes of data memory.

For a user that wants a pre–constructed module using the DS5001FP, RAM, lithium cell, and a real time clock; the DS2251T is available and described in separate data sheet. More details are also contained in the User's Guide section of the Secure Microcontroller Data Book. For users that desire software security, the DS5002FP is functionally identical to the DS5001FP but provides the best firmware security available.

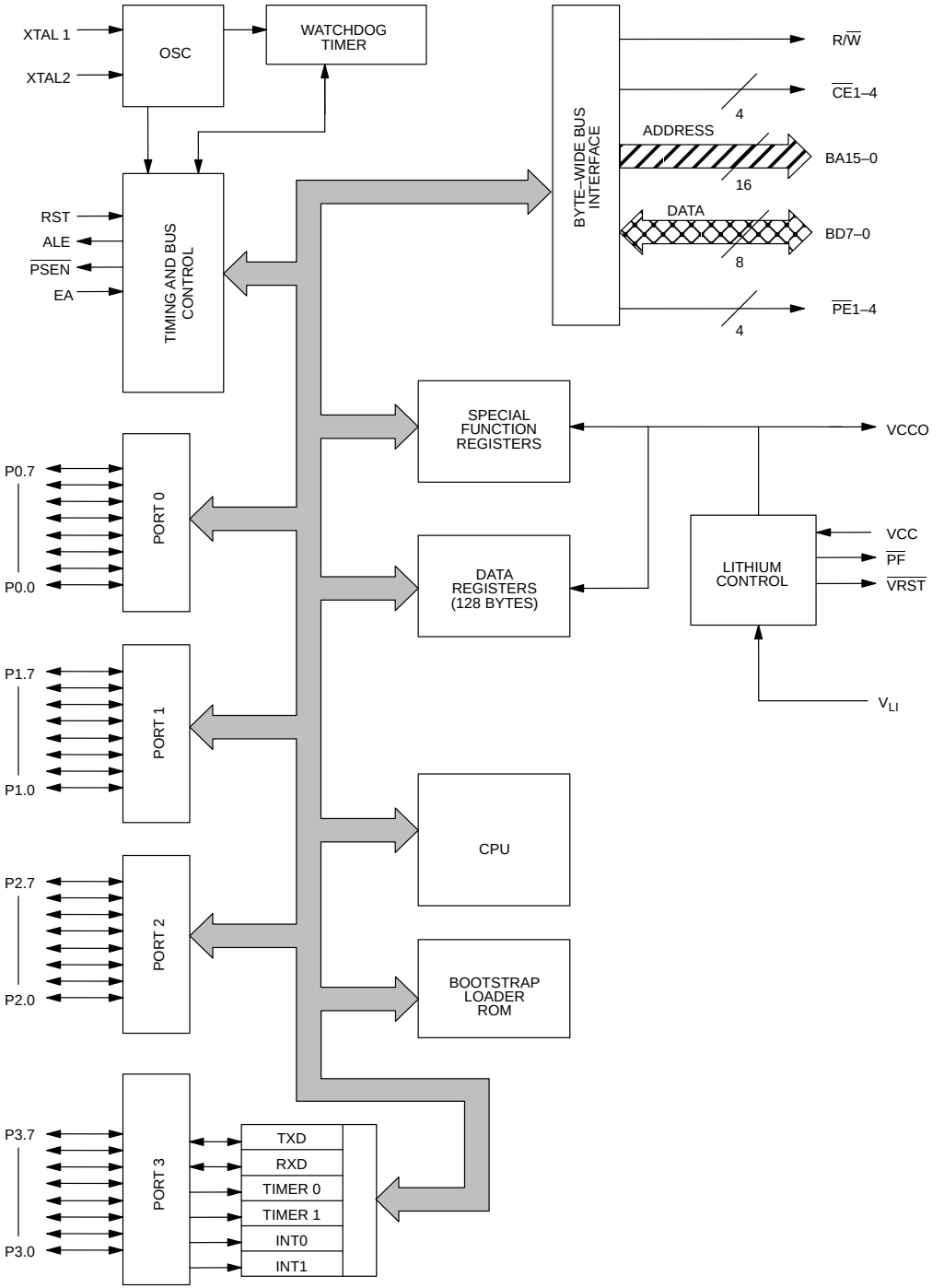
ORDERING INFORMATION

The following devices are available as standard products from Dallas Semiconductor:

PART #	DESCRIPTION
DS5001FP–16	80–pin QFP Max. clock speed 16 MHz, 0°C to +75°C operation

Operating information is contained in the User's Guide section of the Secure Microcontroller Data Book. This data sheet provides ordering information, pinout, and electrical specifications.

DS5001FP BLOCK DIAGRAM Figure 1



PIN DESCRIPTION

PIN	DESCRIPTION
11, 9, 7, 5, 1, 79, 77, 75	**P0.0 – P0.7.** General purpose I/O Port 0. This port is open–drain and can not drive a logic 1. It requires external pull–ups. Port 0 is also the multiplexed Expanded Address/Data bus. When used in this mode, it does not require pull–ups.
15, 17, 19, 21, 25, 27, 29, 31	**P1.0 – P1.7.** General purpose I/O Port 1.
49, 50, 51, 56, 58, 60, 64, 66	**P2.0 – P2.7.** General purpose I/O Port 2. Also serves as the MSB of the address in expanded memory accesses, and as pins of the RPC mode when used.
36	**P3.0 RXD.** General purpose I/O port pin 3.0. Also serves as the receive signal for the on board UART. This pin should NOT be connected directly to a PC COM port.
38	**P3.1 TXD.** General purpose I/O port pin 3.1. Also serves as the transmit signal for the on board UART. This pin should NOT be connected directly to a PC COM port.
39	**P3.2 $\overline{\text{INT0}}$.** General purpose I/O port pin 3.2. Also serves as the active low External Interrupt 0.
40	**P3.3 $\overline{\text{INT1}}$.** General purpose I/O port pin 3.3. Also serves as the active low External Interrupt 1.
41	**P3.4 T0.** General purpose I/O port pin 3.4. Also serves as the Timer 0 input.
44	**P3.5 T1.** General purpose I/O port pin 3.5. Also serves as the Timer 1 input.
45	**P3.6 $\overline{\text{WR}}$.** General purpose I/O port pin. Also serves as the write strobe for Expanded bus operation.
46	**P3.7 $\overline{\text{RD}}$.** General purpose I/O port pin. Also serves as the read strobe for Expanded bus operation.
34	**RST** – Active high reset input. A logic 1 applied to this pin will activate a reset state. This pin is pulled down internally so this pin can be left unconnected if not used. An RC power–on reset circuit is not needed and is NOT recommended.
68	**$\overline{\text{PSEN}}$** – Program Store Enable. This active low signal is used to enable an external program memory when using the Expanded bus. It is normally an output and should be unconnected if not used. $\overline{\text{PSEN}}$ also is used to invoke the Bootstrap Loader. At this time, $\overline{\text{PSEN}}$ will be pulled down externally. This should only be done once the DS5001FP is already in a reset state. The device that pulls down should be open drain since it must not interfere with $\overline{\text{PSEN}}$ under normal operation.
70	**ALE** – Address Latch Enable. Used to de–multiplex the multiplexed Expanded Address/Data bus on Port 0. This pin is normally connected to the clock input on a '373 type transparent latch.
47, 48	**XTAL2, XTAL1.** Used to connect an external crystal to the internal oscillator. XTAL1 is the input to an inverting amplifier and XTAL2 is the output.
52	**GND** – Logic ground.
13	**V_{CC} – +5V.**
12	**V_{CCO}** – V_{CC} Output. This is switched between V_{CC} and V_{LI} by internal circuits based on the level of V_{CC}. When power is above the lithium input, power will be drawn from V_{CC}. The lithium cell remains isolated from a load. When V_{CC} is below V_{LI}, the V_{CCO} switches to the V_{LI} source. V_{CCO} should be connected to the V_{CC} pin of an SRAM.
54	**V_{LI}** – Lithium Voltage Input. Connect to a lithium cell greater than V_{LImin} and no greater than V_{LImax} as shown in the electrical specifications. Nominal value is +3V.

PIN	DESCRIPTION
53, 16, 8, 18, 80, 76, 4, 6, 20, 24, 26, 28, 30, 33, 35, 37	**BA15 – 0.** Byte–wide Address bus bits 15–0. This bus is combined with the non–multiplexed data bus (BD7–0) to access NV SRAM. Decoding is performed using $\overline{CE1}$ through $\overline{CE4}$. Therefore, BA15 is not actually needed except for monitoring and debugging. Read/write access is controlled by R/$\overline{W}$. BA14–0 connect directly to an 8K, 32K, or 128K SRAM. If an 8K RAM is used, BA13 and BA14 will be unconnected. If a 128K SRAM is used, the micro converts $\overline{CE2}$ and $\overline{CE3}$ to serve as A16 and A15 respectively.
71, 69, 67, 65, 61, 59, 57, 55	**BD7 – 0.** Byte–wide Data bus bits 7–0. This 8 bit bi–directional bus is combined with the non–multiplexed address bus (BA14–0) to access NV SRAM. BD7–0 connect directly to an SRAM, and optionally to a Real Time Clock or other peripheral.
10	**R/$\overline{W}$** – Read/Write. This signal provides the write enable to the SRAMs on the Byte–wide bus. It is controlled by the memory map and Partition. The blocks selected as Program (ROM) will be write protected.
74	**$\overline{CE1}$** – Chip Enable 1. This is the primary decoded chip enable for memory access on the Byte–wide bus. It connects to the chip enable input of one SRAM. $\overline{CE1}$ is lithium backed. It will remain in a logic high inactive state when V_{CC} falls below V_{LI}.
72	**$\overline{CE1N}$** – Non battery backed version of chip enable 1. This can be used with a 32K byte EPROM. It should not be used with a battery backed chip.
2	**$\overline{CE2}$** – Chip Enable 2. This chip enable is provided to access a second 32K block of memory. It connects to the chip enable input of one SRAM. When MSEL=0, the micro converts $\overline{CE2}$ into A16 for a 128K x 8 SRAM. $\overline{CE2}$ is lithium backed and will remain at a logic high when V_{CC} falls below V_{LI}.
63	**$\overline{CE3}$** – Chip Enable 3. This chip enable is provided to access a third 32K block of memory. It connects to the chip enable input of one SRAM. When MSEL=0, the micro converts $\overline{CE3}$ into A15 for a 128K x 8 SRAM. $\overline{CE3}$ is lithium backed and will remain at a logic high when V_{CC} falls below V_{LI}.
62	**$\overline{CE4}$** – Chip Enable 4. This chip enable is provided to access a fourth 32K block of memory. It connects to the chip enable input of one SRAM. When MSEL=0, this signal is unused. $\overline{CE4}$ is lithium backed and will remain at a logic high when V_{CC} falls below V_{LI}.
78	**$\overline{PE1}$** – Peripheral Enable 1. Accesses data memory between addresses 0000h and 3FFFh when the PES bit is set to a logic 1. Commonly used to chip enable a Byte–wide Real Time Clock such as the DS1283. $\overline{PE1}$ is lithium backed and will remain at a logic high when V_{CC} falls below V_{LI}. Connect $\overline{PE1}$ to battery backed functions only.
3	**$\overline{PE2}$** – Peripheral Enable 2. Accesses data memory between addresses 4000h and 7FFFh when the PES bit is set to a logic 1. $\overline{PE2}$ is lithium backed and will remain at a logic high when V_{CC} falls below V_{LI}. Connect $\overline{PE2}$ to battery backed functions only.
22	**$\overline{PE3}$** – Peripheral Enable 3. Accesses data memory between addresses 8000h and BFFFh when the PES bit is set to a logic 1. $\overline{PE3}$ is not lithium backed and can be connected to any type of peripheral function. If connected to a battery backed chip, it will need additional circuitry to maintain the chip enable in an inactive state when $V_{CC} < V_{LI}$.
23	**$\overline{PE4}$** – Peripheral Enable 4. Accesses data memory between addresses C000h and FFFFh when the PES bit is set to a logic 1. $\overline{PE4}$ is not lithium backed and can be connected to any type of peripheral function. If connected to a battery backed chip, it will need additional circuitry to maintain the chip enable in an inactive state when $V_{CC} < V_{LI}$.
32	**$\overline{PROG}$** – Invokes the Bootstrap Loader on a falling edge. This signal should be debounced so that only one edge is detected. If connected to ground, the micro will enter Bootstrap loading on power up. This signal is pulled up internally.
42	**$\overline{VRST}$** – This I/O pin (open drain with internal pull–up) indicates that the power supply (V_{CC}) has fallen below the V_{CCmin} level and the micro is in a reset state. When this occurs, the DS5001FP will drive this pin to a logic 0. Because the micro is lithium backed, this signal is guaranteed even when V_{CC}=0V. Because it is an I/O pin, it will also force a reset if pulled low externally. This allows multiple parts to synchronize their power–down resets.

PIN	DESCRIPTION
43	**$\overline{\text{PF}}$** – This output goes to a logic 0 to indicate that the micro has switched to lithium backup. This corresponds to $V_{CC} < V_{LI}$. Because the micro is lithium backed, this signal is guaranteed even when V_{CC}=0V. The normal application of this signal is to control lithium powered current to isolate battery backed functions from non–battery backed functions.
14	**MSEL** – Memory select. This signal controls the memory size selection. When MSEL= +5V, the DS5001FP expects to use 32K x 8 SRAMs. When MSEL = 0V, the DS5001FP expects to use a 128K x 8 SRAM. MSEL must be connected regardless of Partition, Mode, etc.
73	**NC** – Do not connect.

INSTRUCTION SET

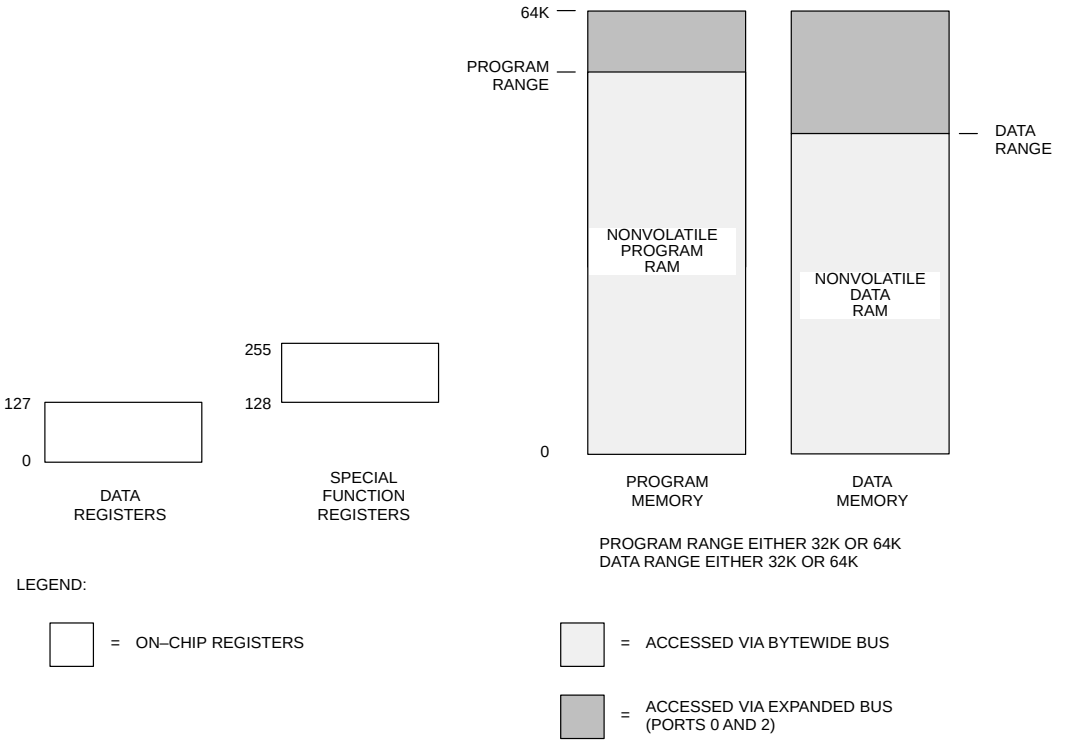
The DS5001FP executes an instruction set that is object code compatible with the industry standard 8051 microcontroller. As a result, software development packages such as assemblers and compilers that have been written for the 8051 are compatible with the DS5001FP. A complete description of the instruction set and operation are provided in the User's Guide section of the Secure Microcontroller Data Book.

Also note that the DS5001FP is embodied in the DS2251T module. The DS2251T combines the DS5001FP with between 32K and 128K of SRAM, a lithium cell, and a real time clock. This is packaged in a 72–pin SIMM module.

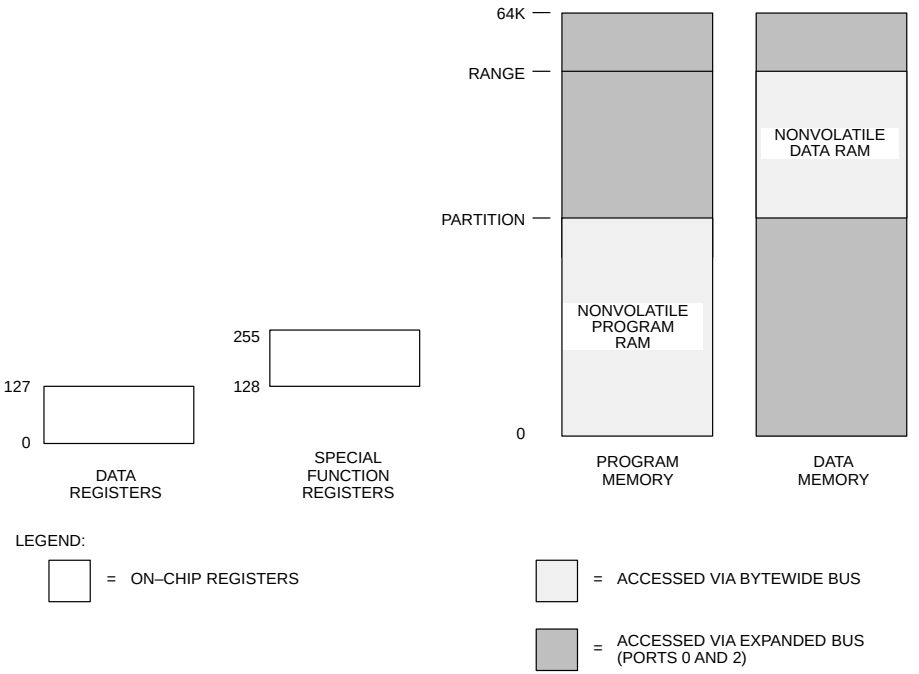
MEMORY ORGANIZATION

Figure 2 illustrates the memory map accessed by the DS5001FP. The entire 64K of program and 64K of data are potentially available to the Byte–wide bus. This preserves the I/O ports for application use. The user controls the portion of memory that is actually mapped to the Byte–wide bus by selecting the Program Range and Data Range. Any area not mapped into the NV RAM is reached via the Expanded bus on Ports 0 and 2. An alternate configuration allows dynamic Partitioning of a 64K space as shown in Figure 3. Selecting PES=1 provides another 64K of potential data storage or memory mapped peripheral space as shown in Figure 4. These selections are made using Special Function Registers. The memory map and its controls are covered in detail in the User's Guide section of the Secure Microcontroller Data Book.

DS5001FP MEMORY MAP IN NON–PARTITIONABLE MODE (PM=1) Figure 2



DS5001FP MEMORY MAP IN PARTITIONABLE MODE (PM=0) Figure 3



NOTE: Partitionable mode is not supported when MSEL pin = 0 (128KB mode).

DS5001FP MEMORY MAP WITH PES=1 Figure 4

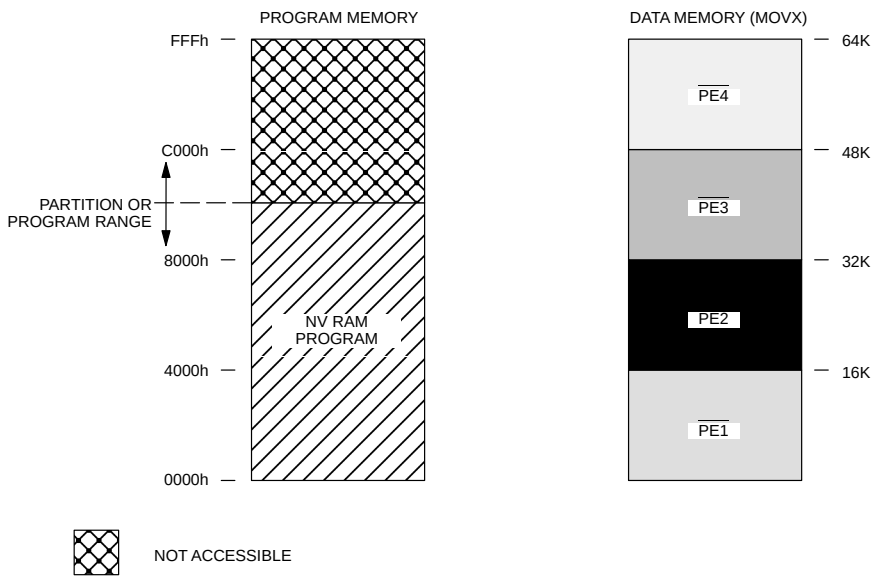
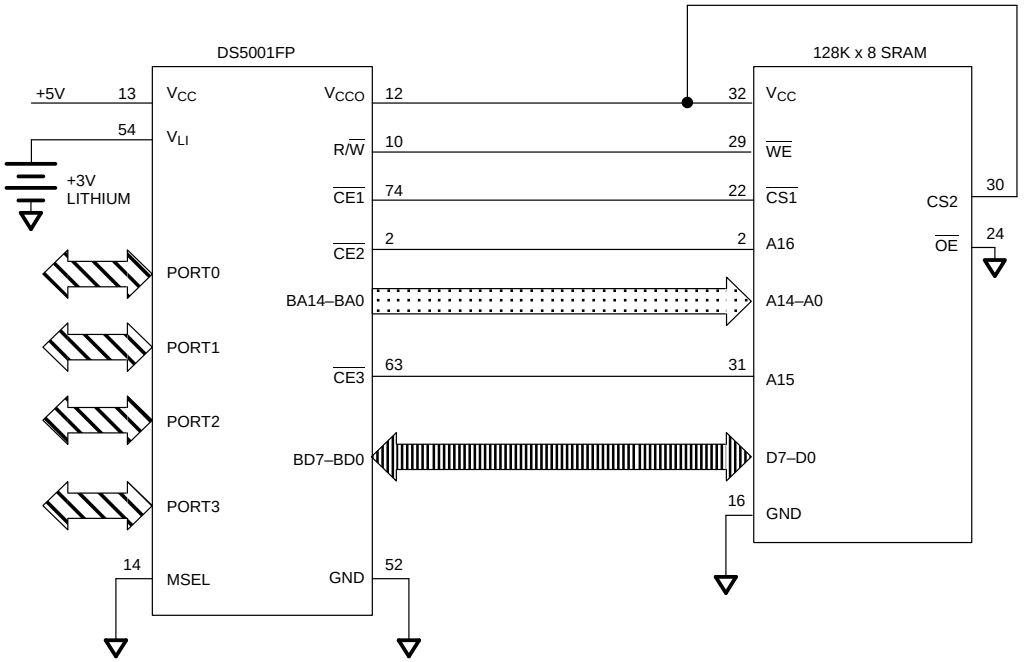
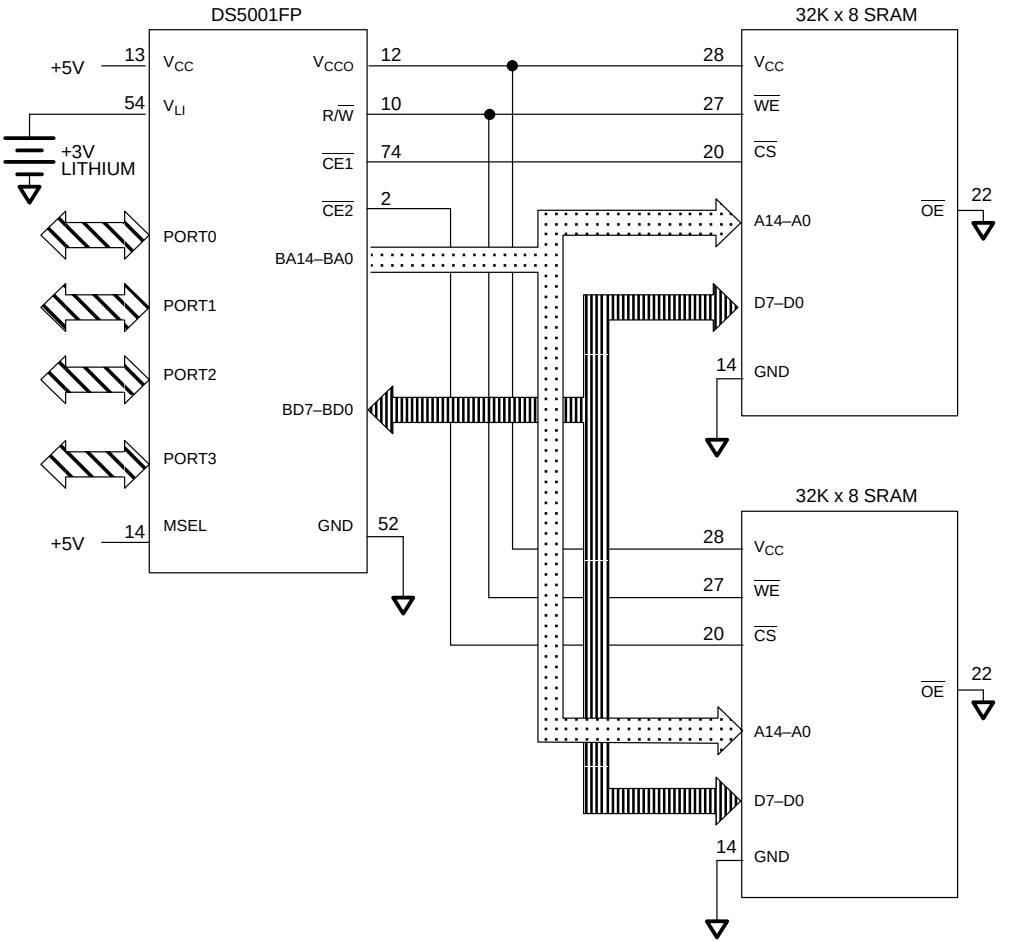


Figure 5 illustrates a typical memory connection for a system using a 128K byte SRAM. Note that in this configuration, both program and data are stored in a common RAM chip Figure 6 shows a similar system with using two 32K byte SRAMs. The Byte–wide Address bus connects to the SRAM address lines. The bi–directional Byte–wide data bus connects the data I/O lines of the SRAM.

DS5001FP CONNECTION TO 128K X 8 SRAM Figure 5



DS5001FP CONNECTION TO 64K X 8 SRAM Figure 6



POWER MANAGEMENT

The DS5001FP monitors V_{CC} to provide Power–fail Reset, early warning Power–fail Interrupt, and switch over to lithium backup. It uses an internal band–gap reference in determining the switch points. These are called V_{PFW}, V_{CCMIN}, and V_{LI} respectively. When V_{CC} drops below V_{PFW}, the DS5001FP will perform an interrupt vector to location 2Bh if the power fail warning was enabled. Full processor operation continues regardless. When power falls further to V_{CCMIN}, the DS5001FP invokes a reset state. No further code execution will be performed unless power rises back above V_{CCMIN}. All decoded chip enables and the R/$\overline{W}$ signal go to an inactive (logic 1) state. V_{CC} is still the power source at this time. When V_{CC} drops further to below V_{LI}, internal circuitry will switch to the lithium cell for power. The majority of internal circuits will be disabled and the remaining nonvolatile states will be retained. Any devices connected to V_{CCO} will be powered by the lithium cell at this time. V_{CCO} will be at the lithium battery voltage less a diode drop. This drop will vary depending on the load. Low power SRAMs should be used for this reason. When using the DS5001FP, the user must select the appropriate battery to match the RAM data retention current and the desired backup lifetime. Note that the lithium cell is only loaded when $V_{CC} < V_{LI}$. The User's Guide has more information on this topic. The trip points V_{CCMIN} and V_{PFW} are listed in the electrical specifications.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC CHARACTERISTICS

(t_A=0°C to 70°C; V_{CC}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Low Voltage	V_{IL}	–0.3		+0.8	V	1
Input High Voltage	V_{IH1}	2.0		V_{CC}+0.3	V	1
Input High Voltage (RST, XTAL1, $\overline{PROG}$)	V_{IH2}	3.5		V_{CC}+0.3	V	1
Output Low Voltage @ I_{OL}=1.6 mA (Ports 1, 2, 3)	V_{OL1}		0.15	0.45	V	
Output Low Voltage @ I_{OL}=3.2 mA (Port 0, ALE, $\overline{PSEN}$, $\overline{PF}$, BA15–0, BD7–0, R/$\overline{W}$, $\overline{CE1N}$, $\overline{CE}$1–4, $\overline{PE}$1–4, V_{RST})	V_{OL2}		0.15	0.45	V	1
Output High Voltage @ I_{OH}=–80 µA (Ports 1, 2, 3)	V_{OH1}	2.4	4.8		V	1
Output High Voltage @ I_{OH}=–400 µA (Ports 0, ALE, $\overline{PSEN}$, $\overline{PF}$, BA15–0, BD7–0, R/$\overline{W}$, $\overline{CE1N}$, $\overline{CE}$1–4, $\overline{PE}$1–4)	V_{OH2}	2.4	4.8		V	1
Input Low Current V_{IN}=0.45V (Ports 1, 2, 3)	I_{IL}			–50	µA	
Transition Current; 1 to 0 V_{IN}=2.0V (Ports 1, 2, 3) (0°C to 70°C)	I_{TL}			–500	µA	
Transition Current; 1 to 0 V_{IN}=2.0V (Ports 1, 2, 3) (–40°C to +85°C)	I_{TL}			–600	µA	10

DC CHARACTERISTICS (cont'd) (t_A=0°C to 70°C; V_{CC}=5V ± 10%)

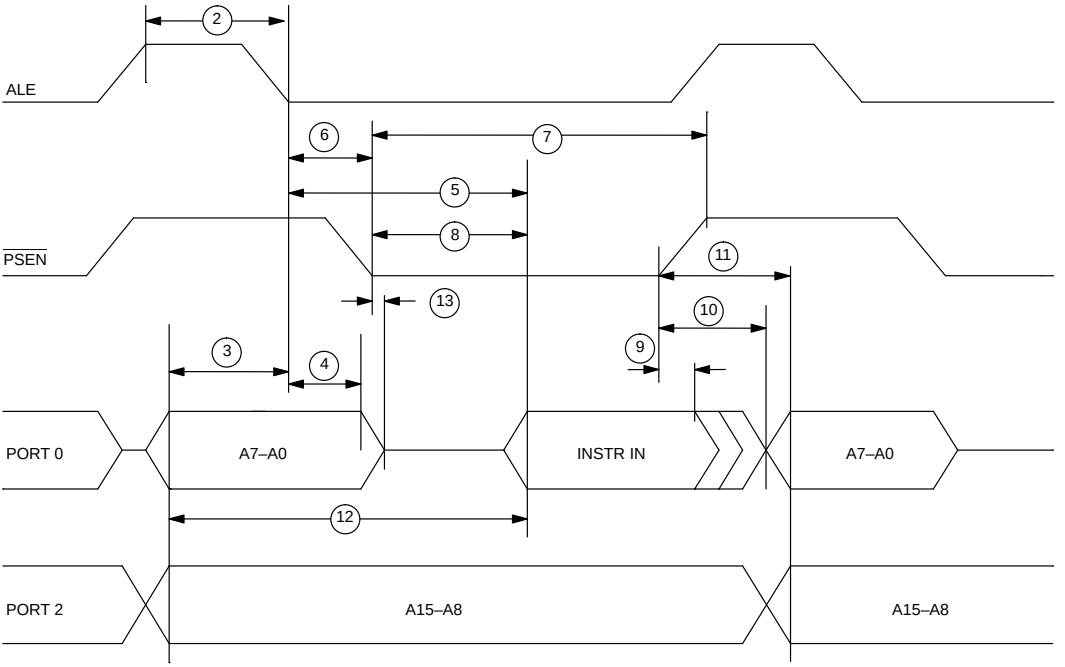
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current 0.45 < V_{IN} < V_{CC} (Port 0, MSEL)	I_{IL}			±10	µA	
RST Pull–down Resistor (0°C to 70°C)	R_{RE}	40		150	KΩ	
RST Pull–down Resistor (–40°C to +85°C)	R_{RE}	40		180	KΩ	10
$\overline{VRST}$ Pull–up Resistor	R_{VR}		4.7		KΩ	
$\overline{PROG}$ Pull–up Resistor	R_{PR}		40		KΩ	
Power–Fail Warning Voltage (0°C to 70°C)	V_{PFW}	4.25	4.37	4.50	V	1
Power–Fail Warning Voltage (–40°C to +85°C)	V_{PFW}	4.1	4.37	4.5	V	1, 10
Minimum Operating Voltage (0°C to 70°C)	V_{CCMIN}	4.00	4.12	4.25	V	1
Minimum Operating Voltage (–40°C to +85°C)	V_{CCMIN}	3.85	4.09	4.25	V	1, 10
Lithium Supply Voltage	V_{LI}	2.5		4.0	V	1
Operating Current @ 16 MHz	I_{CC}			36	mA	2
Idle Mode Current @ 12 MHz (0°C to 70°C)	I_{IDLE}			7.0	mA	3
Idle Mode Current @ 12 MHz (–40°C to +85°C)	I_{IDLE}			8.0	mA	3, 10
Stop Mode Current	I_{STOP}			80	µA	4
Pin Capacitance	C_{IN}			10	pF	5
Output Supply Voltage (V_{CCO})	V_{CCO1}	V_{CC}–0.35			V	1, 2
Output Supply Battery–backed Mode (V_{CCO}, $\overline{CE}$1–4, $\overline{PE}$1–2) (0°C to 70°C)	V_{CCO2}	V_{LI}–0.65			V	1, 8
Output Supply Battery–backed Mode (V_{CCO}, $\overline{CE}$1–4, $\overline{PE}$1–2) (–40°C to +85°C)	V_{CCO2}	V_{LI}–0.9			V	1, 8, 10
Output Supply Current @ V_{CCO}=V_{CC} – 0.3V	I_{CCO1}			75	mA	6
Lithium–backed Quiescent Current	I_{LI}		5	75	nA	7
Reset Trip Point in Stop Mode w/BAT=3.0V (0°C to 70°C) w/BAT=3.0V (–40°C to +85°C) w/BAT=3.3V (0°C to 70°C)		 4.0 3.85 4.4		 4.25 4.25 4.65		 1 1, 10 1

AC CHARACTERISTICS
EXPANDED BUS MODE TIMING SPECIFICATIONS

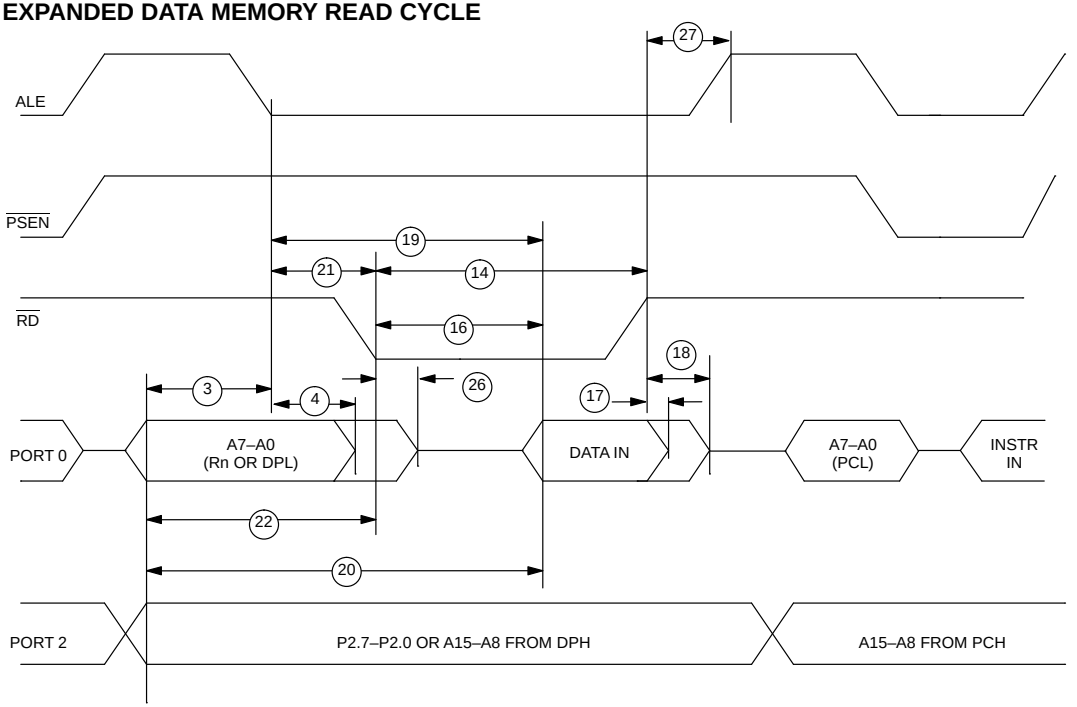
(t_A=0°C to70°C; V_{CC}=5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
1	Oscillator Frequency	$1/t_{CLK}$	1.0	16	MHz
2	ALE Pulse Width	t_{ALPW}	$2t_{CLK}$–40		ns
3	Address Valid to ALE Low	t_{AVALL}	t_{CLK}–40		ns
4	Address Hold After ALE Low	t_{AVAAV}	t_{CLK}–35		ns
5	ALE Low to Valid Instr. In @12 MHz @16 MHz	t_{ALLVI}		$4t_{CLK}$–150 $4t_{CLK}$–90	ns
6	ALE Low to $\overline{PSEN}$ Low	t_{ALLPSL}	t_{CLK}–25		ns
7	$\overline{PSEN}$ Pulse Width	t_{PSPW}	$3t_{CLK}$–35		ns
8	$\overline{PSEN}$ Low to Valid Instr. In @12 MHz @16 MHz	t_{PSLVI}		$3t_{CLK}$–150 $3t_{CLK}$–90	ns ns
9	Input Instr. Hold after $\overline{PSEN}$ Going High	t_{PSIV}	0		ns
10	Input Instr. Float after $\overline{PSEN}$ Going High	t_{PSIX}		t_{CLK}–20	ns
11	Address Hold after $\overline{PSEN}$ Going High	t_{PSAV}	t_{CLK}–8		ns
12	Address Valid to Valid Instr. In @12 MHz @16 MHz	t_{AVVI}		$5t_{CLK}$–150 $5t_{CLK}$–90	ns ns
13	$\overline{PSEN}$ Low to Address Float	t_{PSLAZ}	0		ns
14	$\overline{RD}$ Pulse Width	t_{RDPW}	$6t_{CLK}$–100		ns
15	$\overline{WR}$ Pulse Width	t_{WRPW}	$6t_{CLK}$–100		ns
16	$\overline{RD}$ Low to Valid Data In @12 MHz @16 MHz	t_{RDLDV}		$5t_{CLK}$–165 $5t_{CLK}$–105	ns ns
17	Data Hold after $\overline{RD}$ High	t_{RDHDV}	0		ns
18	Data Float after $\overline{RD}$ High	t_{RDHDZ}		$2t_{CLK}$–70	ns
19	ALE Low to Valid Data In @12 MHz @16 MHz	t_{ALLVD}		$8t_{CLK}$–150 $8t_{CLK}$–90	ns ns
20	Valid Addr. to Valid Data In @12 MHz @16 MHz	t_{AVDV}		$9t_{CLK}$–165 $9t_{CLK}$–105	ns ns
21	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{ALLRDL}	$3t_{CLK}$–50	$3t_{CLK}$+50	ns
22	Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVRDL}	$4t_{CLK}$–130		ns
23	Data Valid to $\overline{WR}$ Going Low	t_{DVWRL}	t_{CLK}–60		ns
24	Data Valid to $\overline{WR}$ High @12 MHz @16 MHz	t_{DVWRH}	$7t_{CLK}$–150 $7t_{CLK}$–90		ns ns
25	Data Valid after $\overline{WR}$ High	t_{WRHDV}	t_{CLK}–50		ns
26	$\overline{RD}$ Low to Address Float	t_{RDLAZ}		0	ns
27	$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{RDHALH}	t_{CLK}–40	t_{CLK}+50	ns

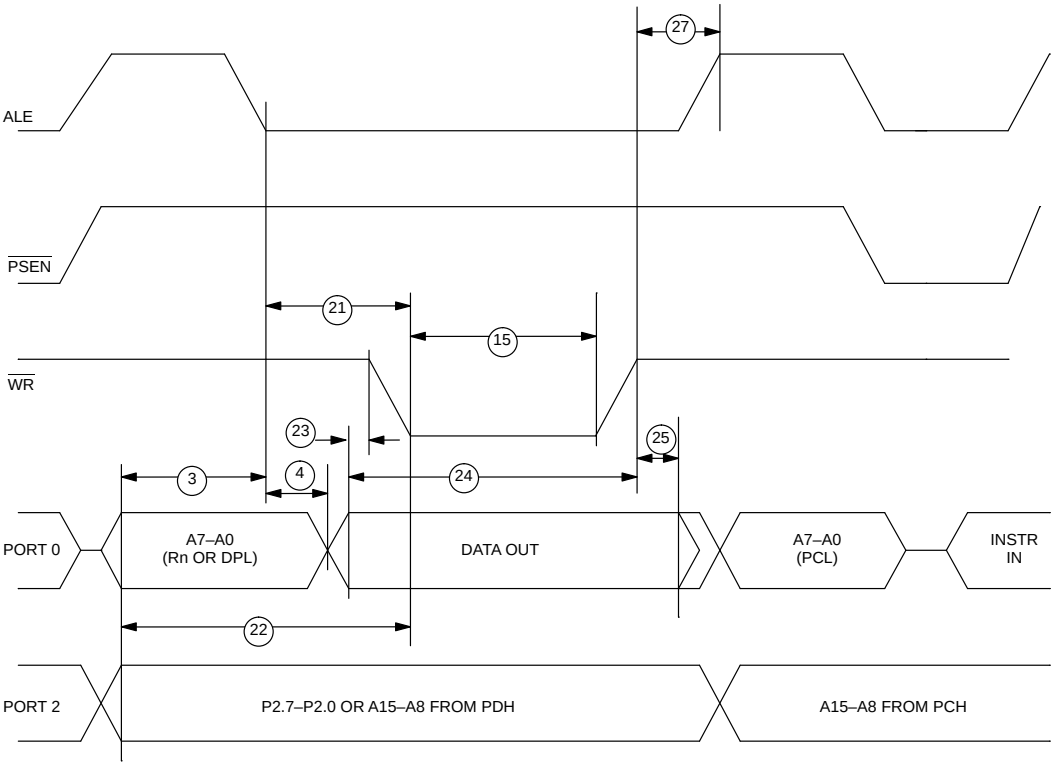
EXPANDED PROGRAM MEMORY READ CYCLE



EXPANDED DATA MEMORY READ CYCLE



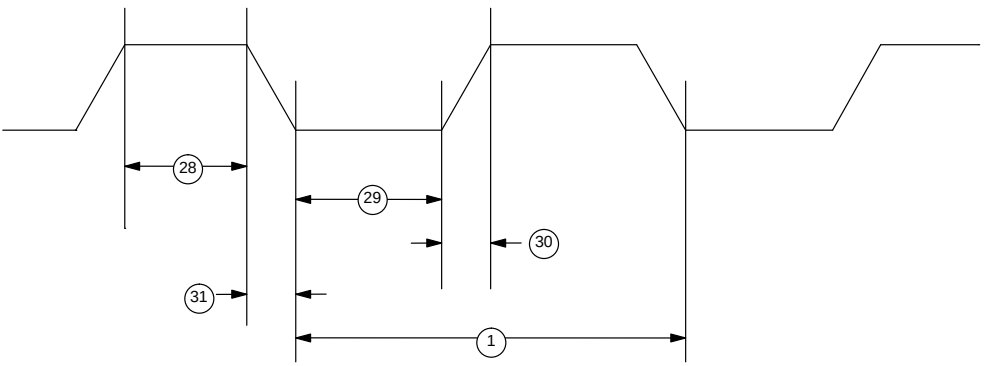
EXPANDED DATA MEMORY WRITE CYCLE



AC CHARACTERISTICS (cont'd)
EXTERNAL CLOCK DRIVE (t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER		SYMBOL	MIN	MAX	UNITS
28	External Clock High Time	@12 MHz @16 MHz	t_{CLKHPW}	20 15		ns ns
29	External Clock Low Time	@12 MHz @16 MHz	t_{CLKLPW}	20 15		ns ns
30	External Clock Rise Time	@12 MHz @16 MHz	t_{CLKR}		20 15	ns ns
31	External Clock Fall Time	@12 MHz @16 MHz	t_{CLKF}		20 15	ns ns

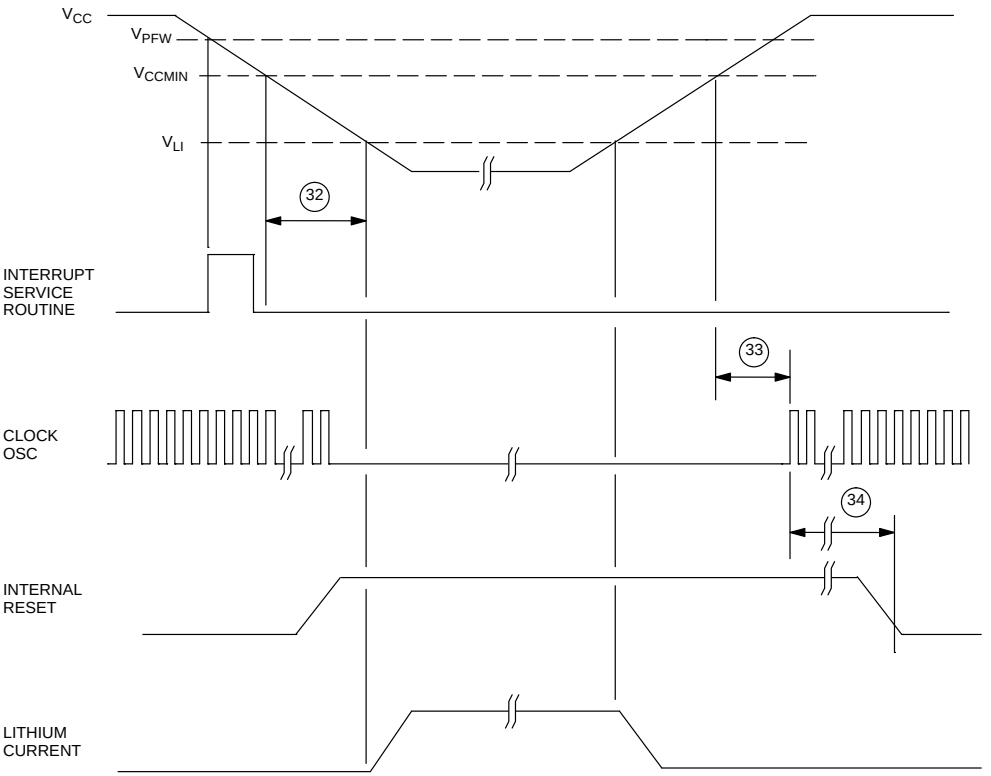
EXTERNAL CLOCK TIMING



AC CHARACTERISTICS (cont'd)
POWER CYCLING TIMING (t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
32	Slew Rate from V_{CCmin} to V_{LI}	t_F	130		µs
33	Crystal Start–up Time	t_{CSU}		(note 9)	
34	Power–On Reset Delay	t_{POR}		21504	t_{CLK}

POWER CYCLE TIMING

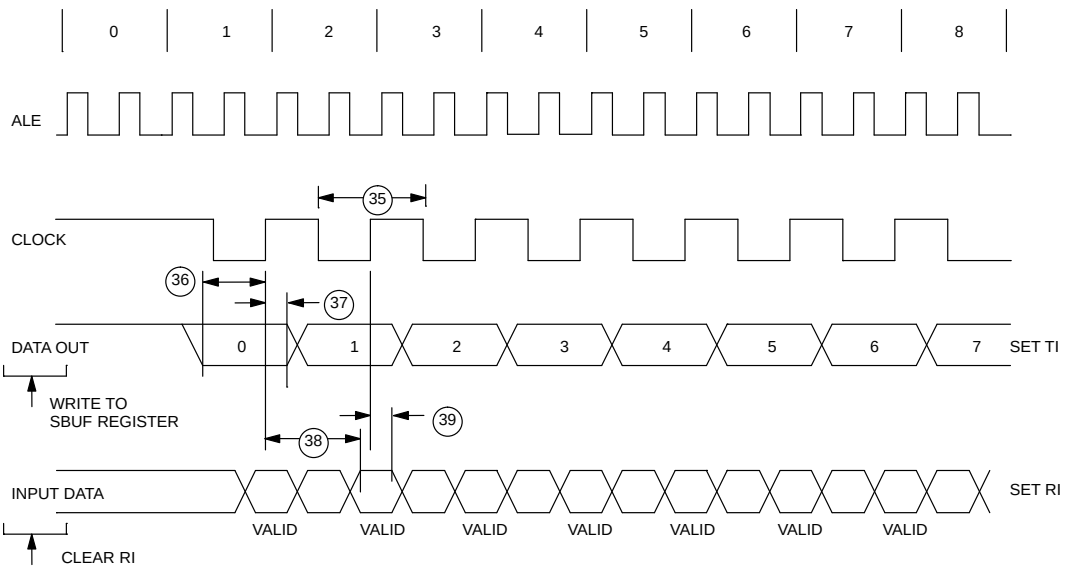


AC CHARACTERISTICS (cont'd)
SERIAL PORT TIMING – MODE 0

(t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
35	Serial Port Clock Cycle Time	t_{SPCLK}	$12t_{CLK}$		µs
36	Output Data Setup to Rising Clock Edge	t_{DOCH}	$10t_{CLK}$–133		ns
37	Output Data Hold after Rising Clock Edge	t_{CHDO}	$2t_{CLK}$–117		ns
38	Clock Rising Edge to Input Data Valid	t_{CHDV}		$10t_{CLK}$–133	ns
39	Input Data Hold after Rising Clock Edge	t_{CHDIV}	0		ns

SERIAL PORT TIMING – MODE 0

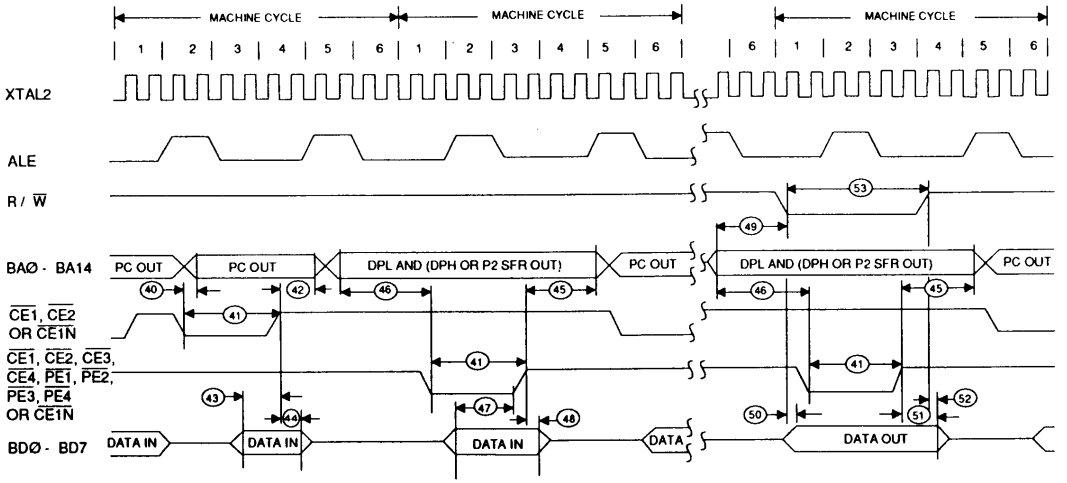


AC CHARACTERISTICS
BYTEWIDE ADDRESS/DATA BUS TIMING

(t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
40	Delay to Byte–wide Address Valid from $\overline{CE1}$, $\overline{CE2}$ or $\overline{CE1N}$ Low During Opcode Fetch	t_{CE1LPA}		30	ns
41	Pulse Width of $\overline{CE}$1–4, $\overline{PE}$1–4 or $\overline{CE1N}$	t_{CEPW}	$4t_{CLK}$–35		ns
42	Byte–wide Address Hold After $\overline{CE1}$, $\overline{CE2}$ or $\overline{CE1N}$ High During Opcode Fetch	t_{CE1HPA}	$2t_{CLK}$–20		ns
43	Byte–wide Data Setup to $\overline{CE1}$, $\overline{CE2}$ or $\overline{CE1N}$ High During Opcode Fetch	t_{OVCE1H}	$1t_{CLK}$+40		ns
44	Byte–wide Data Hold After $\overline{CE1}$, $\overline{CE2}$ or $\overline{CE1N}$ High During Opcode Fetch	t_{CE1HOV}	10		ns
45	Byte–wide Address Hold After $\overline{CE}$1–4, $\overline{PE}$1–4, or $\overline{CE1N}$ High During MOVX	t_{CEHDA}	$4t_{CLK}$–30		ns
46	Delay from Bytewide Address Valid $\overline{CE}$1–4, $\overline{PE}$1–4, or $\overline{CE1N}$ Low During MOVX	t_{CELDA}	$4t_{CLK}$–35		ns
47	Bytewide Data Setup to $\overline{CE}$1–4, $\overline{PE}$1–4, or $\overline{CE1N}$ High During MOVX (read)	t_{DACEH}	$1t_{CLK}$+40		ns
48	Bytewide Data Hold After $\overline{CE}$1–4, $\overline{PE}$1–4, or $\overline{CE1N}$ High During MOVX (read)	t_{CEHDV}	10		ns
49	Bytewide Address Valid to R/$\overline{W}$ Active During MOVX (write)	t_{AVRWL}	$3t_{CLK}$–35		ns
50	Delay from R/$\overline{W}$ Low to Valid Data Out During MOVX (write)	t_{RWLDV}	20		ns
51	Valid Data Out Hold Time from $\overline{CE}$1–4, $\overline{PE}$1–4, or $\overline{CE1N}$ High	t_{CEHDV}	$1t_{CLK}$–15		ns
52	Valid Data Out Hold Time from R/$\overline{W}$ High	t_{RWHDV}	0		ns
53	Write Pulse Width (R/$\overline{W}$ Low Time)	t_{RWLPW}	$6t_{CLK}$–20		ns

BYTEWIDE BUS TIMING



RPC AC CHARACTERISTICS – DBB READ

(t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
54	$\overline{CS}$, A_0 Setup to $\overline{RD}$	t_{AR}	0		ns
55	$\overline{CS}$, A_0 Hold After $\overline{RD}$	t_{RA}	0		ns
56	$\overline{RD}$ Pulse Width	t_{RR}	160		ns
57	$\overline{CS}$, A_0 to Data Out Delay	t_{AD}		130	ns
58	$\overline{RD}$ to Data Out Delay	t_{RD}	0	130	ns
59	$\overline{RD}$ to Data Float Delay	t_{RDZ}		85	ns

RPC AC CHARACTERISTICS – DBB WRITE (t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
60	$\overline{CS}$, A_0 Setup to $\overline{WR}$	t_{AW}	0		ns
61A	$\overline{CS}$, Hold After $\overline{WR}$	t_{WA}	0		ns
61B	A_0, Hold After $\overline{WR}$	t_{WA}	20		ns
62	$\overline{WR}$ Pulse Width	t_{WW}	160		ns
63	Data Setup to $\overline{WR}$	t_{DW}	130		ns
64	Data Hold After $\overline{WR}$	t_{WD}	20		ns

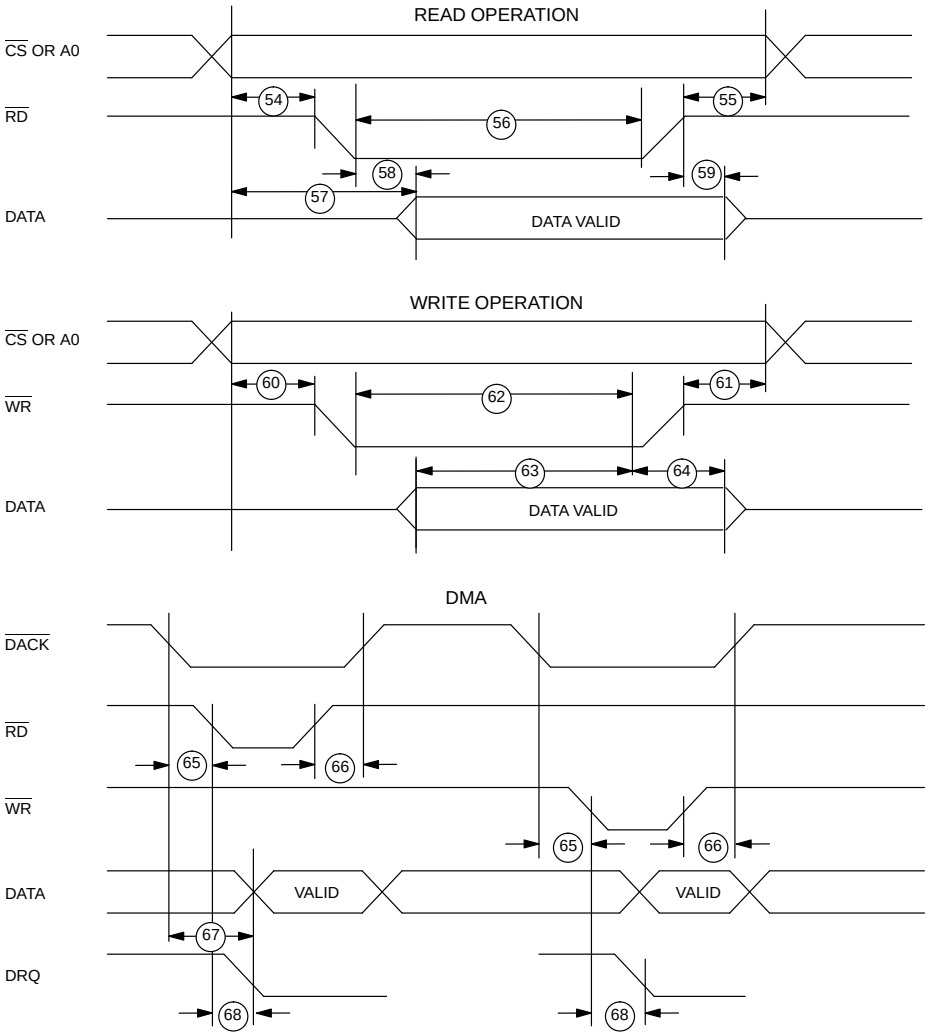
AC CHARACTERISTICS – DMA (t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
65	$\overline{DACK}$ to $\overline{WR}$ or $\overline{RD}$	t_{ACC}	0		ns
66	$\overline{RD}$ or $\overline{WR}$ to $\overline{DACK}$	t_{CAC}	0		ns
67	$\overline{DACK}$ to Data Valid	t_{ACD}	0	130	ns
68	$\overline{RD}$ or $\overline{WR}$ to DRQ Cleared	t_{CRQ}		110	ns

AC CHARACTERISTICS – $\overline{PROG}$ (t_A = 0°C to70°C; V_{CC} = 5V ± 10%)

#	PARAMETER	SYMBOL	MIN	MAX	UNITS
69	$\overline{PROG}$ Low to Active	t_{PRA}	48		CLKS
70	$\overline{PROG}$ High to Inactive	t_{PRI}	48		CLKS

RPC TIMING MODE

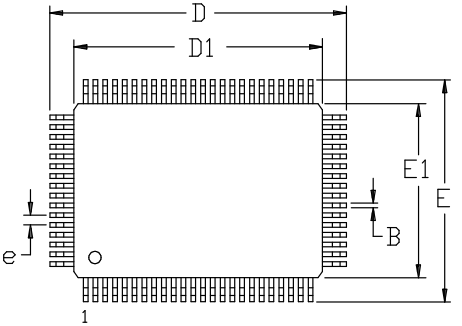


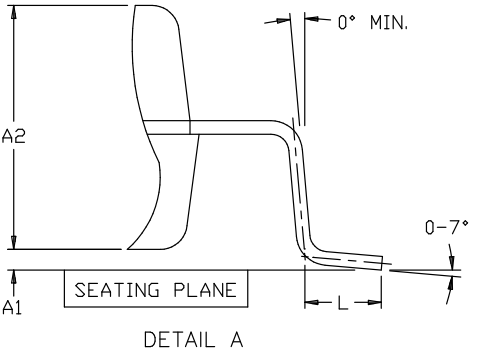
NOTES:
All parameters apply to both commercial and industrial temperature operation unless otherwise noted.

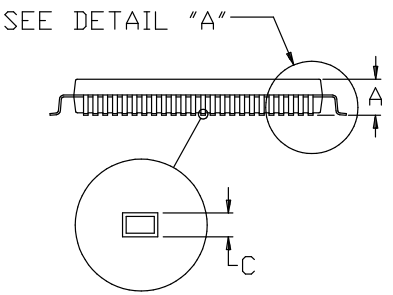
1. All voltages are referenced to ground.
2. Maximum operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with t_{CLKR}, t_{CLKF}=10 ns, V_{IL} = 0.5V; XTAL2 disconnected; RST = PORT0 = V_{CC}, MSEL = V_{SS}.
3. Idle mode I_{IDLE} is measured with all output pins disconnected; XTAL1 driven with t_{CLKR}, t_{CLKF} = 10 ns, V_{IL} = 0.5V; XTAL2 disconnected; PORT0 = V_{CC}, RST = MSEL = V_{SS}.
4. Stop mode I_{STOP} is measured with all output pins disconnected; PORT0 = V_{CC}; XTAL2 not connected; RST = MSEL = XTAL1 = V_{SS}.

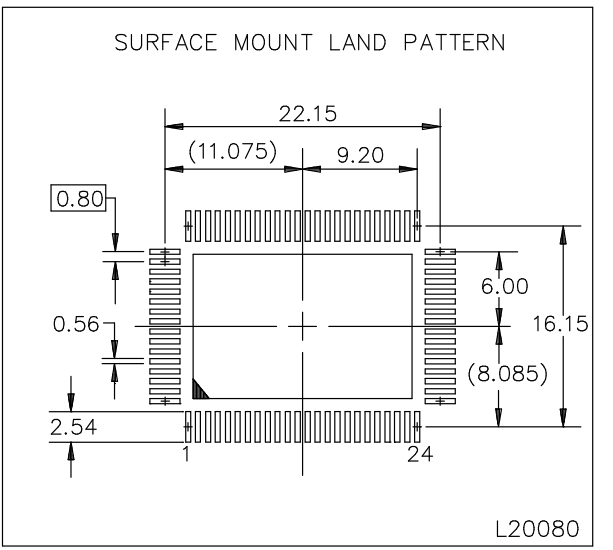
5. Pin Capacitance is measured with a test frequency – 1 MHz, t_A = 25°C.
6. I_{CCO1} is the maximum average operating current that can be drawn from V_{CCO} in normal operation.
7. I_{LI} is the current drawn from V_{LI} input when V_{CC} = 0V and V_{CCO} is disconnected.
8. V_{CCO2} is measured with $V_{CC} < V_{LI}$, and a maximum load of 10 µA on V_{CCO}.
9. Crystal start–up time is the time required to get the mass of the crystal into vibrational motion from the time that power is first applied to the circuit until the first clock pulse is produced by the on–chip oscillator. The user should check with the crystal vendor for a worst case specification on this time.
10. This parameter applies to industrial temperature operation.

DS50001FP CMOS MICROPROCESSOR









DIM	MILLIMETERS	
	MIN	MAX
A	–	3.15
A1	0.25	–
A2	2.55	2.87
B	0.30	0.50
C	0.13	0.23
D	23.70	24.10
D1	19.90	20.10
E	17.40	18.10
E1	13.90	14.10
e	0.80 BSC	
L	0.65	0.95

56–G4005–001

DATA SHEET REVISION SUMMARY

The following represent the key differences between 11/27/95 and 07/24/96 version of the DS50001FP data sheet. Please review this summary carefully.

1. Change V_{CC02} specification from V_{LI} – 0.5 to V_{LI} – 0.65 (PCN F62501).
2. Update mechanical specifications.

The following represent the key differences between 07/24/96 and 11/19/96 version of the DS50001FP data sheet. Please review this summary carefully.

1. Change V_{CC01} from V_{CC}–0.3 to V_{CC}–0.35.