

DATA SHEET

BF909A; BF909AR **Dual-gate MOS-FETs**

Preliminary specification
File under Discrete Semiconductors, SC07

1998 Mar 06

Dual-gate MOS-FETs

BF909A; BF909AR

FEATURES

- Specially designed for use at 5 V supply voltage
- High forward transfer admittance
- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz
- Superior cross-modulation performance during AGC.

APPLICATIONS

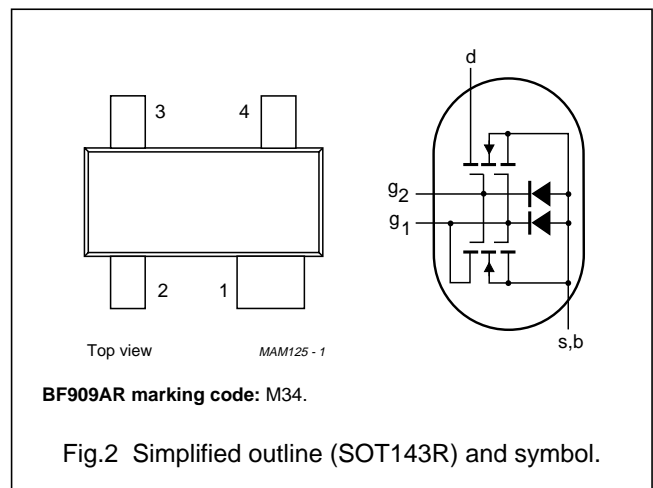
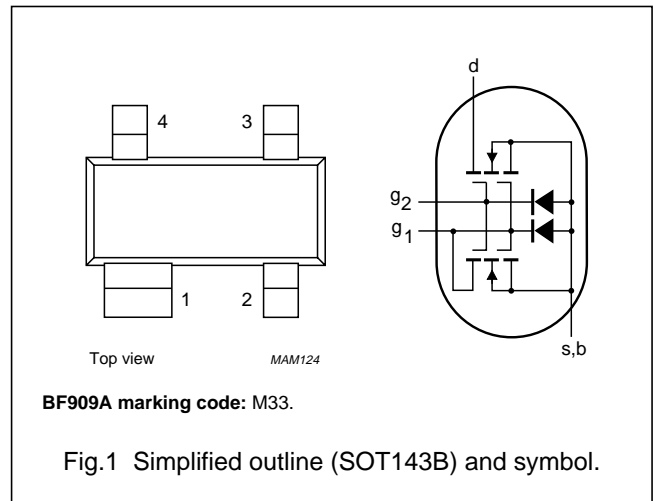
- VHF and UHF applications with 3 to 7 V supply voltage such as television tuners and professional communications equipment.

DESCRIPTION

Enhancement type field-effect transistor in a plastic microminiature SOT143B or SOT143R package. The transistor consists of an amplifier MOS-FET with source and substrate interconnected and an internal bias circuit to ensure good cross-modulation performance during AGC.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g ₂	gate 2
4	g ₁	gate 1



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{DS}	drain-source voltage		–	–	7	V
I _D	drain current		–	–	40	mA
P _{tot}	total power dissipation		–	–	200	mW
T _j	operating junction temperature		–	–	150	°C
y _{fs}	forward transfer admittance		36	43	50	mS
C _{ig1-s}	input capacitance at gate 1		–	3.6	4.3	pF
C _{rs}	reverse transfer capacitance	f = 1 MHz	–	35	50	fF
F	noise figure	f = 800 MHz	–	2	2.8	dB

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A, and SNW-FQ-302B.

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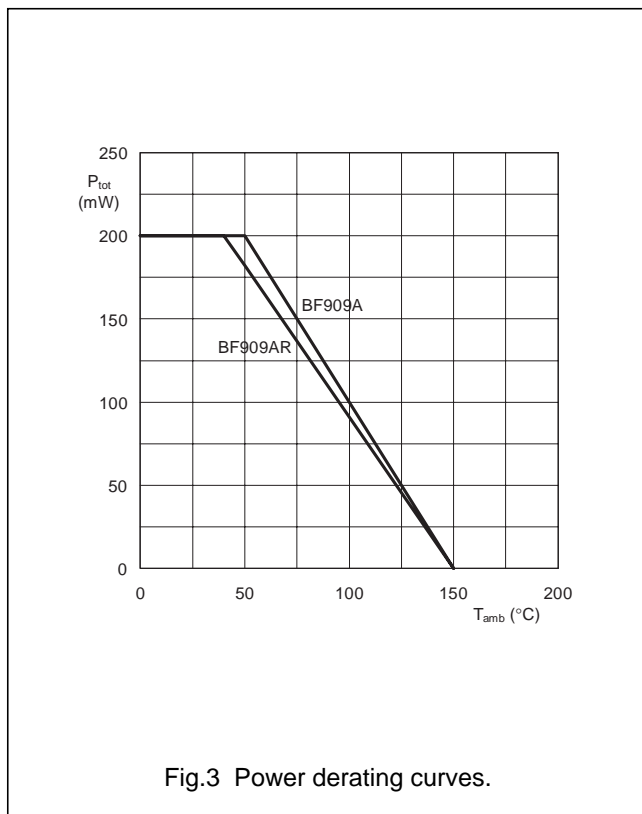
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{DS}	drain-source voltage		–	7	V
I _D	drain current		–	40	mA
I _{G1}	gate 1 current		–	±10	mA
I _{G2}	gate 2 current		–	±10	mA
P _{tot}	total power dissipation BF909A BF909AR	see Fig.3 T _{amb} ≤ 50 °C; note 1 T _{amb} ≤ 40 °C; note 1	– –	200 200	mW mW
T _{stg}	storage temperature		–65	+150	°C
T _j	operating junction temperature		–	150	°C

Note

1. Device mounted on a printed-circuit board.



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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1		
	BF909A		500	K/W
	BF909AR		550	K/W
$R_{th\ j-s}$	thermal resistance from junction to soldering point	note 2		
	BF909A	$T_s = 92\text{ °C}$	290	K/W
	BF909AR	$T_s = 78\text{ °C}$	360	K/W

Notes

1. Device mounted on a printed-circuit board.
2. T_s is the temperature at the soldering point of the source lead.

STATIC CHARACTERISTICS

$T_j = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)G1-SS}$	gate 1-source breakdown voltage	$V_{G2-S} = V_{DS} = 0$; $I_{G1-S} = 10\text{ mA}$	6	15	V
$V_{(BR)G2-SS}$	gate 2-source breakdown voltage	$V_{G1-S} = V_{DS} = 0$; $I_{G2-S} = 10\text{ mA}$	6	15	V
$V_{(F)S-G1}$	forward source-gate 1 voltage	$V_{G2-S} = V_{DS} = 0$; $I_{S-G1} = 10\text{ mA}$	0.5	1.5	V
$V_{(F)S-G2}$	forward source-gate 2 voltage	$V_{G1-S} = V_{DS} = 0$; $I_{S-G2} = 10\text{ mA}$	0.5	1.5	V
$V_{G1-S(th)}$	gate 1-source threshold voltage	$V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $I_D = 20\text{ }\mu\text{A}$	0.3	1	V
$V_{G2-S(th)}$	gate 2-source threshold voltage	$V_{G1-S} = V_{DS} = 5\text{ V}$; $I_D = 20\text{ }\mu\text{A}$	0.3	1.2	V
I_{DSX}	drain-source current	$V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $R_{G1} = 120\text{ k}\Omega$; note 1	12	20	mA
I_{G1-SS}	gate 1 cut-off current	$V_{G1-S} = 5\text{ V}$; $V_{G2-S} = V_{DS} = 0$	–	50	nA
I_{G2-SS}	gate 2 cut-off current	$V_{G2-S} = 5\text{ V}$; $V_{G1-S} = V_{DS} = 0$	–	50	nA

Note

1. R_{G1} connects gate 1 to $V_{GG} = 5\text{ V}$; see Fig.18.

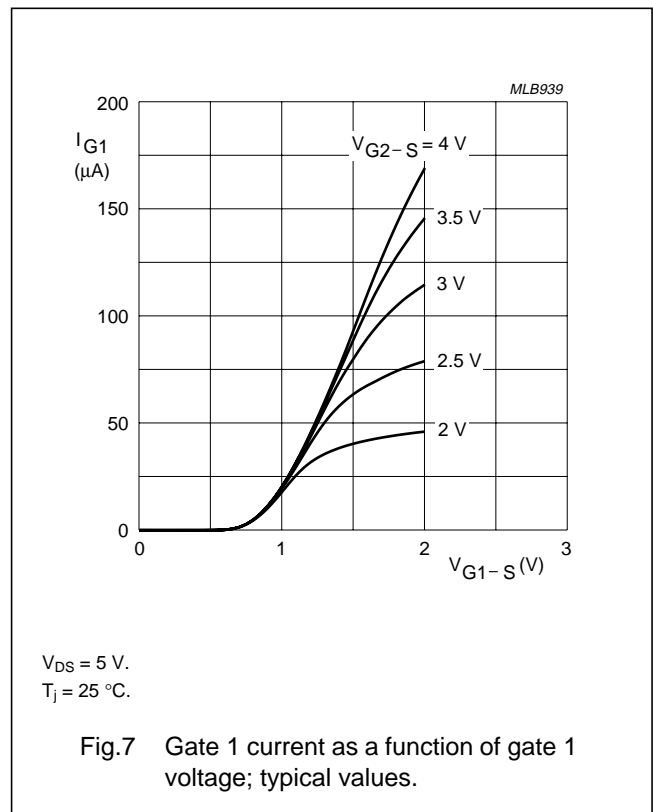
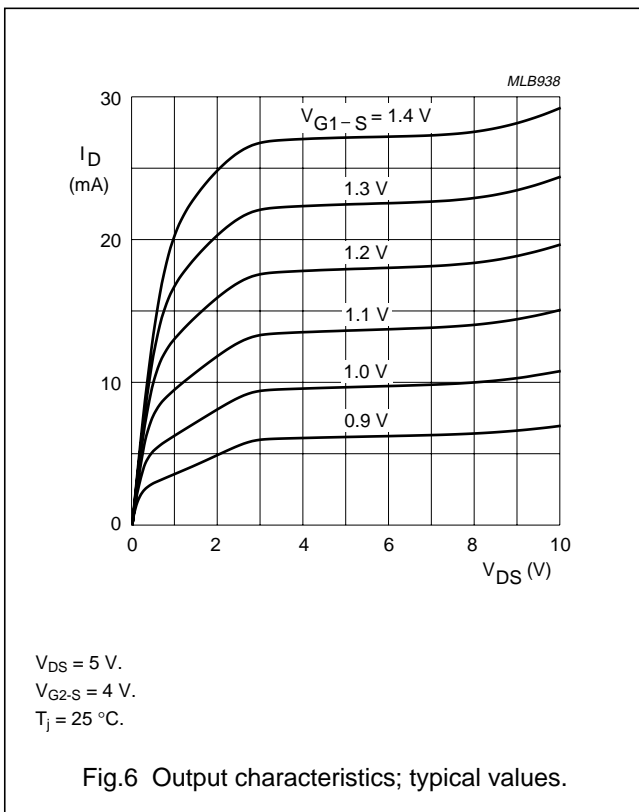
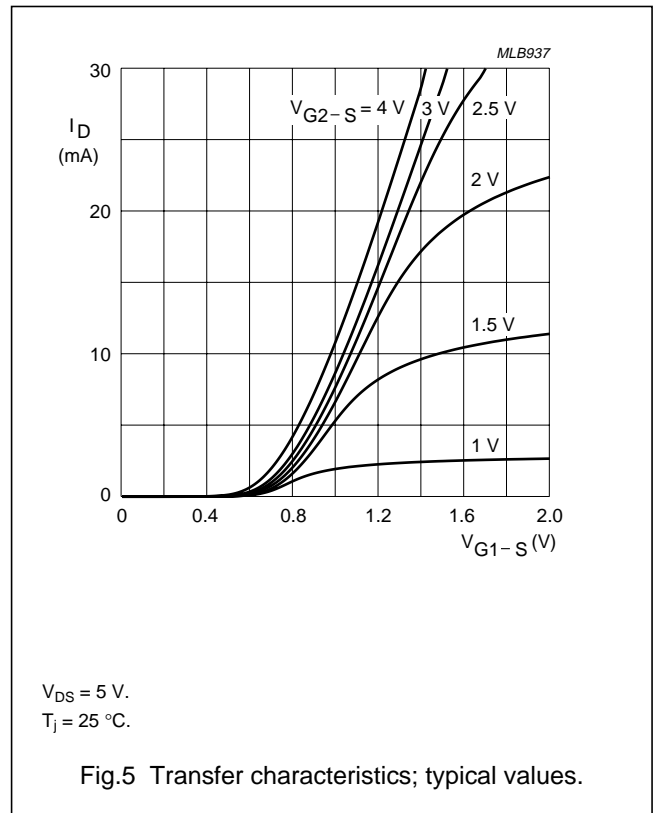
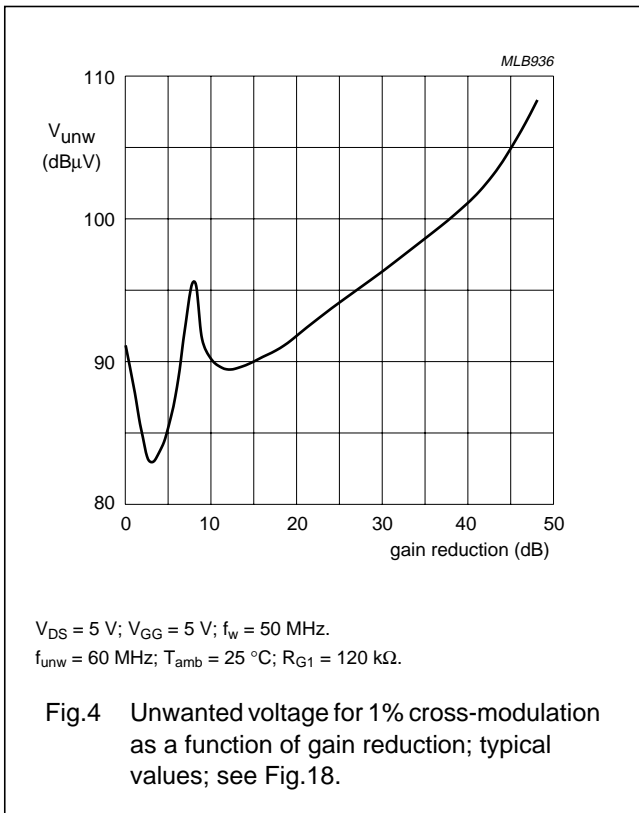
DYNAMIC CHARACTERISTICS

Common source; $T_{amb} = 25\text{ °C}$; $V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 15\text{ mA}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$ y_{fs} $	forward transfer admittance	pulsed; $T_j = 25\text{ °C}$	36	43	50	mS
C_{ig1-s}	input capacitance at gate 1	$f = 1\text{ MHz}$	–	3.6	4.3	pF
C_{ig2-s}	input capacitance at gate 2	$f = 1\text{ MHz}$	–	2.3	3	pF
C_{os}	drain-source capacitance	$f = 1\text{ MHz}$	–	2.4	3	pF
C_{rs}	reverse transfer capacitance	$f = 1\text{ MHz}$	–	35	50	fF
F	noise figure	$f = 800\text{ MHz}$; $G_S = G_{Sopt}$; $B_S = B_{Sopt}$	–	2	2.8	dB

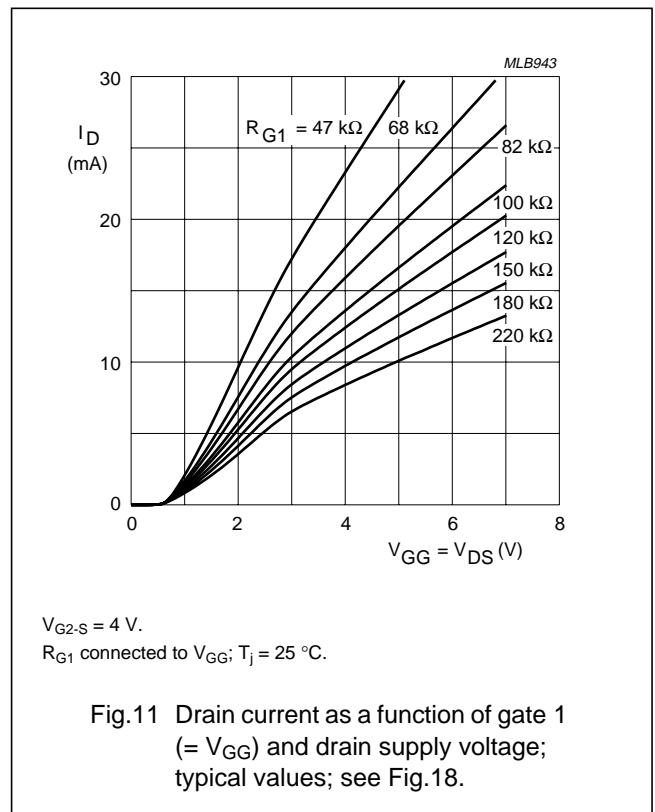
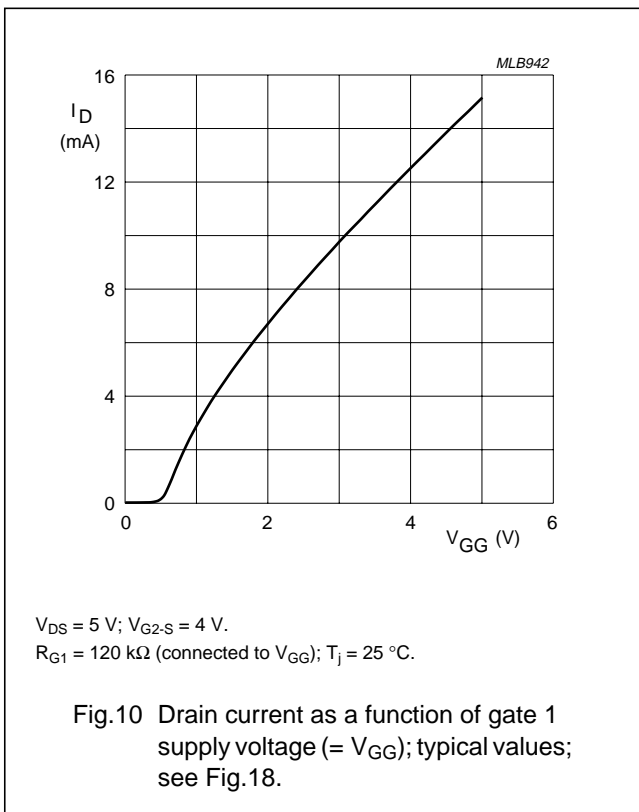
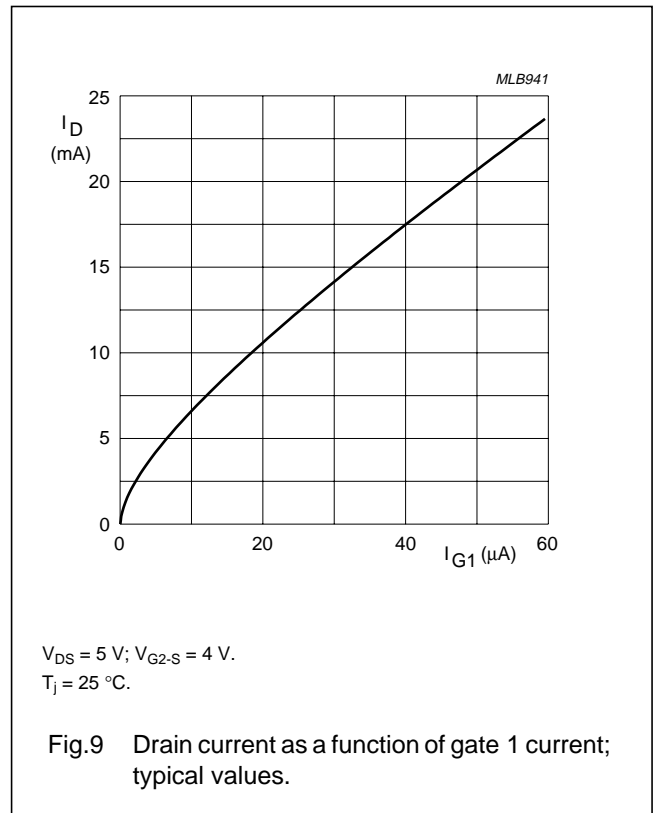
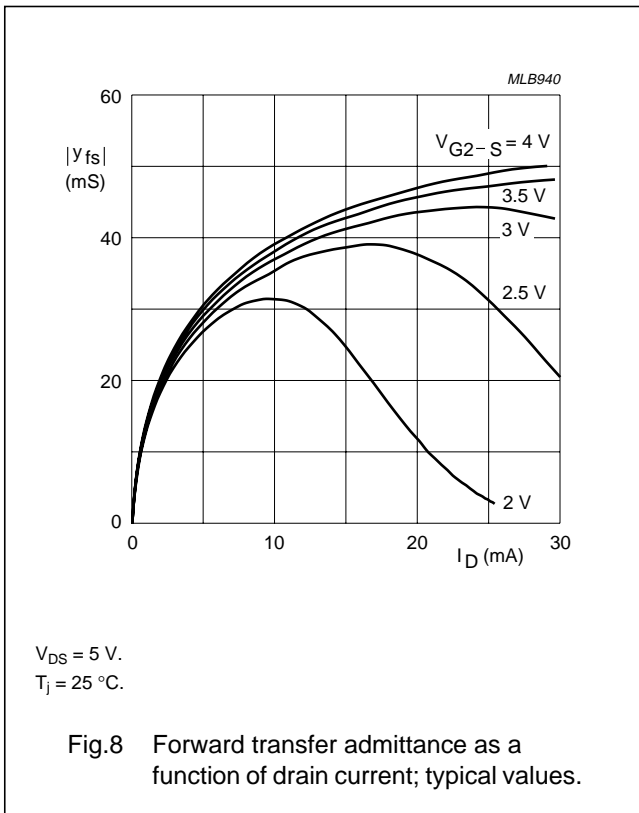
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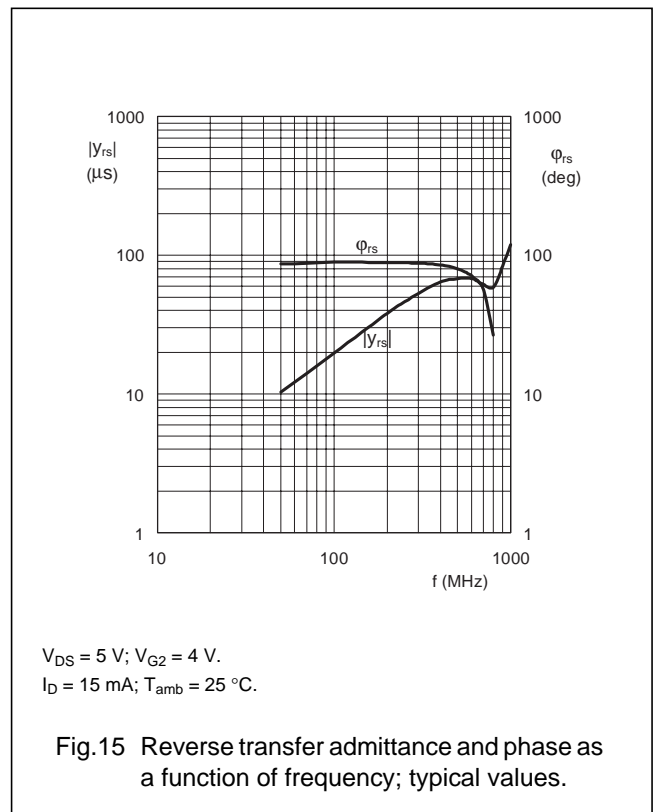
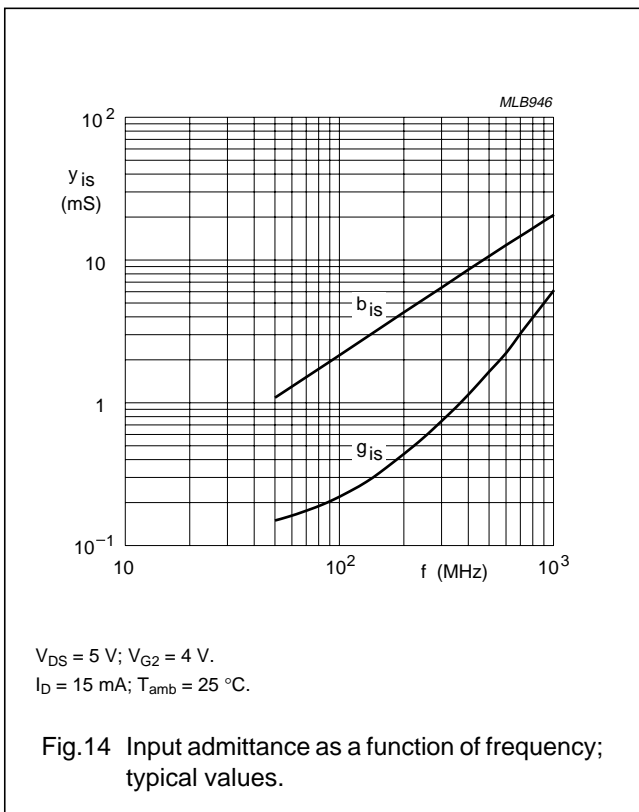
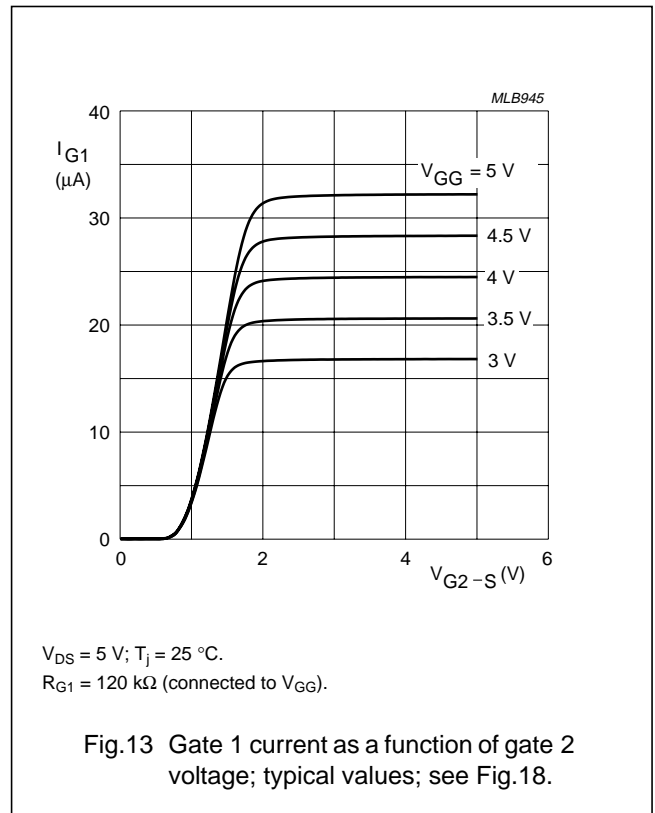
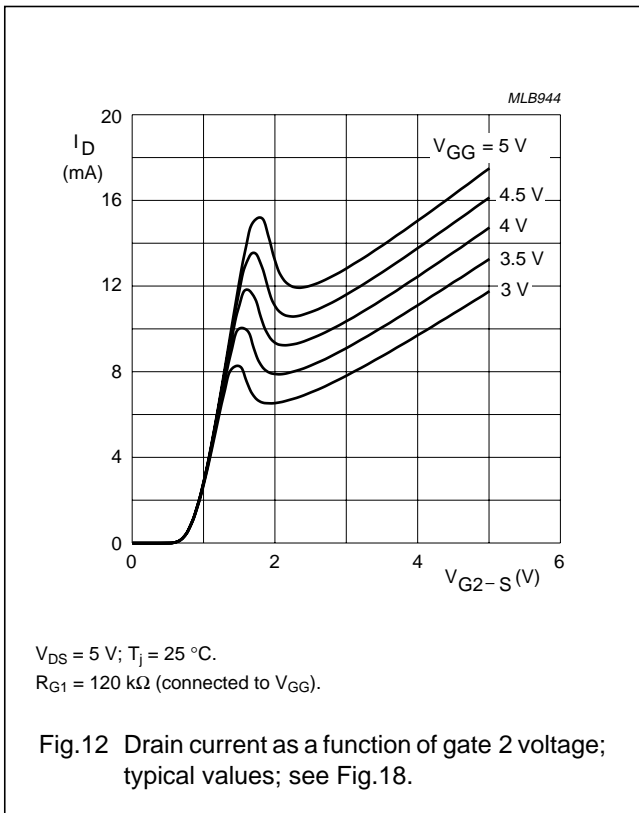
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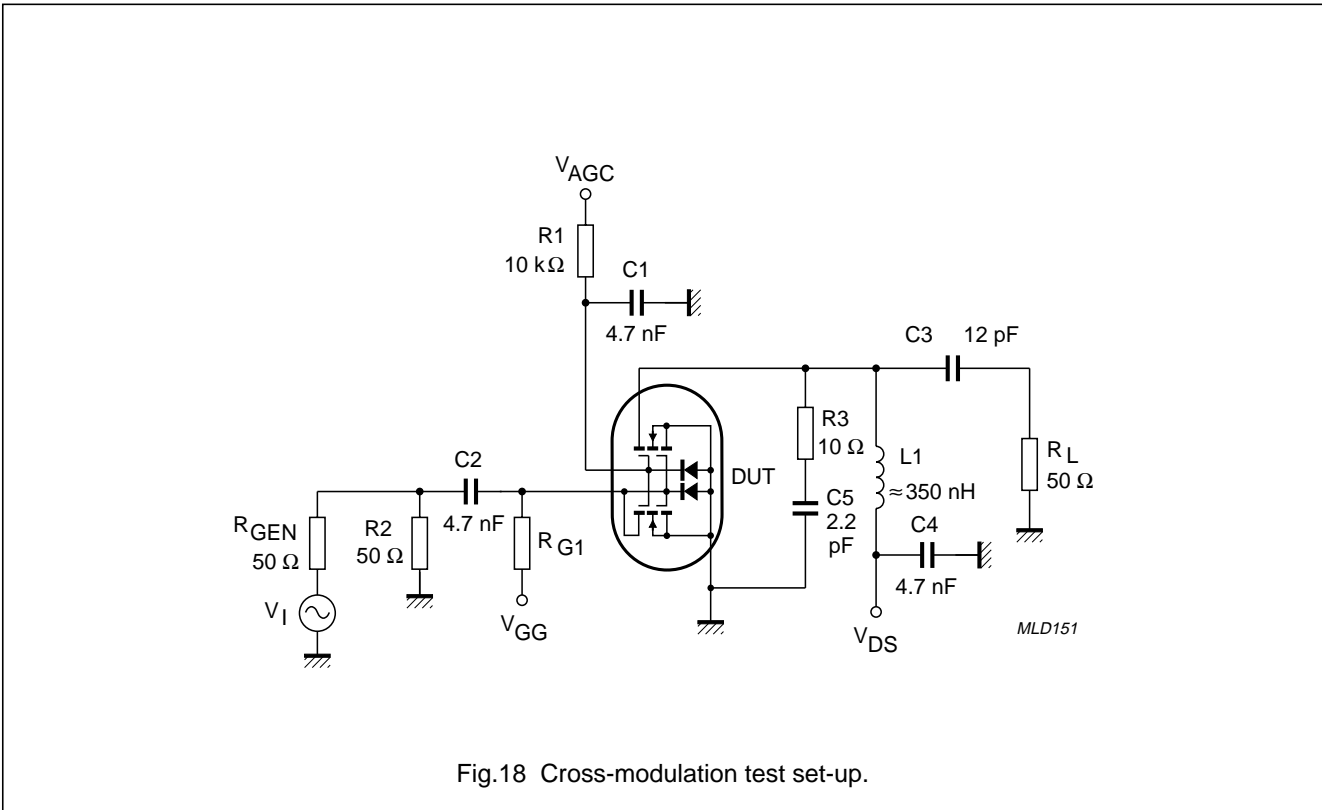
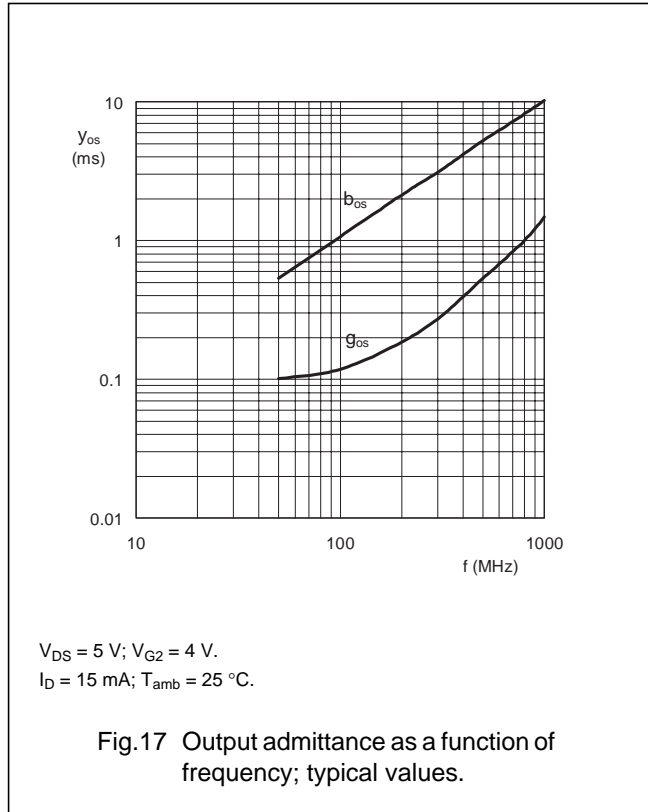
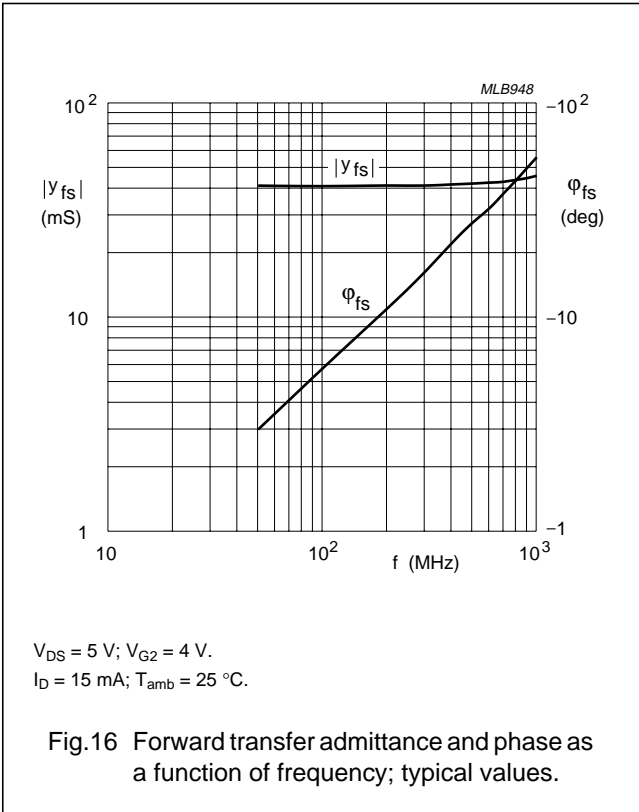
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Dual-gate MOS-FETs

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Table 1 Scattering parameters: $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 15\text{ mA}$

f (MHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.988	-5.9	4.258	172.8	0.001	89.1	0.990	-3.2
100	0.982	-11.9	4.219	165.4	0.002	81.9	0.998	-6.4
200	0.964	-23.4	4.090	151.7	0.004	73.9	0.979	-12.6
300	0.939	-34.3	3.899	138.4	0.005	66.8	0.969	-18.6
400	0.911	-44.7	3.708	125.9	0.005	61.7	0.956	-24.4
500	0.883	-54.2	3.467	114.2	0.005	60.5	0.944	-29.9
600	0.853	-62.9	3.246	103.3	0.005	63.3	0.934	-35.1
700	0.828	-70.9	3.036	92.7	0.004	72.4	0.924	-40.1
800	0.805	-78.3	2.843	82.5	0.004	97.9	0.916	-45.1
900	0.777	-85.4	2.634	72.6	0.005	121.3	0.906	-50.0
1000	0.749	-91.8	2.450	63.2	0.006	138.7	0.890	-54.9

Table 2 Noise data: $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 15\text{ mA}$

f (MHz)	F _{min} (dB)	Γ _{opt}		r _n
		(ratio)	(deg)	
800	2.00	0.603	67.71	0.581

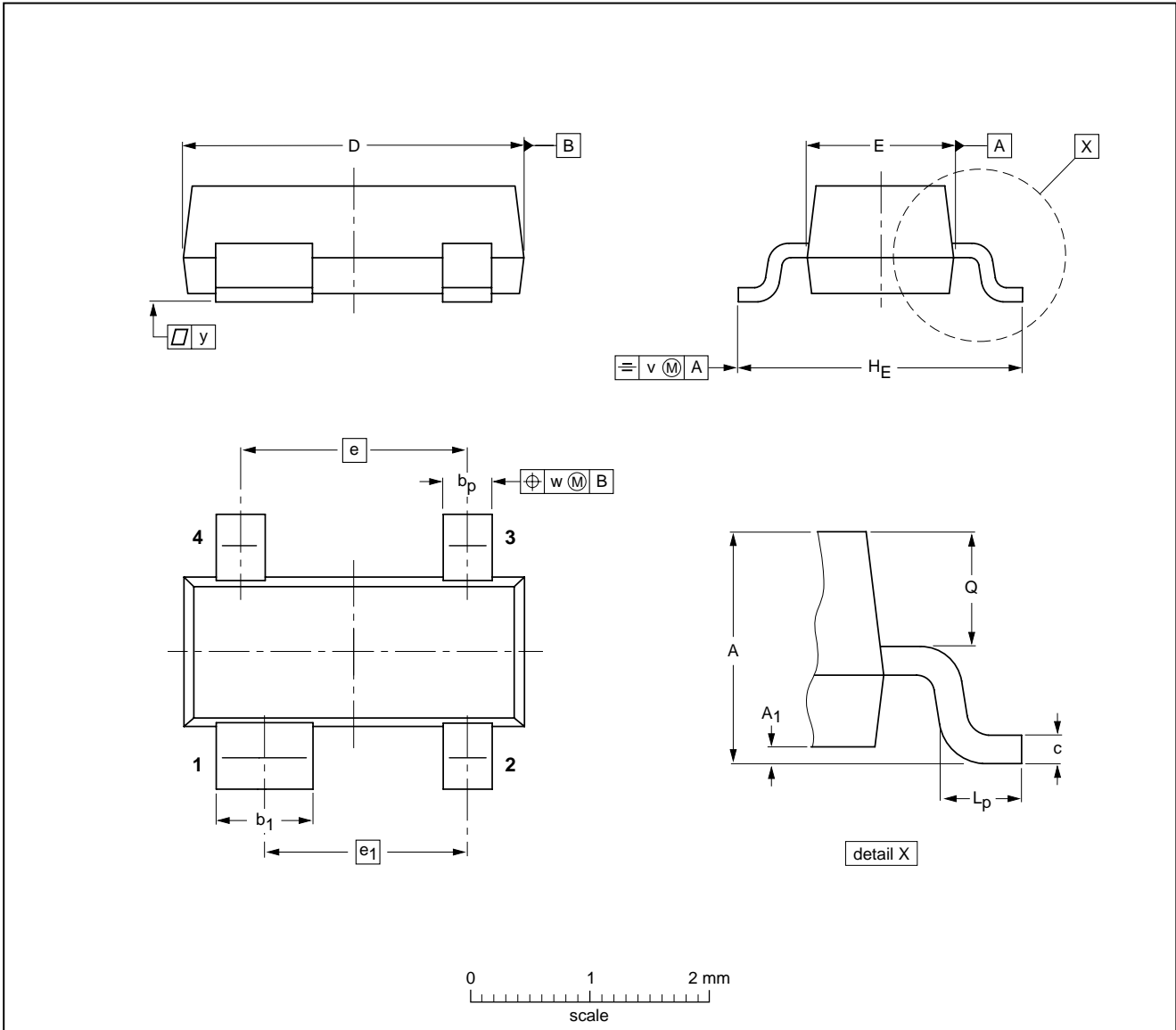
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PACKAGE OUTLINES

Plastic surface mounted package; 4 leads

SOT143B



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	b ₁	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT143B						97-02-28

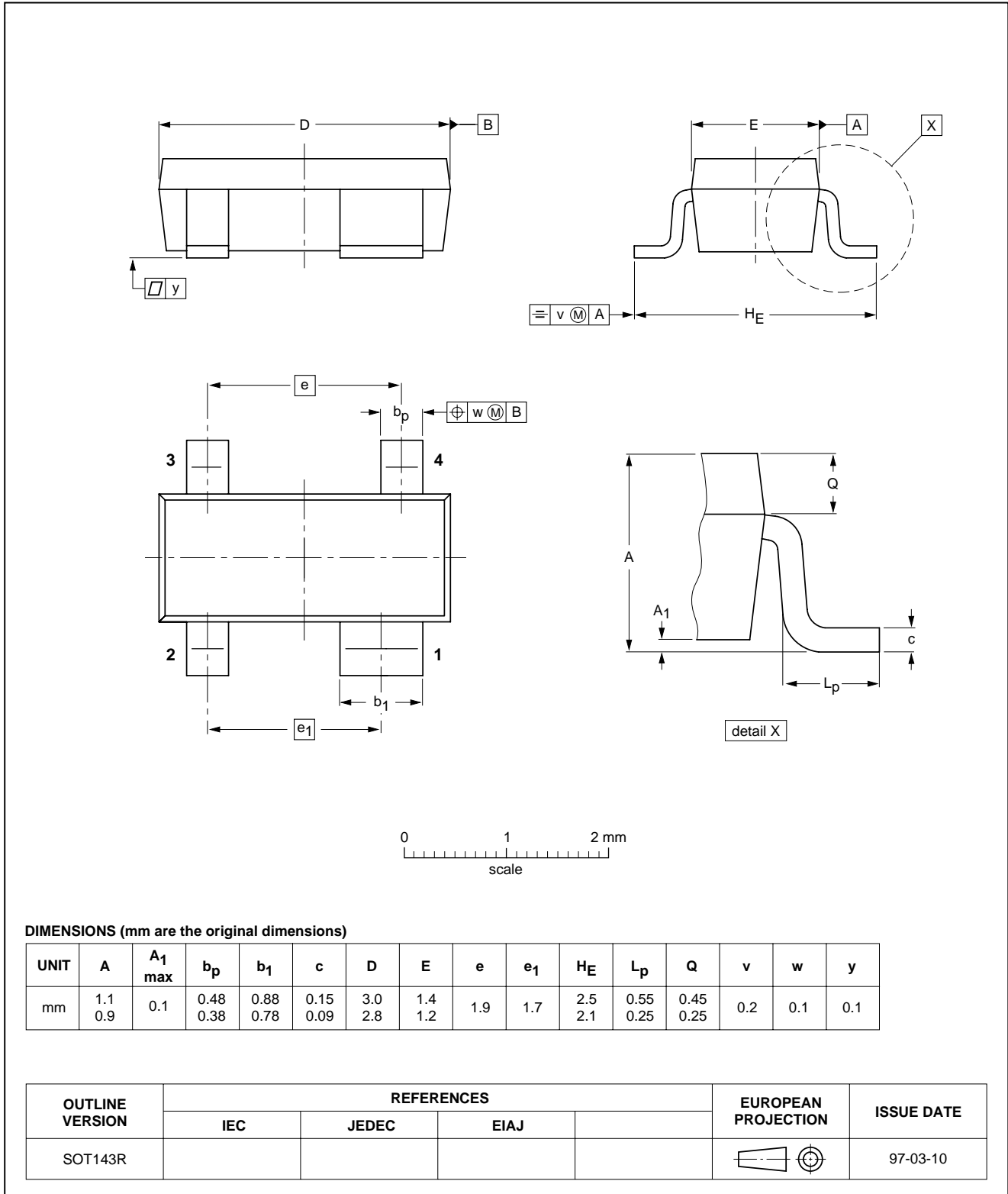
Dual-gate MOS-FETs

BF909A; BF909AR

PACKAGE OUTLINES

Plastic surface mounted package; reverse pinning; 4 leads

SOT143R



Dual-gate MOS-FETs

BF909A; BF909AR

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

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