HM62G36128 Series

4M Synchronous Fast Static RAM
(128k-words x 36-bits)

HITACHI

ADE-203-1008(Z)
Preliminary, Rev. 0.0
Feb. 5, 1999

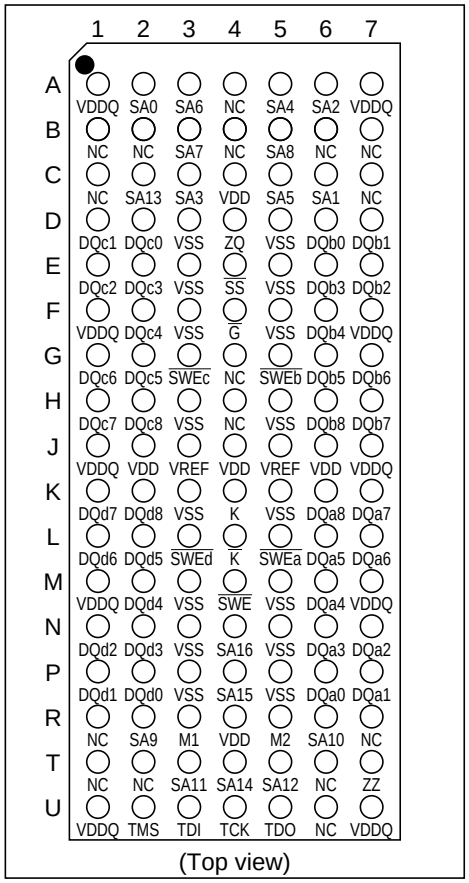
Features

- 3.3V+10%, –5% Operation
- 4M bit density
- 200MHz - 250MHz frequency
- Synchronous Operation
- Internal self-timed Late Write
- Byte Write Control
  (4 byte write selects, one for each 9 bits)
- Optional x 18 configuration
- HSTL compatible I/O
- Programmable impedance output drivers
- User selective input trip - point
- Differential , HSTL Clock Inputs
- Asynchronous $\overline{G}$ Output Control
- Asynchronous sleep mode
- BGA 119pin Package
- Limited set of boundary scan JTAG IEEE 1149.1 compatible
- Protocol : Single Clock Register-Register Mode

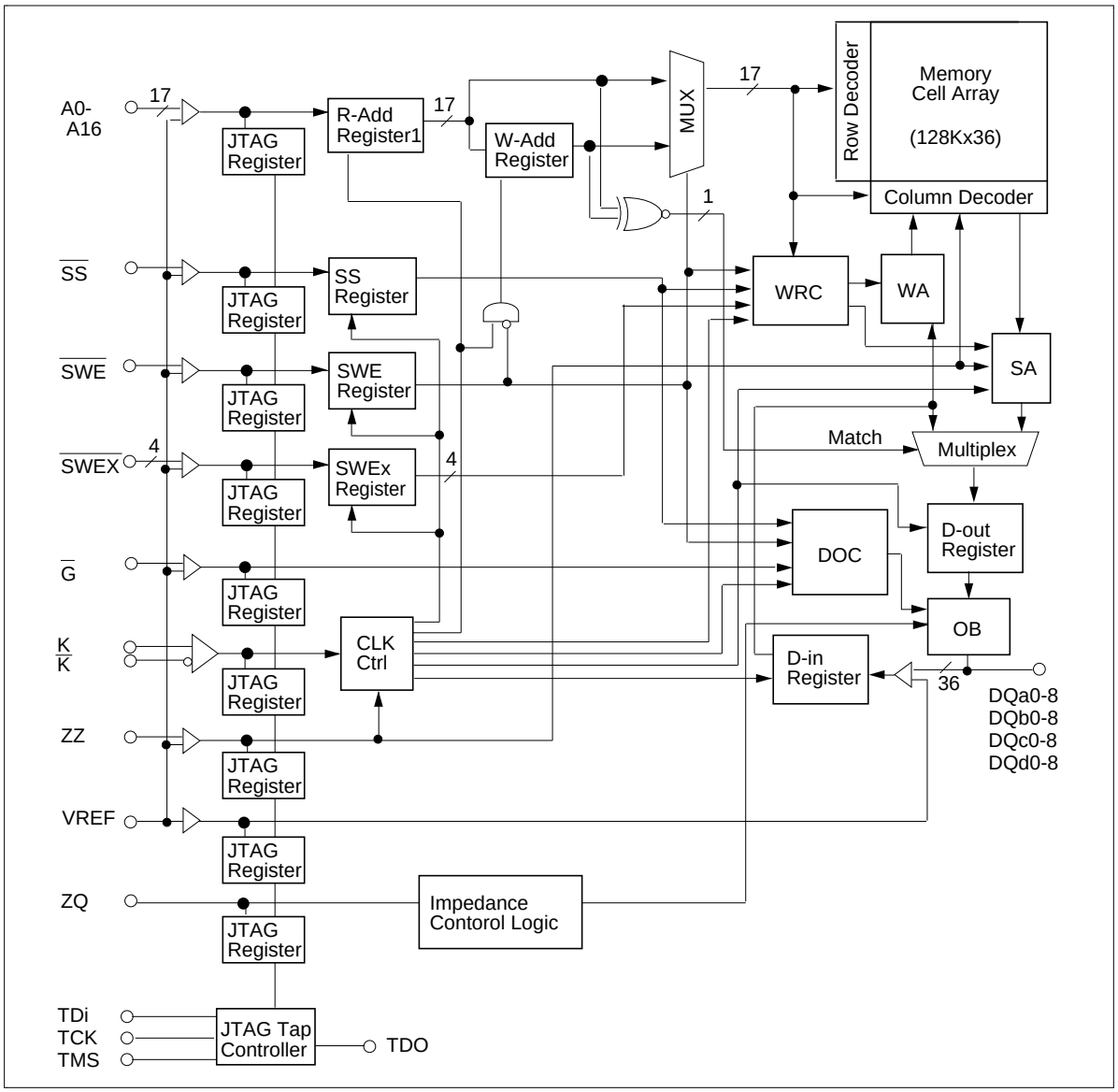
Ordering Information

Type Number	Access Time	Cycle Time	Package
HM62G36128BP-5	2.5ns	5.0ns	119 Bump 1. 27 mm
HM62G36128BP-4	2.2 ns	4.0 ns	14 mm × 22 mm BGA (BP-119A)

Pin Arrangement



Block Diagram



Pin Descriptions

Name	I/O Type	Descriptions	Note
V_{DD}	Supply	Core Power Supply	
V_{SS}	Supply	Ground	
V_{DDQ}	Supply	Output Power Supply	
V_{REF}	Supply	Input Reference : provides input reference voltage	
K	Input	Clock Input. Active high.	
$\overline{K}$	Input	Clock Input. Active low.	
$\overline{SS}$	Input	Synchronous Chip Select	
$\overline{SWE}$	Input	Synchronous Write Enable	
SAn	Input	Synchronous Address Input	n=0,1,2...16
$\overline{SWEx}$	Input	Synchronous Byte Write Enables	x = a, b, c, d
$\overline{G}$	Input	Asynchronous Output Enable	
ZZ	Input	Power Down Mode Select	
ZQ	Input	Output impedance control	1
DQxn	I/O	Synchronous Data Input / Output	x = a, b, c, d, n=0,1,2...8
M1, M2	Input	Output Protocol Mode Select	
TMS	Input	Boundary Scan Test Mode Select	
TCK	Input	Boundary Scan Test Clock	
TDI	Input	Boundary Scan Test Data Input	
TDO	Output	Boundary Scan Test Data Output	
NC	—	No Connection	

M1	M2	Protocol	
V_{SS}	V_{DD}	Synchronous register to register operation	2

Notes: 1. ZQ is to be connected to Vss via a resistance RQ where 150Ω ≤ RQ ≤350 Ω, if ZQ=V_{DDQ} or open, output buffer impedance will be maximum. A case of minimum impedance, it needs to connect over 120Ω between ZQ and Vss.

2. There is 1 protocol with mode pin. Mode control pins(M1 , M2) are to be tied either VDD or Vss. The state of the Mode control inputs must be set before power-up and must not change during device operation. Mode control inputs are not standard inputs and may not meet VIH or VIL specification.

Truth Table

ZZ	$\overline{SS}$	$\overline{G}$	$\overline{SWE}$	$\overline{SWEa}$	$\overline{SWEb}$	$\overline{SWEc}$	$\overline{SWEd}$	K	$\overline{K}$	Operation	DQ(n)	DQ(n+1)
H	X	X	X	X	X	X	X	X	X	sleep mode	High-Z	High-Z
L	H	X	X	X	X	X	X	L-H	H-L	Dead (not selected)	X	High-Z
L	X	H	X	X	X	X	X	X	X	Dead (Dummy read)	High-Z	High-Z
L	L	L	H	X	X	X	X	L-H	H-L	Read	X	Dout(a,b,c,d)0-8
L	L	X	L	L	L	L	L	L-H	H-L	Write a, b, c, d byte	High-Z	Din(a,b,c,d)0-8
L	L	X	L	H	L	L	L	L-H	H-L	Write b, c, d byte	High-Z	Din(b,c,d)0-8
L	L	X	L	L	H	L	L	L-H	H-L	Write a, c, d byte	High-Z	Din(a,c,d)0-8
L	L	X	L	L	L	H	L	L-H	H-L	Write a, b, d byte	High-Z	Din(a,b,d)0-8
L	L	X	L	L	L	L	H	L-H	H-L	Write a, b, c byte	High-Z	Din(a,b,c)0-8
L	L	X	L	H	H	L	L	L-H	H-L	Write c, d byte	High-Z	Din(c,d)0-8
L	L	X	L	L	H	H	L	L-H	H-L	Write a, d byte	High-Z	Din(a,d)0-8
L	L	X	L	L	L	H	H	L-H	H-L	Write a, b byte	High-Z	Din(a,b)0-8
L	L	X	L	H	L	L	H	L-H	H-L	Write b,c byte	High-Z	Din(b,c)0-8
L	L	X	L	H	H	H	L	L-H	H-L	Write d byte	High-Z	Din(d)0-8
L	L	X	L	H	H	L	H	L-H	H-L	Write c byte	High-Z	Din(c)0-8
L	L	X	L	H	L	H	H	L-H	H-L	Write b byte	High-Z	Din(b)0-8
L	L	X	L	L	H	H	H	L-H	H-L	Write a byte	High-Z	Din(a)0-8

Notes: 1. X means don't care for synchronous inputs, and H or L for asynchronous inputs.

2. $\overline{SWE}$, $\overline{SS}$, $\overline{SWEa}$ to $\overline{SWEd}$, SA are sampled at the rising edge of K clock.

3. Although differential clock operation is implied, this SRAM will operate properly with one clock phase (either K or $\overline{K}$)tied to Vref. Under such single-ended clock operation, all parameters specification within this document will be met.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Input Voltage on any pin	V_{IN}	-0.5 to V_{DDQ}+0.5	V	1, 4
Core Supply voltage	V_{DD}	-0.5 to 3.9	V	1
Output Supply Voltage	V_{DDQ}	-0.5 to 2.2	V	1, 4
Operating Temperature	T_{OPR}	0 to 70	°C	
Storage Temperature	T_{STG}	-55 to 125	°C	
Output Short–Circuit Current	I_{OUT}	25	mA	
Latch up Current	I_{LI}	200	mA	
Package junction to case thermal resistance	θJC	2	°C/W	5,7
Package junction to ball thermal resistance	θJB	5	°C/W	6,7

Notes: 1. All voltage are referenced to V_{SS}.

2. Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted the Operation Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
3. These CMOS memory circuits have been designed to meet the DC and AC specifications shown in the tables after thermal equilibrium has been established.
4. The following supply voltage application sequence is recommended: V_{SS}, V_{DD}, V_{DDQ}, V_{ref} then Vin. Remember, according to the Absolute Maximum Ratings table, V_{DDQ} is not to exceed 3.9V, whatever the instantaneous value of V_{DDQ}.
5. θJC is measured at the center of mold surface in fluorocarbon.(See Fig1.)
6. θJB is measured on the center ball pad after removing the ball in fluorocarbon. (See Fig1.)
7. These thermal resistance value have error of +/- 5°C/W.

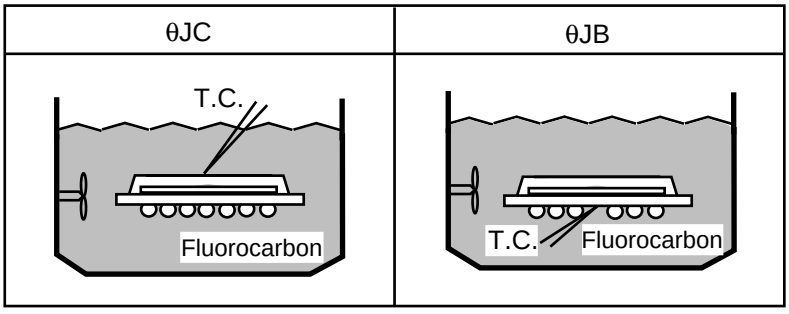


Fig.1 Definition of measurement

Recommended DC Operating Conditions (Ta = 0 to 70°C [Tj max = 110°C])

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Power Supply voltage -- Core	V_{DD}	3.135	3.30	3.63	V	
Power Supply voltage -- I/O	V_{DDQ}	1.4	1.5	1.6	V	
Input Reference Voltage -- I/O	V_{REF}	0.65	0.75	0.90	V	1
Input High Voltage	V_{IH}	V_{REF} +0.1	—	V_{DDQ}+0.3	V	
Input Low Voltage	V_{IL}	–0.5	—	V_{REF}–0.1	V	
Clock Differential Voltage	V_{DIF}	0.1	—	V_{DDQ}+0.3	V	2, 3
Clock Common Mode Voltage	V_{CM}	0.55	—	0.90	V	3
Clock input Differential Voltage	V_{DIF}	0.2	—	V_{DDQ}+0.3	V	3

Notes : 1. Peak to Peak AC component superimposed on V_{ref} may not exceed 5% of V_{ref}.

2. Minimum differential input voltage required for differential input clock operation.

3. See Figure 1.

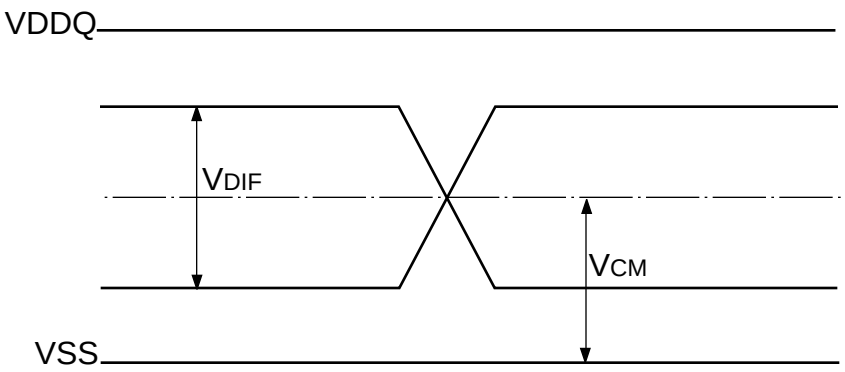


Figure 1. Diffrential Voltage / Common Mode Voltage

DC Characteristics (Ta = 0 to 70°C, [Tjmax=110˚C], V_{DD} = 3.3V+10%, –5%)

Parameter		Symbol	Min	Max	Unit	Note
Input Leakage Current		I_{LI}	—	2	µA	1
Output Leakage Current		I_{LO}	—	5	µA	2
Standby Current		I_{SBZZ}	—	100	mA	3
VDD Operating Current, excluding output drivers.	4ns cycle	I_{DD4}	—	580	mA	4
	5ns cycle	I_{DD5}	—	500	mA	4
Quiescent Active Power Supply Current.		I_{DD2}	—	180	mA	5

Parameter	Symbol	Min	Typ	Max	Unit	Note
Output Low Voltage	V_{OL}	V_{SS}	—	V_{SS}+0.4	V	6
Output High Voltage	V_{OH}	V_{DDQ}–0.4	—	V_{DDQ}	V	6
ZQ pin Connect Resistance	RQ	150	250	350	Ω	
Output “Low” Current	I_{OL}	(V_{DDQ}/2)/[(RQ/5)–15%]		(V_{DDQ}/2)/[(RQ/5)+15%]	mA	7,9
Output “High” Current	I_{OH}	(V_{DDQ}/2)/[(RQ/5)+15%]		(V_{DDQ}/2)/[(RQ/5)–15%]	mA	8,9

Note:
1. $0 \le Vin \le V_{DDQ}$ for all input pins(except V_{REF} ,ZQ,M1,M2 pin)
2. $0 \le VOUT \le V_{DDQ}$, DQ in High–Z
3. All inputs (except clock) are held at either VIH or VIL,ZZ is held at VIH,Iout=0 mA
4. Iout = 0 mA, read 50% / write 50%, $V_{DD} = V_{DD}$ max , Frequency =min.cycle
5. Iout = 0 mA, read 50% / write 50%, $V_{DD} = V_{DD}$ max , Frequency = 3 Mhz
6. Minimum impedance push pull output buffer mode, I_{OH}=–6mA, I_{OL}=6mA
7. Measured at V_{OL}=1/2 V_{DDQ}
8. Measured at V_{OH}=1/2 V_{DDQ}
9. Output buffer impedance can be programmed by terminating the ZQ pin to VSS through a precision resister(RQ). The value of RQ is five times the output impedance desired. The allowable range of RQ to guarantee impedance matching with a tolerance of 15% is between 150Ω and 350Ω . If the status of ZQ pin is open ,output impedance is maximum. Maximum impedance occurs with ZQ connected to V_{DDQ}. The impedance update of the output driver occurs when the SRAM is in High-Z. Write and Deselect operations will synchronously switch the SRAM into and out of High-Z, therefore triggering an update. The user may choose to invoke asynchronous $\overline{G}$ updates by providing a $\overline{G}$ setup and hold about the K clock to guarantee the proper update. At power up, the output impedance default to minimum impedance. It will take 1024 cycles for the impedance to be completely updated if the programmed impedance is much higher than minimum impedance.

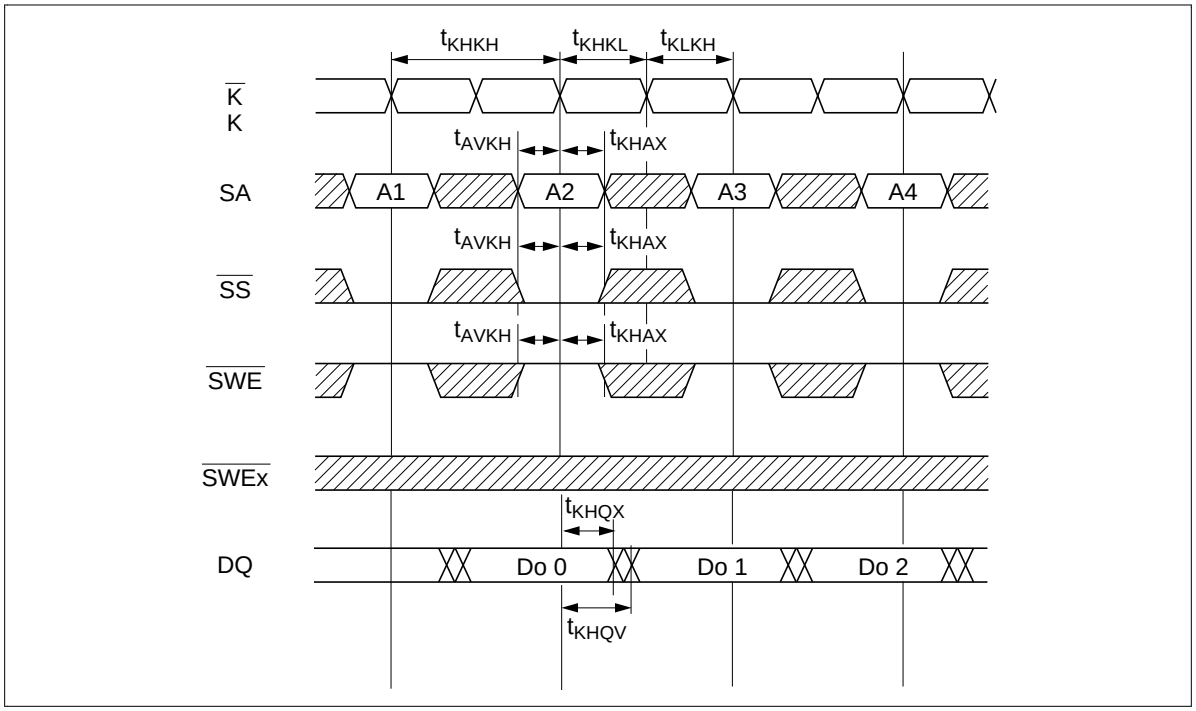
AC Characteristics ($0^{\circ}C \leq Ta \leq 70^{\circ}C$ [Tj max = 110°C], V_{DD}= 3.3V+10%, –5%)

Single Differential Clock Register-Register Mode (M1 = V_{SS}, M2 = V_{DD})

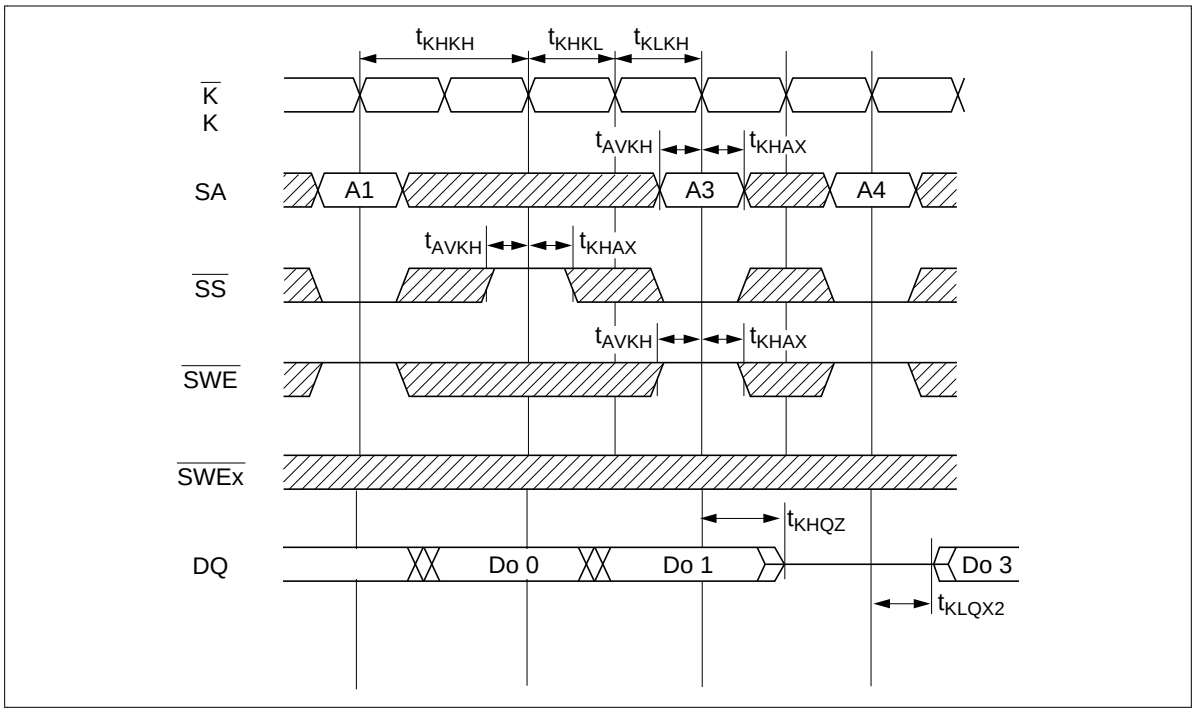
		– 4		– 5			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
CK Clock Cycle time	t_{KHKH}	4.0	—	5.0	—	ns	
CK Clock High Width	t_{KHKL}	1.5	—	1.5	—	ns	
CK Clock Low Width	t_{KLKH}	1.5	—	1.5	—	ns	
Address Setup Time	t_{AVKH}	0.5	—	0.5	—	ns	
Data Setup Time	t_{DVKH}	0.5	—	0.5	—	ns	
Address Hold Time	t_{KHAX}	—	0.75 [1)]	—	1.0	ns	
Data Hold Time	t_{KHDX}	—	0.75 [1)]	—	1.0	ns	
Clock High to output valid	t_{KHQV}	—	2.2	—	2.5	ns	2
Clock High to output hold	t_{KHQX}	0.5	—	0.5	—	ns	2
Clock High to output valid(/SS ctrl.)	t_{KHQX2}	—	2.2	—	2.5	ns	2,5
Clock High to output High-Z	t_{KHQZ}	—	2.5	—	3.0	ns	2,3
Output Enable low to output Low-Z	t_{GLQX}	0.5	—	0.5	—	ns	2,5
Output Enable low to output valid	t_{GLQV}	—	2.5	—	2.5	ns	2,3
Output Enable low to output High-Z	t_{GHQZ}	—	2.5	—	2.5	ns	2,3
Sleep mode recovery time	t_{ZZR}	10.0	—	10.0	—	ns	
Sleep mode enable time	t_{ZZE}	—	10.0	—	10.0	ns	2,3

Notes: 1. Guaranteed by design.
2. See AC Test Loading figure.
3. Transitions are measured at start point of output high impedance from output low impedance.
4. Output Driver Impedance update specifications for $\overline{G}$ induced updates. Write and Deselected cycles will also induce Output Driver updates during High-Z.
5. Transitions are measured ±50mV from steady state voltage.

Read Cycle 1

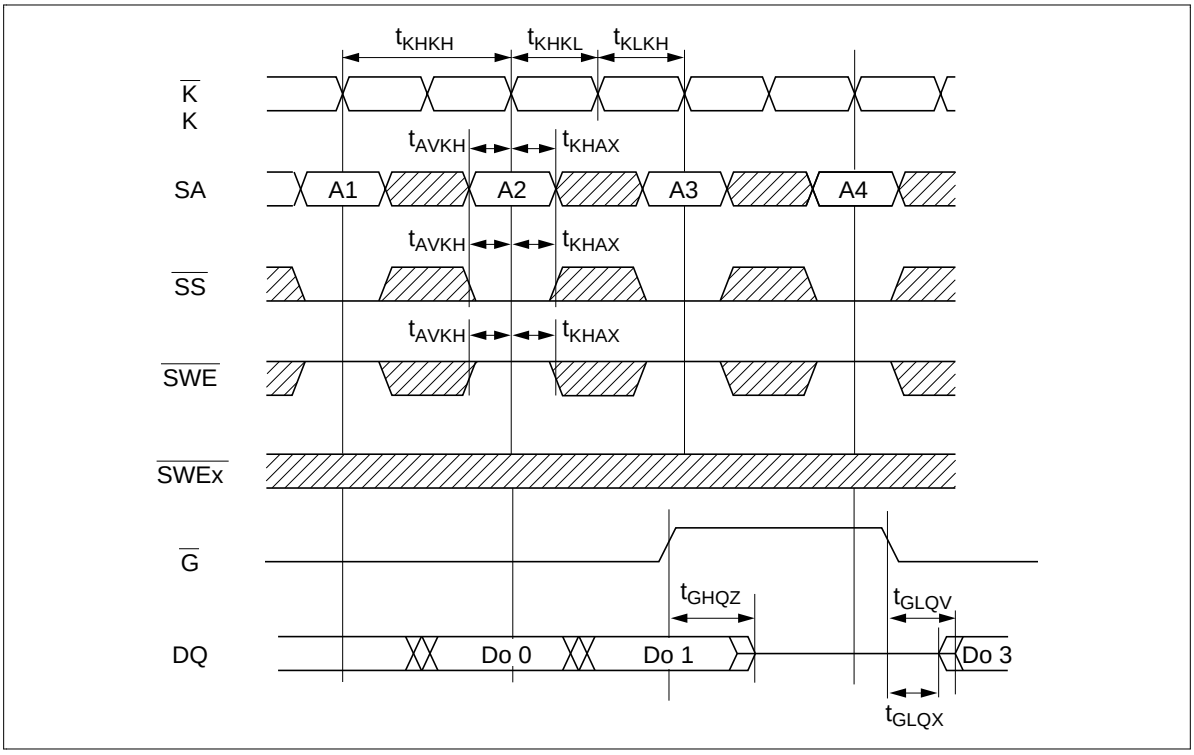


Read Cycle 2 ($\overline{SS}$ Controlled)

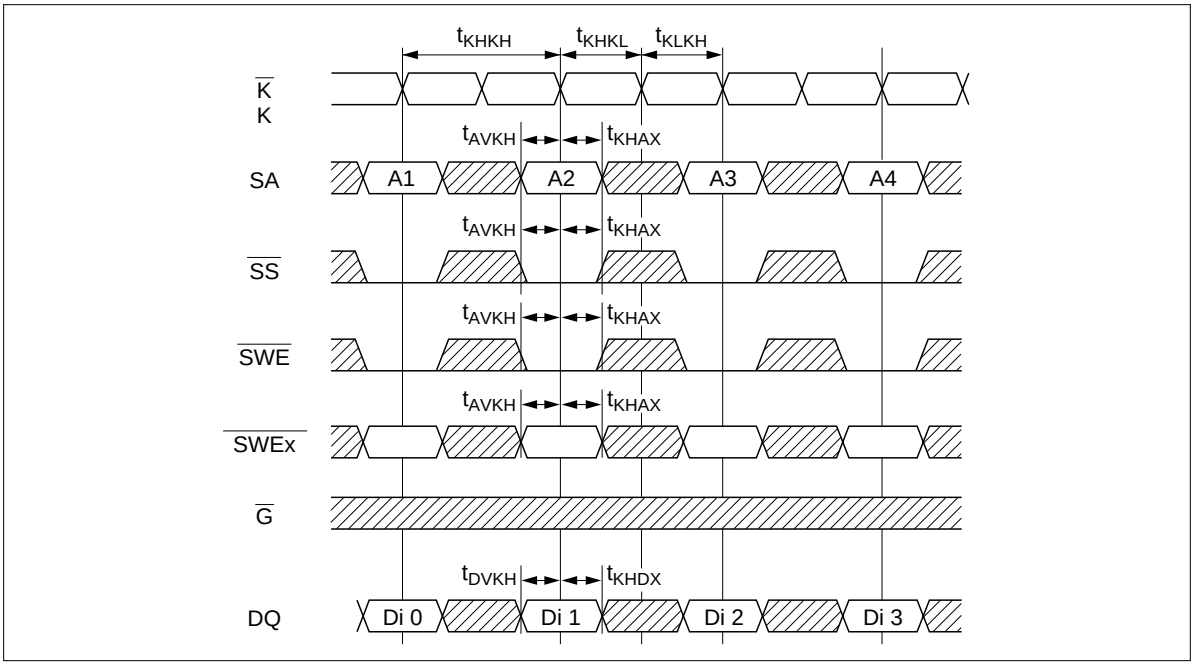


Notes:$\overline{G}$,ZZ=VIL,x=a,b,c,d

Read Cycle 3 ($\overline{G}$ Controlled)

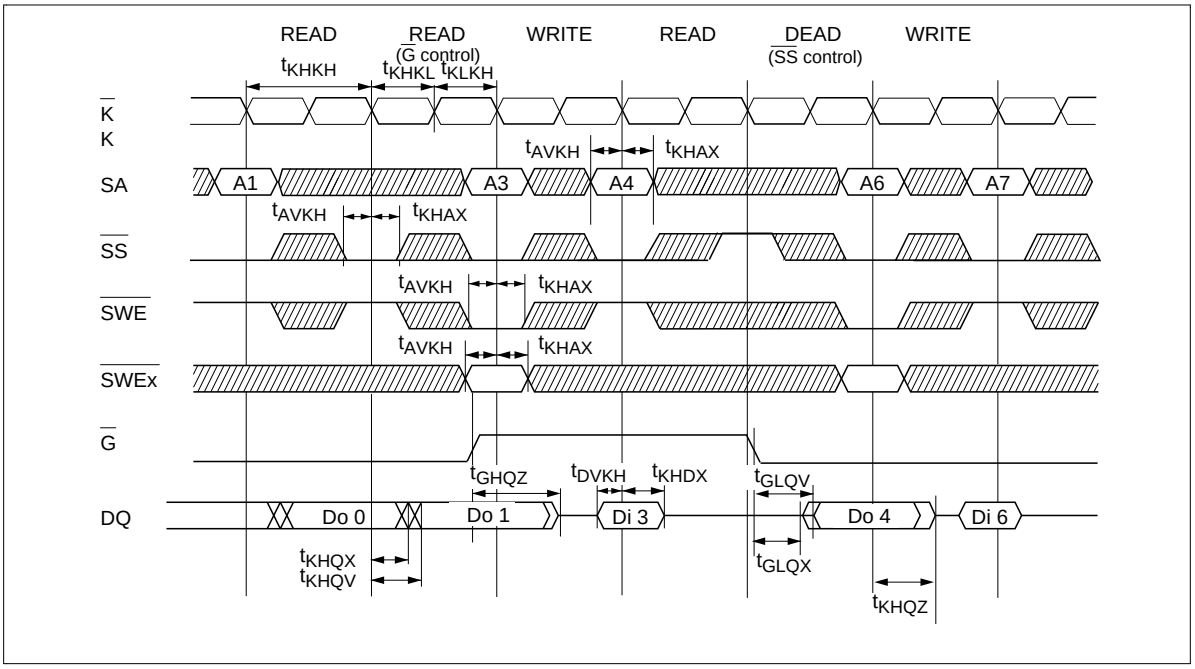


Write Cycle

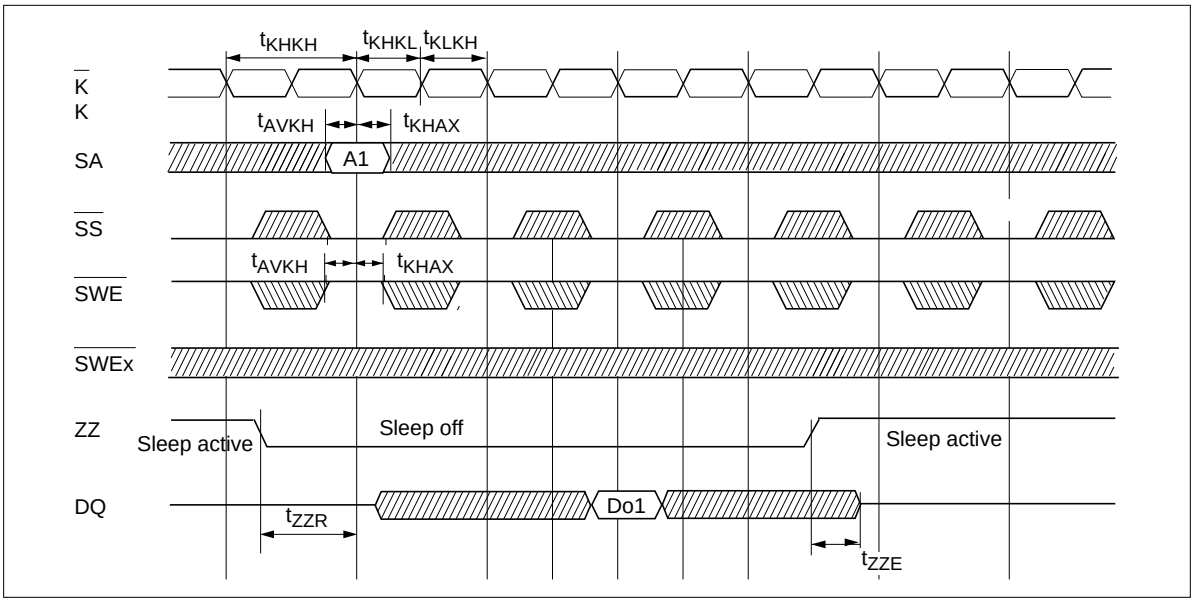


Notes:ZZ=VIL,x=a,b,c,d

Read-Write Cycle



ZZ Control



Notes: ZZ=VIL,x=a,b,c,d

Input Capacitance (Ta = 25°C, f = 1 MHz)

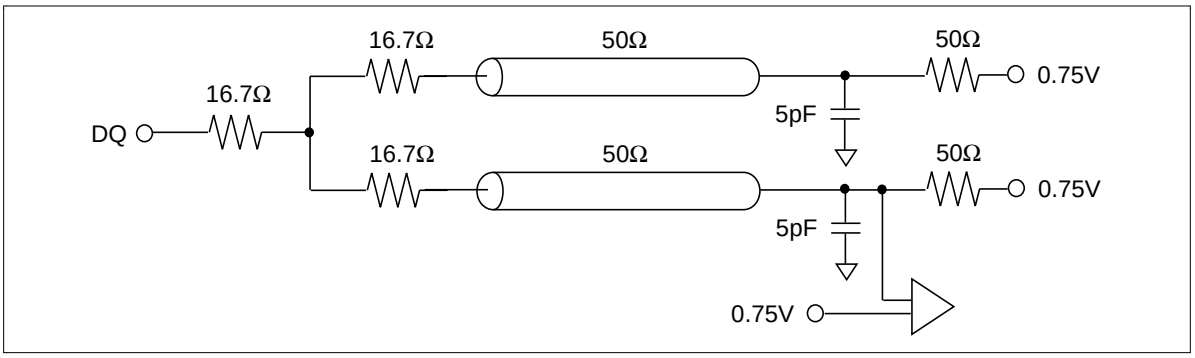
Parameter	Symbol	Min	Max	Unit	Pin Name
Input Capacitance	C_{IN}	—	4	pF	SAn, SS, SWE, SWEx
Clock Input Capacitance	C_{CLK}	—	7	pF	K, K, G
I/O Capacitance	C_{IO}	—	5	pF	DQxn

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

Parameter	Symbol	Conditions	Unit	Note
Input and output timing reference levels	V_{REF}	0.75	V	
Input signal amplitude	V_{IL}, V_{IH}	0.25 to 1.25	V	
Input rise / fall time	tr, tf	0.5 (10% to 90%)	ns	
Clock input timing reference level		Differential Cross Point		
V_{DIF} to Clock		0.75	V	
V_{CM} to Clock		0.75	V	
Output Loading conditions		See Figures		

Note : Measurement condition is the minimum impedance push pull output buffer mode, I_{OH}=-6mA,I_{OL}=6mA



Boundary Scan Test Access Port Operations

overview

In order to perform the interconnect testing of the modules that include this SRAM, the serial boundary scan test access port (TAP) is designed to operate in a manner consistent with IEEE Standard 1149.1 - 1990. But does not implement all of the functions required for 1149.1 compliance The HM62G series contains a TAP controller. Instruction register, Boundary scan register, Bypass register and ID register.

Test Access Port Pins

Symbol I/O	Name
TCK	Test Clock
TMS	Test Mode Select
TDI	Test Data In
TDO	Test Data Out

Notes: This Device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1.
To disable the TAP, TCK must be connected to Vss. TDO should be left unconnected.
To test Boundary scan, ZZ need to be kept below Vref –0.4V.

TAP DC Operating Characteristics (Ta = 0˚C to 70˚C [Tj max = 110°C])

Parameter	Symbol	Min	Max	Note
Boundary scan Input High voltage	V_{IH}	2.0 V	V_{DD} + 0.3 V	
Boundary scan Input Low voltage	V_{IL}	–0.5 V	0.8 V	
Boundary scan Input Leakage Current	I_{LI}	–2µA	+2µA	1
Boundary scan Output Low voltage	V_{OL}		0.4 V	2
Boundary scan Output High voltage	V_{OH}	2.4 V		3

Notes: 1. $0 \le Vin \le V_{DD}$ for all logic input pin
2. I_{OL} = –8 mA
3. I_{OH} = 8 mA

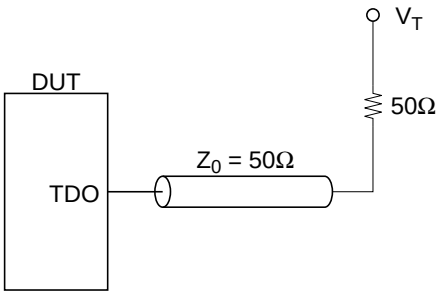
TAP AC Operating Characteristics (Ta = 0˚C to 70˚C [Tj max = 110 °C])

Parameter	Symbol	Min	Max	Unit	Note
Test Clock Cycle Time	t_{THTH}	67	—	ns	
Test Clock High Pulse Width	t_{THTL}	30	—	ns	
Test Clock Low Pulse Width	t_{TLTH}	30	—	ns	
Test Mode Select Setup	t_{MVTH}	10	—	ns	
Test Mode Select Hold	t_{THMX}	10	—	ns	
Capture Setup	t_{CS}	10	—	ns	1
Capture Hold	t_{CH}	10	—	ns	1
TDI Valid to TCK High	t_{DVTH}	10	—	ns	
TCK High to TDI Don't Care	t_{THDX}	10	—	ns	
TCK Low to TDO Unknown	t_{TLQX}	0	—	ns	
TCK Low to TDO Valid	t_{TLQV}	—	20	ns	

Note: 1. t_{CS} + t_{CH} defines the minimum pause in RAM I/O pad transitions to assure pad data capture.

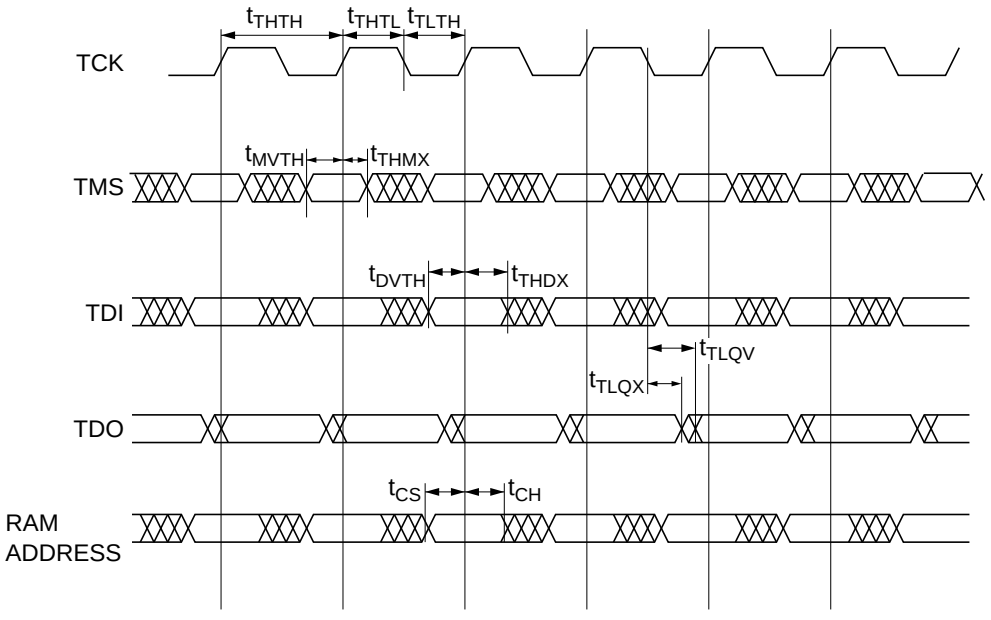
TAP AC Test Conditions

- Temperature — 0°C ≤ Ta ≤ 70°C [Tj max = 110°C]
- Input timing measurement reference Level — 1.5 V
- Input pulse levels — 0 to 3.0 V
- Input Rise/Fall Time — 2.0 ns typical (10% to 90%)
- Output timing measurement reference Level — 1.5 V
- Test load termination supply voltage (V_T) — 1.5 V
- Output Load — See figures



boundary scan AC test Load

TAP Controller Timing Diagram



TAP Controller Timing Diagram

Test Access Port Registers

Register Name	Length	Symbol	Note
Instruction Register	3 bits	IR [0;2]	
Bypass Register	1 bits	BP	
ID Register	32 bits	ID [0;31]	
Boundary Scan Register	70 bits	BS [1;70]	HM62G36128 series

TAP Controller Instruction Set

IR2	IR1	IR0	Instruction	Operation
0	0	0	SAMPLE-Z	Tristate all data drivers and capture the pad value
0	0	1	IDCODE	
0	1	0	SAMPLE-Z	Tristate all data drivers and capture the pad value
0	1	1	BYPASS	
1	0	0	SAMPLE	
1	0	1	BYPASS	
1	1	0	BYPASS	
1	1	1	BYPASS	

Note: This Device does not perform EXTEST, INTEST or the preload portion of the PRELOAD command in IEEE 1149.1.

Boundary Scan Order

Bit #	Bump ID	Signal Name	Bit #	Bump ID	Signal Name
1	5R	M2	36	3B	SA7
2	4P	SA15	37	2B	NC
3	4T	SA14	38	3A	SA6
4	6R	SA10	39	3C	SA3
5	5T	SA12	40	2C	SA13
6	7T	ZZ	41	2A	SA0
7	6P	DQa0	42	2D	DQc0
8	7P	DQa1	43	1D	DQc1
9	6N	DQa3	44	2E	DQc3
10	7N	DQa2	45	1E	DQc2
11	6M	DQa4	46	2F	DQc4
12	6L	DQa5	47	2G	DQc5
13	7L	DQa6	48	1G	DQc6
14	6K	DQa8	49	2H	DQc8
15	7K	DQa7	50	1H	DQc7
16	5L	SWEa	51	3G	SWEc
17	4L	K	52	4D	ZQ
18	4K	K	53	4E	SS
19	4F	G	54	4G	NC
20	5G	SWEb	55	4H	NC
21	7H	DQb7	56	4M	SWE
22	6H	DQb8	57	3L	SWEd
23	7G	DQb6	58	1K	DQd7
24	6G	DQb5	59	2K	DQd8
25	6F	DQb4	60	1L	DQd6
26	7E	DQb2	61	2L	DQd5
27	6E	DQb3	62	2M	DQd4
28	7D	DQb1	63	1N	DQd2
29	6D	DQb0	64	2N	DQd3
30	6A	SA2	65	1P	DQd1
31	6C	SA1	66	2P	DQd0
32	5C	SA5	67	3T	SA11
33	5A	SA4	68	2R	SA9
34	6B	NC	69	4N	SA16
35	5B	SA8	70	3R	M1

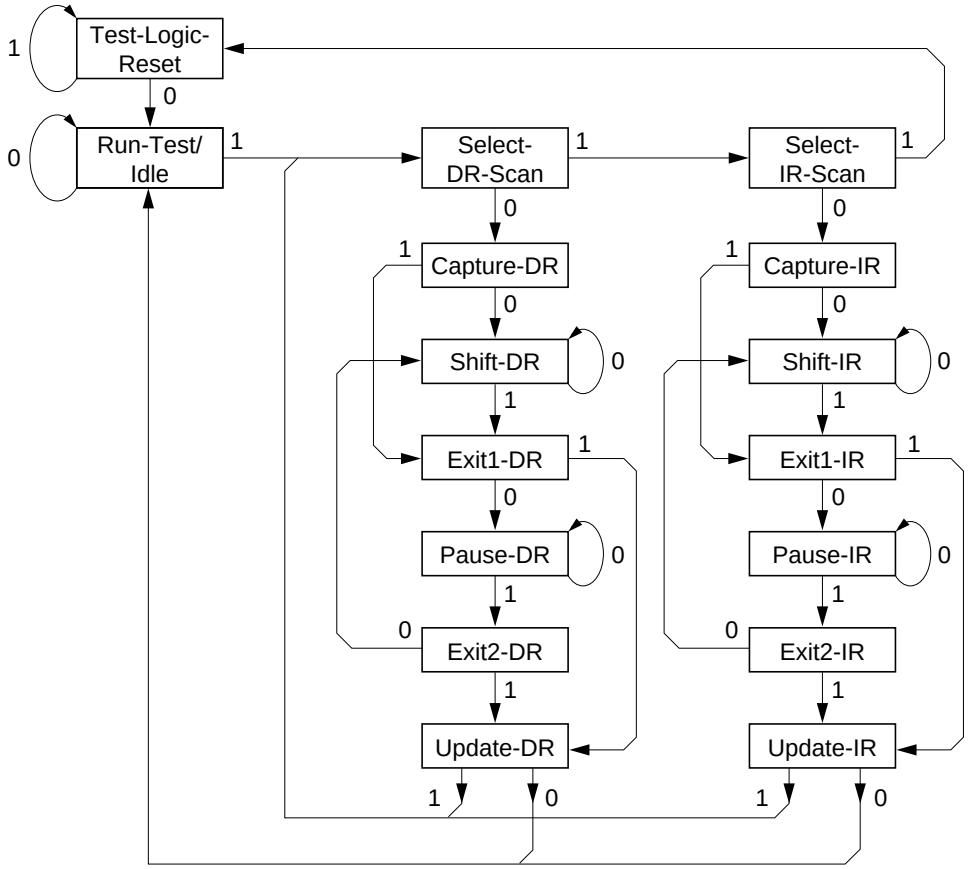
Notes: 1. Bit#1 is the first scan bit to exit the chip.

2. The NC pads listed in this table are indeed no connects, but are represented in the boundary scan register by a “Place Holder”. Place holder registers are internally connected to VSS.
3. In Boundary scan mode, differential input K and $\overline{K}$ are referenced to each other and must be at opposite logic levels for reliable operation.
4. ZZ must remain at V_{IL} during boundary scan.
5. In boundary scan mode, ZQ must be driven to VDDQ or VSS supply rail to ensure consistent results.
6. M1 and M2 must be driven to VDD or VSS supply rail to ensure consistent results.

ID register

Bit#	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	x	x	x	1	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
	Vendor Revision No.				Depth					Width					Use in the future						Vendor ID No.											Fix

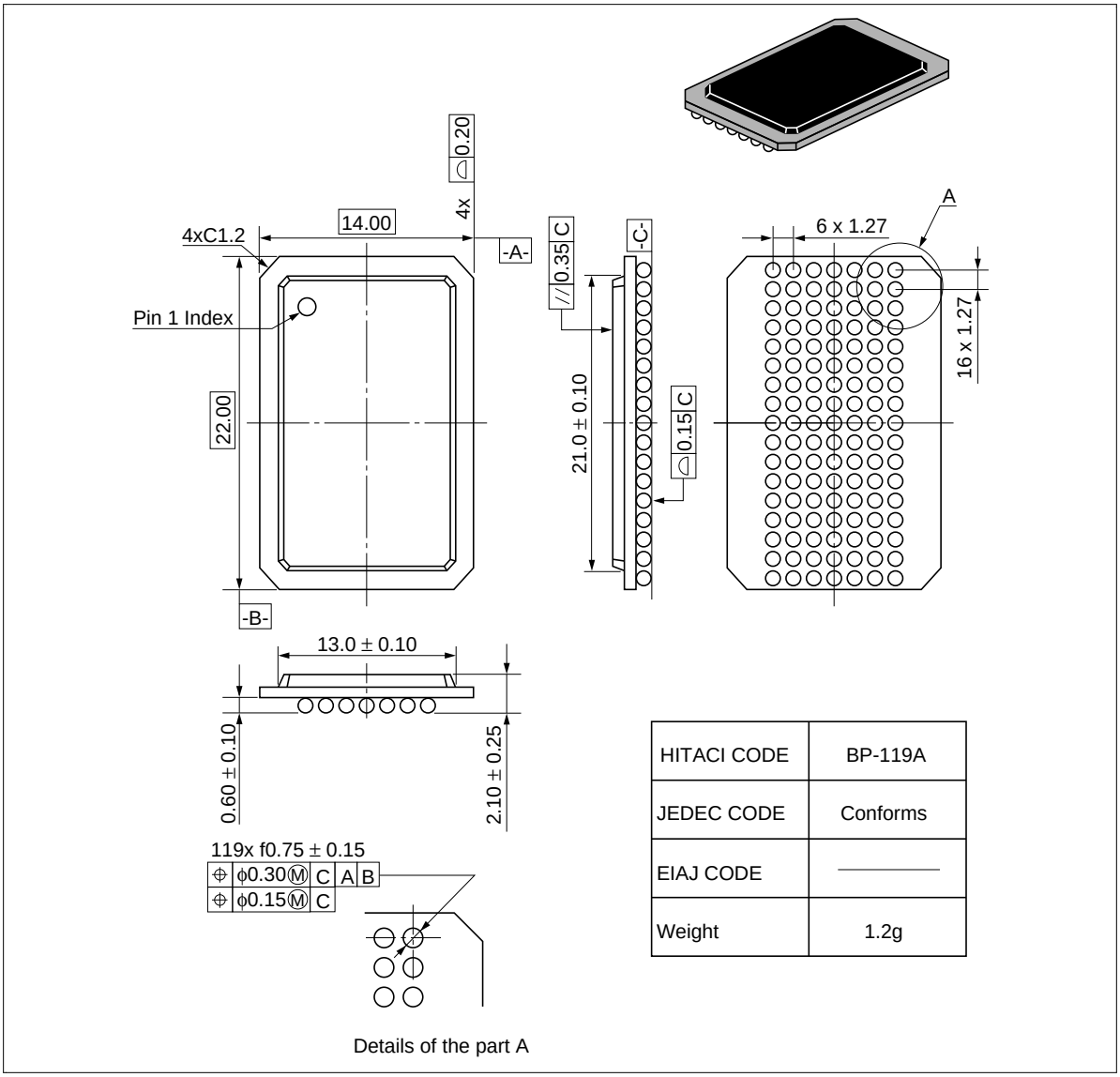
TAP Controller State Diagram



Note: The value adjacent to each state transition in this figure represents the signal present at TMS at the time of a rising edge at TCK.
No matter what the original state of the controller, it will enter Test-Logic-Reset when TMS is held high for at least five rising edges of TCK.

Package Outline

(BP-119A) (Unit : mm)



HITACI CODE	BP-119A
JEDEC CODE	Conforms
EIAJ CODE	————
Weight	1.2g

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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Feb. 05,1999	Initialrelease	M.Ikeda	S.Nakazato