Section 4

PRINCIPLES OF OPERATION

4.1 GENERAL

The principles of operation of Series 2000 DMM are presented in two main subdivisions. Initially, in paragraphs 4.1 through 4.6, the functional performance of each of the major subsystems is presented in brief. This is intended to provide an understanding of the general function of the unit: of how the different types of input signals are processed through to the display in the various modes of operation. The remainder of Section 4 contains detailed circuit explanations. Such material is useful for further study and understanding of the instrument operation and for detailed corrective maintenance, but may be omitted unitl needed without detracting from the effective use of the Series 2000 DMM.

4.2 SYSTEM BLOCK DIAGRAM

In its simplest form, the Model 2500 DMM is represented by the Block Diagram of Figure 4-1. The system consists of an input Signal Conditioning block, followed by the TRI-PHASIC™ Analog to Digital (A/D) Converter block, whose decoded outputs are driving signals for the Timing and Display block. The Timing & Control block and two Power Supply blocks complete the unit.

The major blocks in Figure 4-1 physically comprise the following:

Analog Block Diagram (Figure 4-2)

Digital Block Diagram (Figure 4-3).

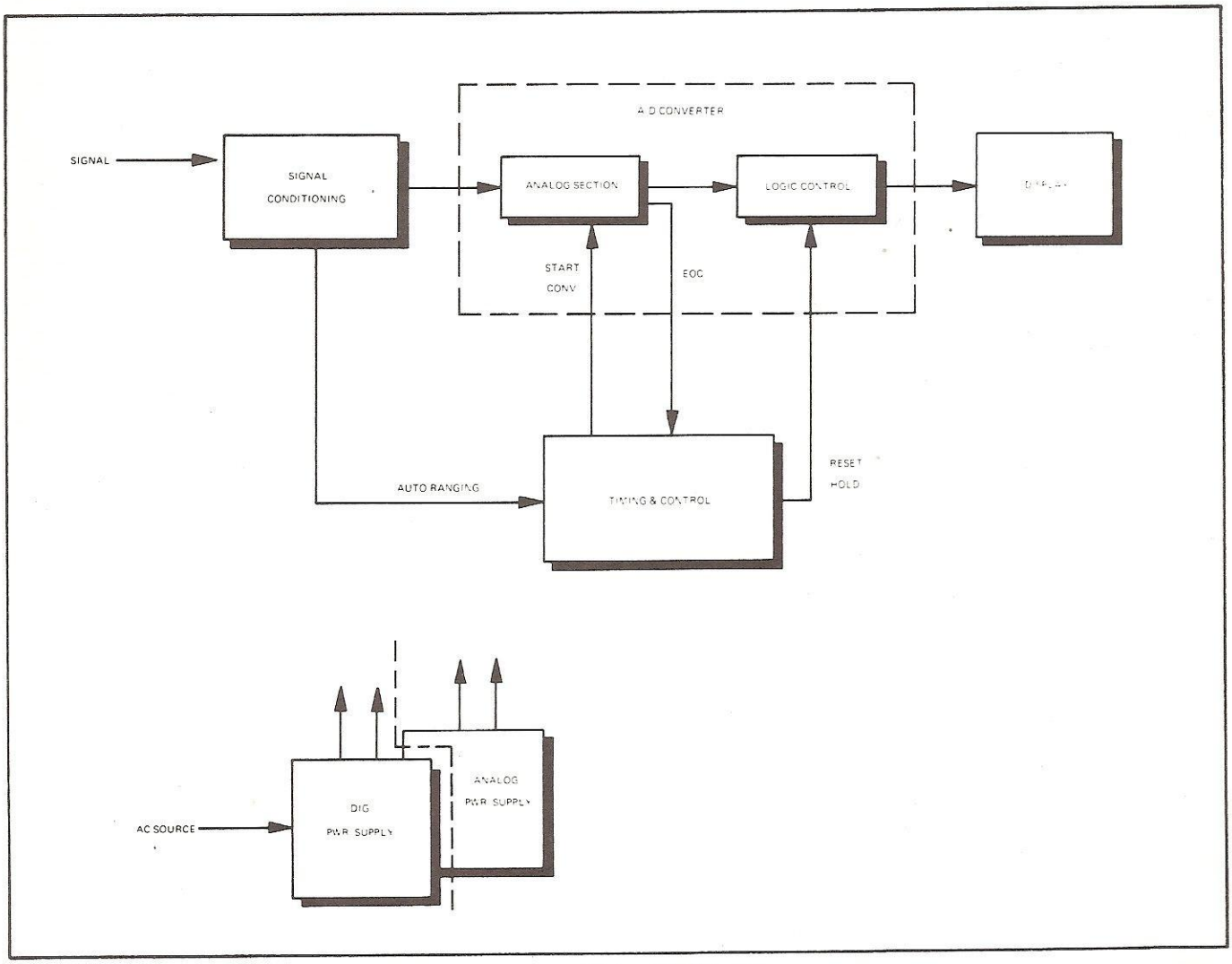


Figure 4-1. DMM Simplified Block Diagram

The analog portion of the TRI-PHASIC A/D converter accomplishes the conversion in the three phases of (1) self zeroing, (2) unknown integration, and (3) reference integration, the latter two compensated by the stored value of compensating offset.

In the Analog Block Diagram (Figure 4-2), one of the three signal conditioning blocks (for Resistance, DC Volts, and AC Volts measurements) is connected via a switching network as the input to the A/D preamplifier. The preamplifier output is integrated and then processed by the high gain amplifier. The high gain amplifier outputs: (1) drive the sign indicator at the end of phase 2 to obtain the switching control signals that select the appropriate polarity of the ISO-Polar™ reference voltage to be applied (via the switching network) to the A/D preamplifier in phase 3 and at the same time drive the Display to indicate sign, and (2) indicate end of phase 3. The high gain amplifier in phase 1 also drives the self zeroing circuitry to develop the offset signal to be applied during the phases 2 and 3 as an input to the A/D preamplifier. Logic and Control

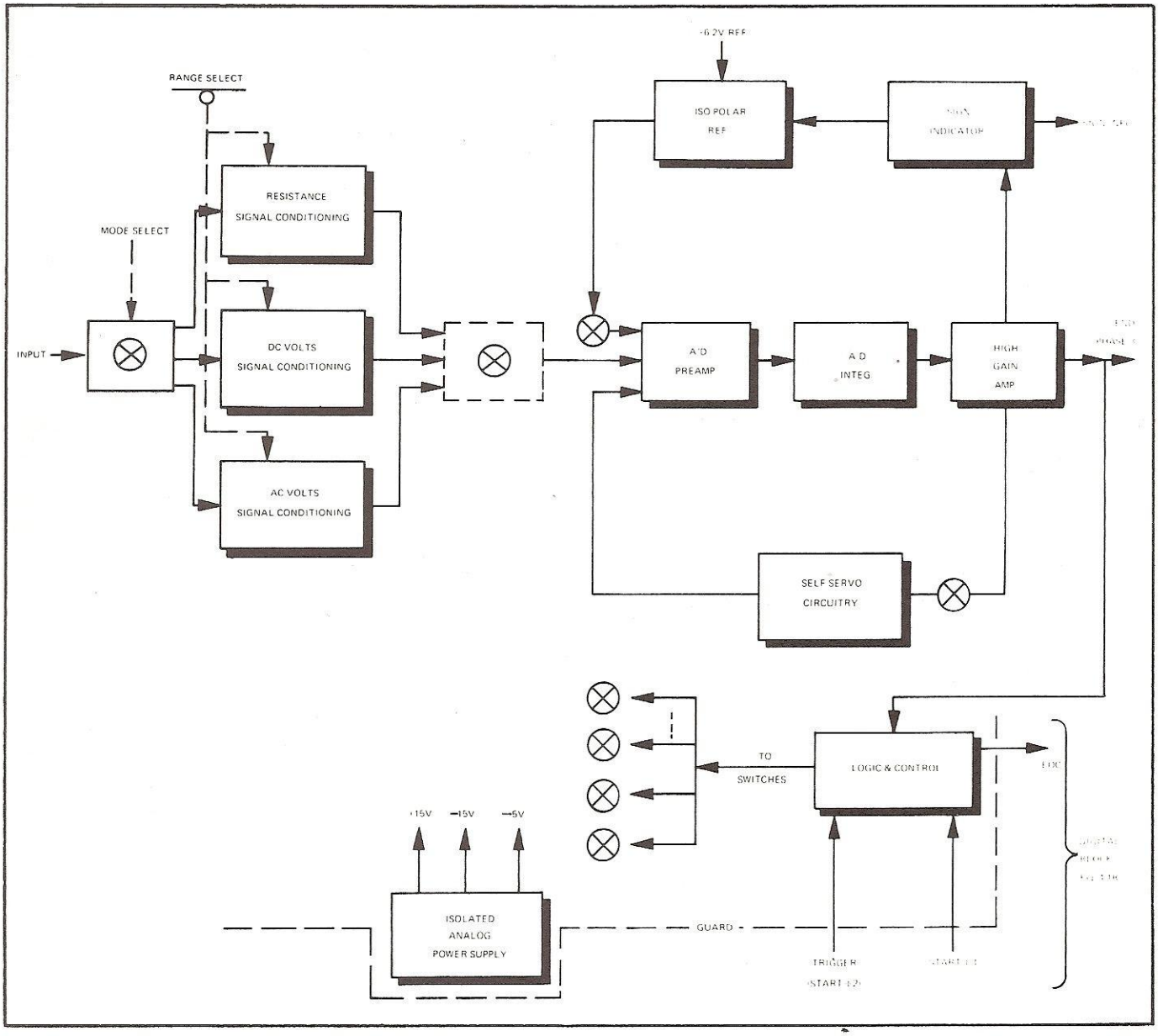


Figure 4-2. DMM Analog Block Diagram

circuitry in the Analog Block Diagram receive transformer-coupled "trigger" and "start-phase 3" pulses from the Digital Blocks to initiate phase 2 and phase 3 Converter action, respectively, in each conversion cycle and develop end of conversion pulses to be transmitted via transformer coupling to the Digital Blocks to end phase 3. An isolated and triple-shielded Analog Power Supply furnishing ±15V and -5V completes the DMM Analog Block section.

In the Digital Block Diagram (Figure 4-3), the Trigger Block generates a control pulse (from its own internal timing circuitry or from external command) as the "start convert" command to the Enable FF. If not blocked by the External Enable signal, the Enable FF gate permits the Crystal Clock pulses to drive the Decade Counter Chain block to start phase 2 operation. At 100000 counts (end of phase 2) a carry pulse (10^5 CARRY) is transmitted to the Analog Block to start phase 3, while the decade chain continues its counting. When an EOC pulse is received from the Analog Block, the digital control block applies a stop command to the Enable FF stopping the count. At the same time, the Control Block generates a transfer command to enable the transfer from the Counter to the Latches, Decoders, and Drivers, updating the NIXIE™ display. The updated count (at end of conversion) is held in the Latch and the Display until the next update and is also available as BCD output from the Latch Block for remote data output applications.

The Range Select Block is driven by one of three sources: manual range selection, remote range selection, or (when in auto range) a command developed when the range of a particular conversion results in a phase 3 count of less than 10,000 or more than 119,999.

Paragraphs that follow now trace the signal through the functional blocks of Figures 4-1, 4-2, and 4-3.

4.3 SIGNAL CONDITIONING BLOCK

Figure 4-2

An input signal to be measured is introduced into the Signal Conditioning block where it is attenuated according to the range scale chosen, so that a normalized full scale value of ±1.0 volts DC is delivered to the A/D Converter Block. Overrange capability of 120% of full scale is obtained by accurate operation of the Signal Conditioning block to an output value of ±1.2 volts.

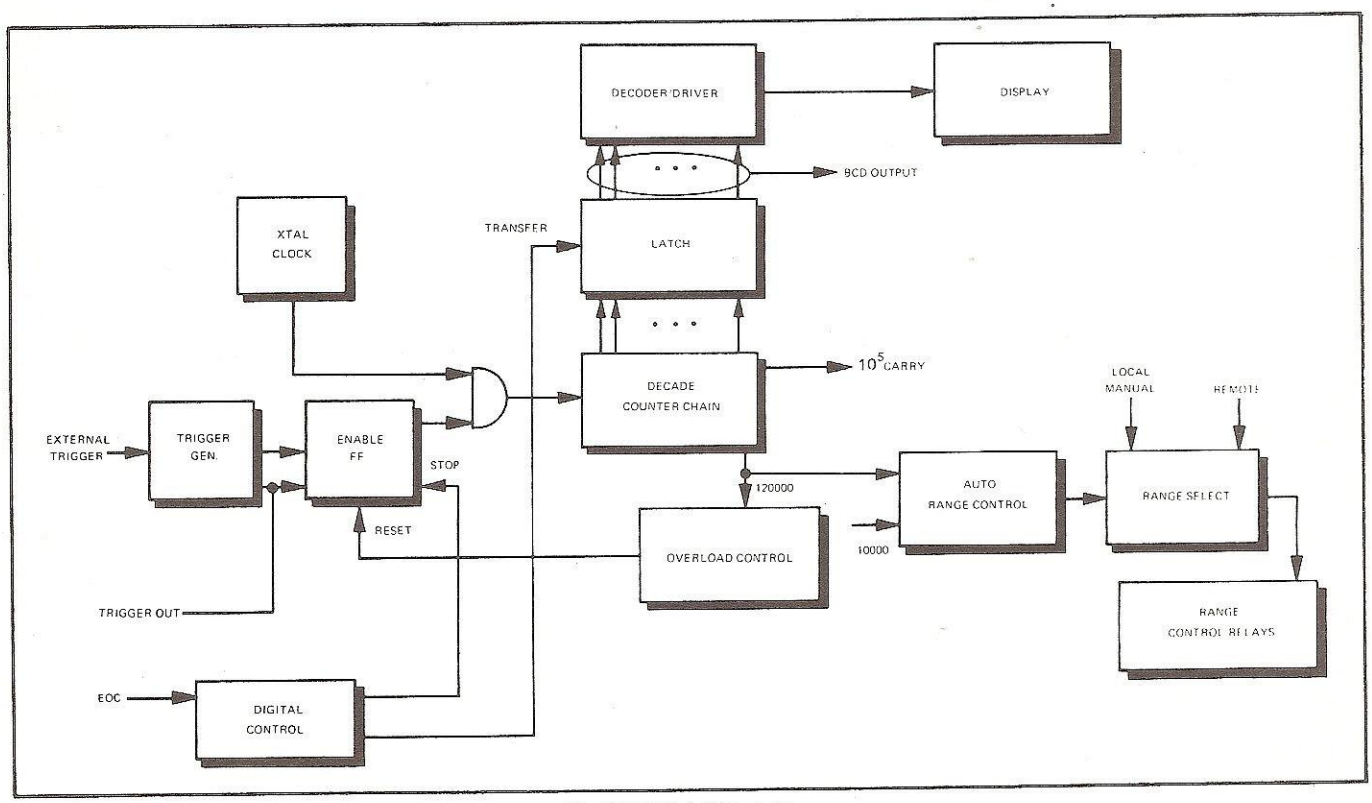
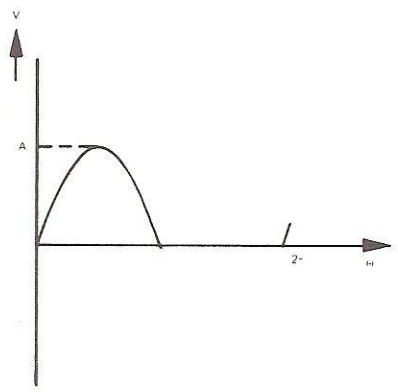


Figure 4-3. DMM Digital Block Diagram

Signal Conditioning of DC voltage inputs from ±1V to ±1000V full scale is accomplished by inserting appropriate attenuating factors for the selected full scale range. Signal conditioning in the 0.1V full scale (option) range is accomplished in the A/D Converter block.

For AC voltage inputs, the Signal Conditioning block rectifies and filters the input signal so that the output, a DC signal, represents the average value of the sine wave multiplied by the conversion factor of 2.22 to yield the RMS equivalent (Figure 4-4).



$$\text{AVG Value 1/2 SINE Wave} = \frac{1}{\pi}\int A \sin\theta\, d\theta$$

$$= \frac{A^2}{\pi}\left[-\cos\theta\right]_0^{\pi} = \frac{2A}{\pi}$$

$$= 0.318A$$

$$\text{RMS Value} = 0.707A$$

$$\text{RMS} = 2.22 \times \text{AVG Value}$$

Figure 4-4. RMS/AVG Scaling Constant

In the Ratiohmic™ resistance measurement technique, a voltage is connected across a range-selected accurately calibrated resistance in series with the unknown resistance, and the voltage drop across the unknown resistance is treated as an unknown DC voltage to be measured as before. In phase 3, however, the voltage drop across the calibrated resistance is used as the reference. Because the unknown and standard resistors are in series, the ratio of voltage drops is a direct measure of unknown resistance.

Attenuation components in the Signal Conditioning block are relay operated in response to control signals. These may be initiated by operating the front panel push buttons at the DMM, by control signals transmitted from a remote station via the rear panel connector, or by control signals generated within the DMM when in AUTO ranging.

4.4 TRI-PHASIC A/D CONVERTER BLOCK (Figure 4-2)

The three pahses of performance of the TRI-PHASIC A/D Converter are:

Phase 1: Accumulation and storage of offset

Phase 2: Integration of Input minus offset

Phase 3: Integration of Reference minus offset

In Phase 1 --

a. Inputs are disconnected from the A/D Converter;

b. Amplifier is clamped;

c. Long-term non-zero offsets are servo-accumulated and stored for later use;

d. Offset is updated continuously until the DMM phase 1 action ends in response to the trigger command.

In Phase 2--

a. Clamp is removed and input is connected to the amplifier;

b. Integration of input signal, algebraically reduced by the stored offset value, proceeds for 100 milliseconds as determined by Crystal Clock;

c. Result of the 100-millisecond integration appears as a voltage of the integrating capacitor.

In Phase 3--

a. Input is disconnected from A/D;

b. Voltage of opposite polarity is selected from ISO-Polar reference, algebraically reduced by value of stored offset, and the difference integrated to discharge the integrating capacitor linearly to zero;

c. At the zero crossover, end of conversion is generated, and transmitted to digital control circuitry.

4.5 TRIGGER GENERATOR AND CLOCK (Digital Block Diagram, Figure 4-3)

Primary control for DMM measurement is the trigger which initiates each conversion (start of phase 2). The trigger, in its internal DMM circuitry, is generated by the discharge of a neon tube after an RC path charges a capacitor to the neon tube break-down voltage. The trigger is factory selected for a pulse repetition rate of approximately 3 per second.

The trigger may be blocked and a conversion cycle delayed indefinitely by grounding the ENABLE input for as long as

desired. The display, or BCD equivalent, is held until a new trigger is generated. In addition, each conversion may be remotely triggered from an external source by a circuit which is activated when all front panel range select push buttons are in the OUT position.

4.6 DECADE COUNTER CHAIN, LATCH, AND DECODER (Digital Block Diagram)

The decade counter chain, latch, and decoder are composed of monolithic IC units (one for each of five decimal digits in each of the counter, latch, and decoder blocks) under control of digital control flip flops.

During phase 2, the counter fills up to 99,999, and the 5th decade carry pulse switches the actions of the Analog block from phase 2 to phase 3 operations.

During phase 3, the counter continues counting until it is stopped by digital control initiated by the EOC (end of conversion) pulse from the A/D Converter block.

The digital control also enables the transfer from decade counter chain to the Latch which acts as an isolating circuit and storage memory. The BCD data are connected to decoder drivers where they activate appropriate decimal lines in the NIXIE tubes.

4.7 RANGING (Digital Block Diagram)

Range scaling is accomplished by relays which may be activated in any one of three ways:

a. Manually - by pushing front panel range select push buttons;

b. Automatically - by digital logic control. When in AUTO Range, if the counter reaches a count of 120000 in phase 3, the AUTO Range control flip flop transmits a level output that selects the highest range possible (according to the DMM model configuration) and for subsequent conversion of less than 10000 counts steps down the selection one range step at a time to the range scale of the maximum resolution;

c. Remotely - when in remote trigger control, a discrete range scale may be selected, by grounding directly, or by a logic low level command.

4.8 POWER SUPPLY BLOCK

The Power Supply block may be connected for either a 115-volt or 230-volt AC Source of frequency from 47 to 420 Hz. The block is essentially two separate sets of supplies, driven from the same input transformer primary. The analog supply is triple shielded, floating, and incorporated in a "guarded" area for proper isolation. It develops ±15V regulated supply voltage for the analog circcircuitry, -5V for the digital control in this section, and develops the 6.2 volt, oven controlled, extremely low temperature coefficient, reference source for the A/D Converter. Common ground for the precise reference is used as the high voltage for the isolated digital control section, where the low voltage level is the -5 volts.

The transformer primary drives three additional secondaries whose outputs are rectified and provide +20 volts for relay operation, +180 volts for NIXIE tube operation, and a regulated +5 volts for digital logic. These appear in the digital section of the converter and use the digital ground as their return.

4.9 DETAILED OPERATION

A more complete function diagram of the multimeter is illustrated in Figure 4-5. The major blocks comprising the unit are divided into subunits or are repeated to indicate the several functions performed sequentially by the block, and this division forms a basis for complete systems understanding, detailed circuit explanation, and maintenance. Complete schematics, from which simplified schematics and block diagrams have been derived, are contained in Section 6 and are prepared as fold-outs for convenient reference when reading the following text.

The sequence of functions illustrated in Figure 4-5 consists of the following:

1. Operating mode and Full Scale Range are selected. Proper attenuation elements for the selected range are connected in the Signal Conditioning block.
2. Input signal is applied.
3. Prior to the trigger pulse starting a conversion measurement, the A/D Converter input is clamped, and the Signal Conditioning output is removed from the A/D Converter. During that time, phase 1 drift integration proceeds and the self zeroing circuit determines the A/D amplifier accumulated drift and stores it for phase 2 and phase 3 operation.
4. Following the trigger pulse generated in the Timing & Control unit;
   a) The clamp is removed from the A/D Converter.
   b) The Signal Conditioner Output is connected to the input of the A/D Converter.
   c) The self-zeroed drift is introduced as an algebraic negative offset.

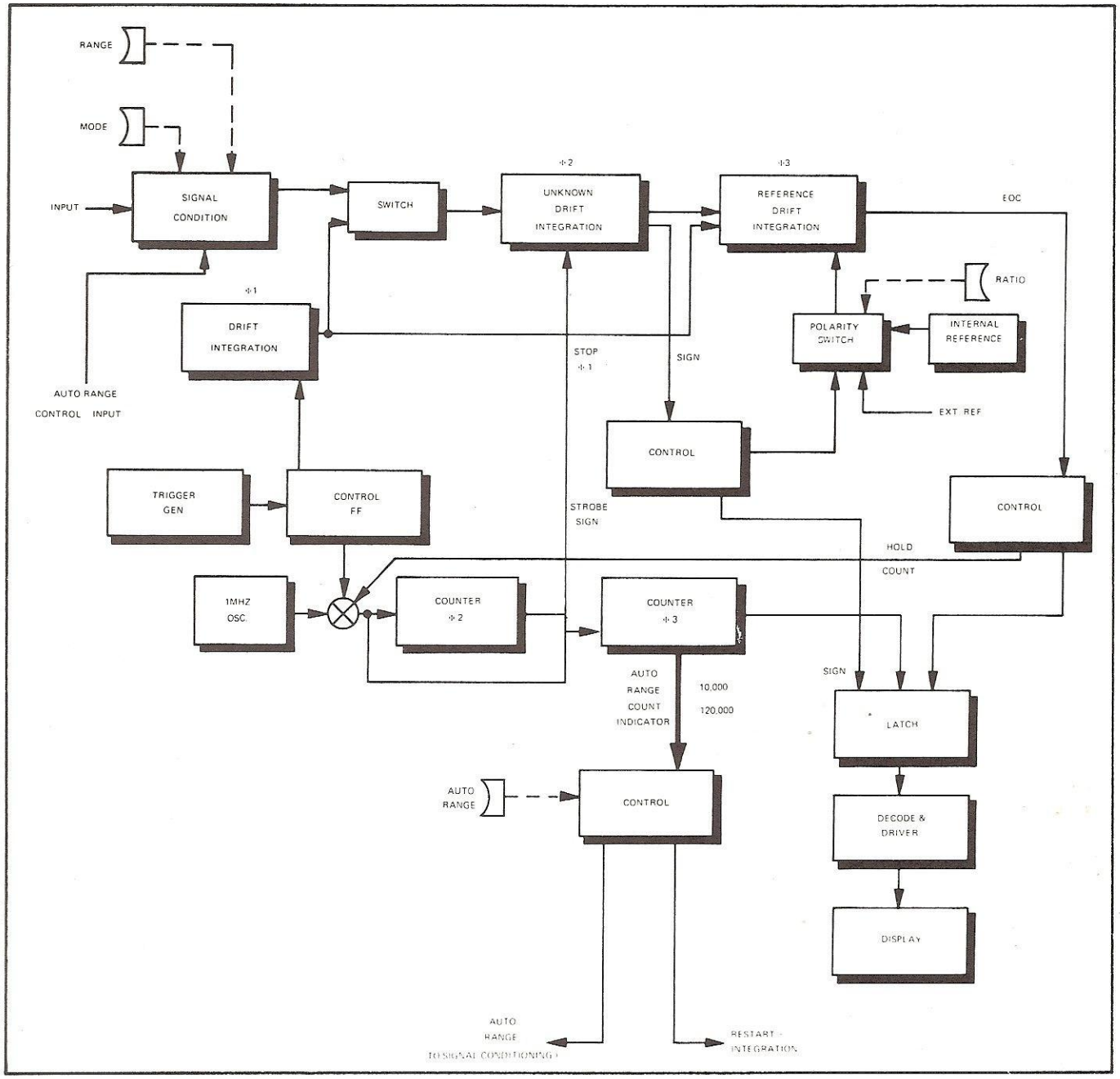


Figure 4-5. DMM Functional System Block Diagram

d) The counter is reset to zero and starts its fixed count for the phase 2 integraton.

5. When the count has reached 100000 (100 millisec.),

a) The second integration is stopped.

b) The sign of the input is interrogated by strobing the integrator output.

c) The unknown signal input is removed from the integrator.

d) The appropriate polarity of internal reference voltage is applied to the A/D input.

e) The reference voltage reduced algebraically by the stored drift (as in phase 2) is integrated during phase 3 integration.

6. When the integrated reference compensates the integrated unknown input (when the output of the integration returns to the starting point),

a) Phase 3 integration process ends.

b) The input clamp is re-established.

c) The clock input to the counter is stopped.

d) A READ OUT signal is transmitted indicating End of Conversion.

e) The accumulated count is transferred to the display.

The timing sequence is illustrated in the chart of Figure 4-6, indicating the three phases of the operation.

Detailed explanations of these functions are presented in the following sequence:

a. Input signal conditioning.

b. Phase 1 Drift Integration.

c. Phase 2 Unknown-Drift Integration.

d. Phase 3 Reference-Drift Integration.

e. Digital Control and Display.

f. Ranging circuits and Remote display and control functions.

4.10 SIGNAL CONDITIONING DETAILS

a. DC Voltage

Input DC voltages are applied through the HI and LO input terminal, and connected to the input attenuator network through the contacts of Mode Switch S12 and S13 when placed in DC Volts Mode. Relay actions of K1 and K2, determined by the range selection, then establish the attenuator actions.

A simplified schematic of the DC Voltage Signal Conditioning action is shown in Figure 4-7.

The relay pair (K1A and K1B) and relay K2A provide four range selections from 1V Full Scale to 1000V Full Scale. (Range change from 1.0V to 0.1V Full Scale is accomplished in the A/D Converter.) Action of the relays and resultant attenuation of the input signal

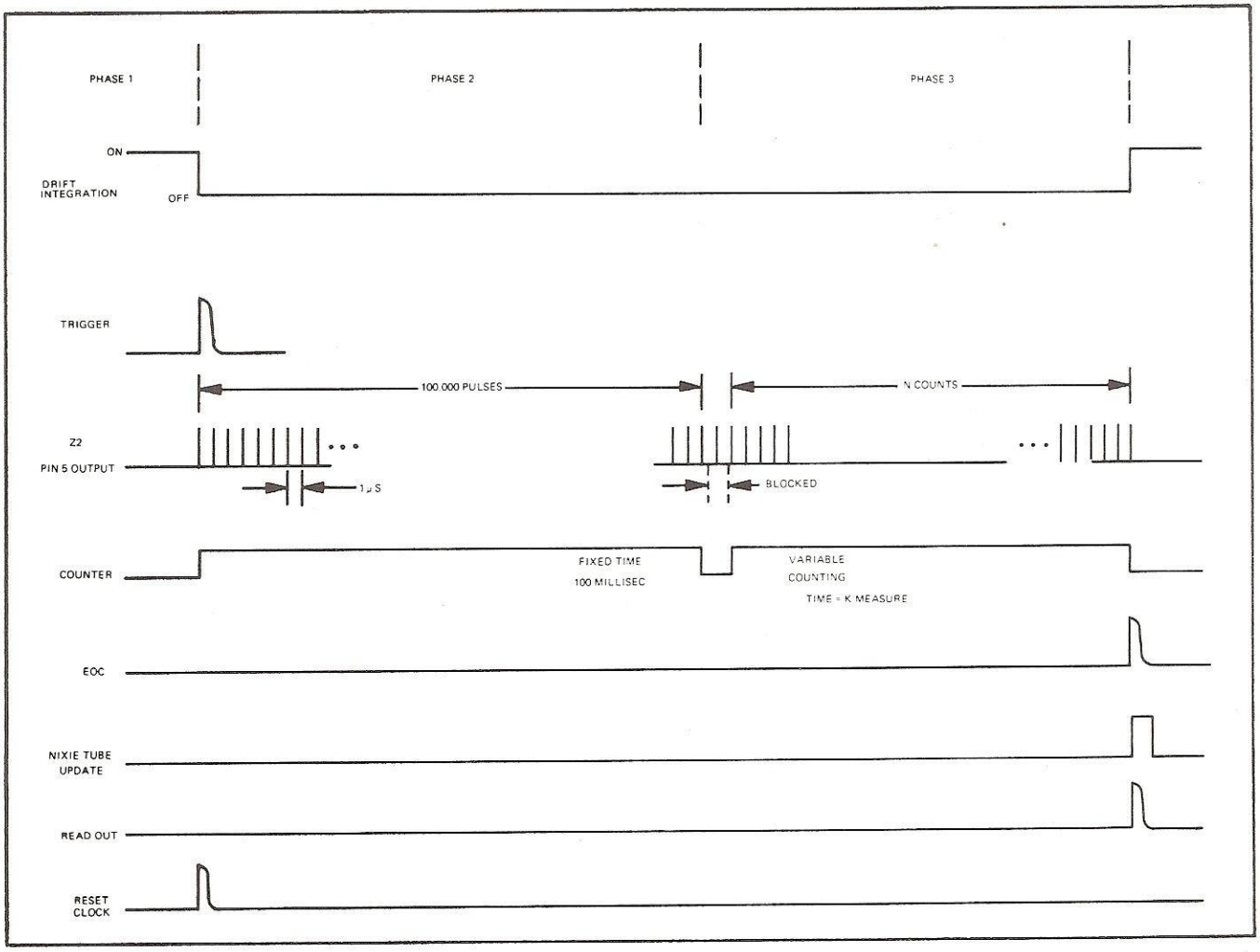


Figure 4-6. DMM System Timing Diagram

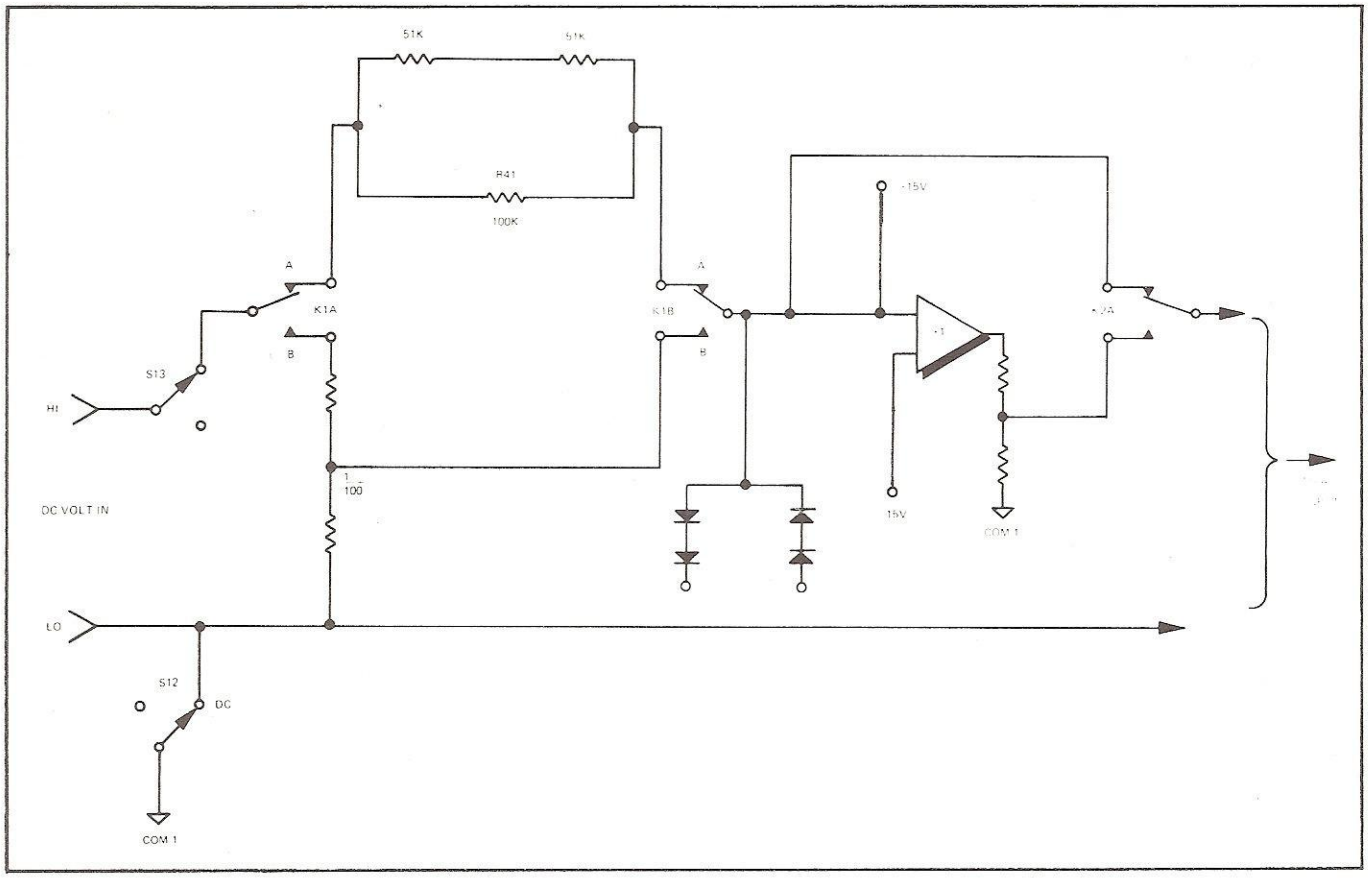


Figure 4-7. DC Voltage Signal Conditioning Simplified Schematic

on the different range scales are summarized by the table below.

Full Scale Range Select.	Relay K1 1/100	Relay K2 1/10	Result. Atten.
1 Volt	OFF	OFF	1
10 Volts	OFF	ON	1/10
100 Volts	ON	OFF	1/100
1000 Volts	ON	ON	1/1000

Full scale voltage delivered to the A/D Converter is 1 volt on all ranges except the 0.1 Volt scale. In that range the full scale output of the Signal Conditioning block is 0.1 volt. In all cases, overrange values, up to 120% of full scale are converted accurately in the A/D Converter, up to a maximum input of 1000 volts DC.

The signal conditioner amplifier is a high impedance, unity gain, isolation unit, provided with voltage and current offset adjustments. It is connected only when relay K2 is activated. The input network, including R41 and the biasing diodes, is designed to protect the Multimeter from accidental connection of high voltages up to ±1000 volts regardless of the range selector setting.

When not in DC Volt Measurement Mode, the input is removed from the indicated circuitry.

b. AC Voltage

In AC Voltage Mode, the input is connected to a broad band active attenuator followed by an active rectifier and filter. Networks in the feedback path of the input amplifier determine the attenuation for the selected full scale range. Capacitor trimmers are adjusted to maintain constant feedback ratios over the range of input signal frequencies. Manual push button action or automatic ranging signals control the relay-operated selection of the appropriate attenuation decade. A simplified schematic of the circuit is shown in Figure 4-8. This illustrates the amplifier and its feedback decades, the half-wave rectification of the second amplifier output, and the low pass filter which passes the average DC component of the rectified output.

The filtered, rectified DC Voltage output is scaled to the RMS value of the applied input signal and feeds the A/D Converter.

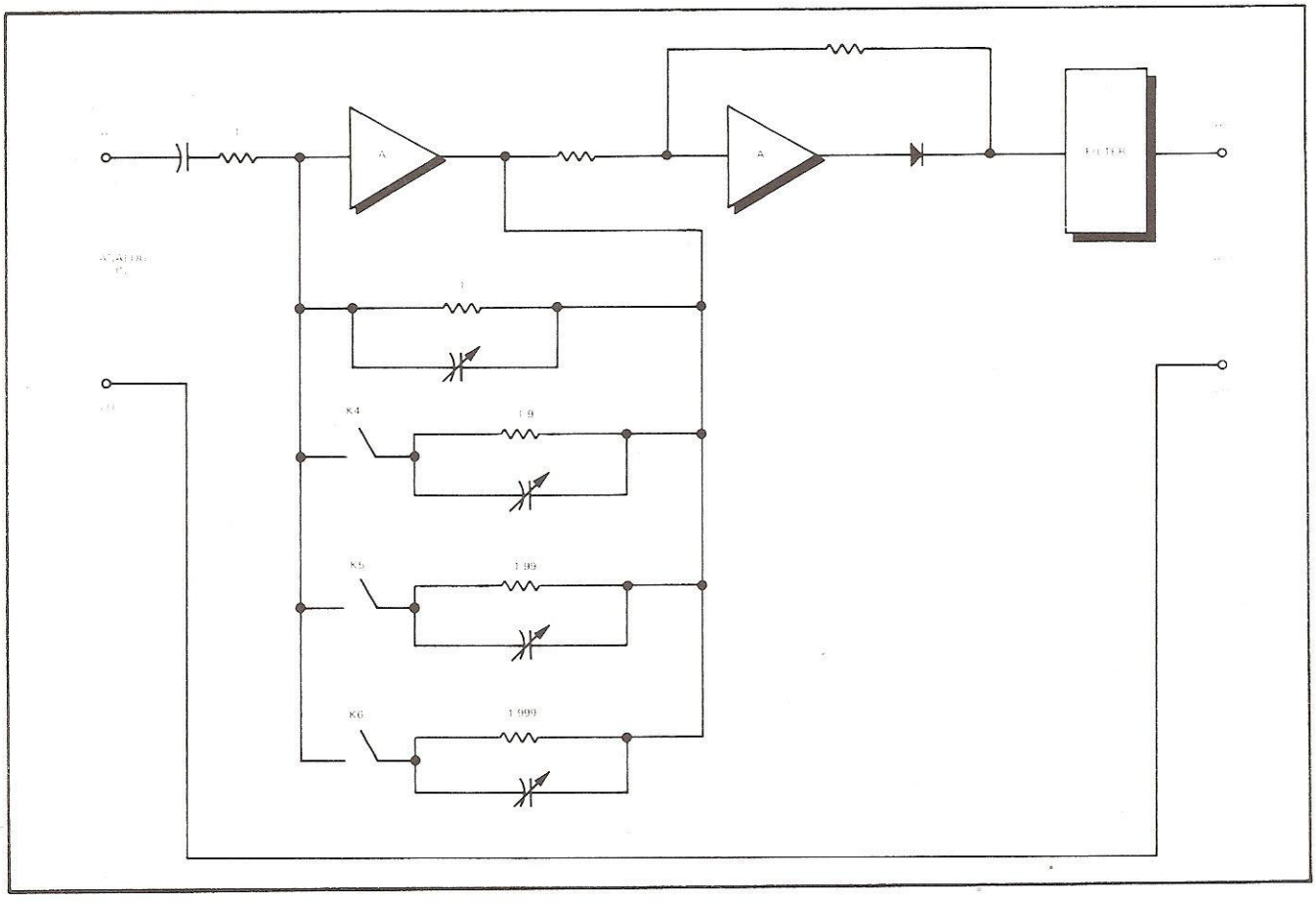


Figure 4-8. AC Voltage Signal Conditioning Simplified Schematic

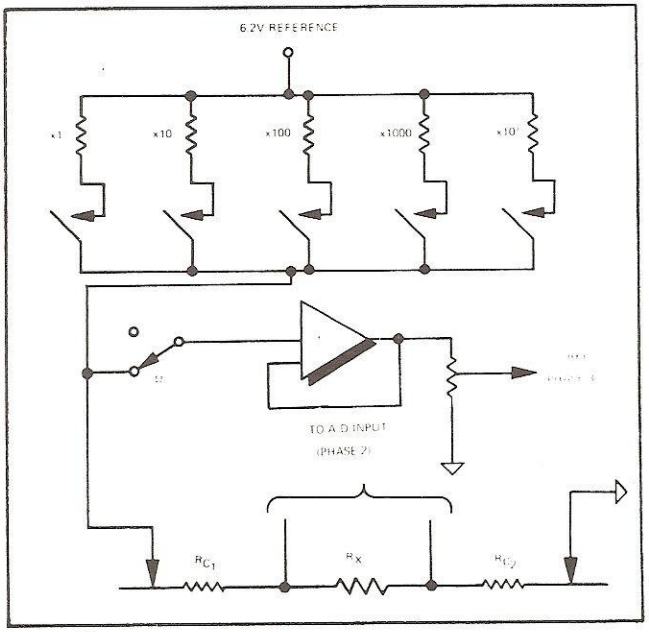


Figure 4-9.
Resistance Measurement Signal Conditioning Simplified Schematic

4.11 RATIOHMIC RESISTANCE INPUT CONDITIONING DETAILS

Connections for Resistance measurements are shown in the schematic of Figure 4-9. The unknown resistor is made part of a resistance series set consisting of a selected range scale resistor, the undetermined contact resistances Rc_1 and Rc_2, and itself. This set is driven from the temperature controlled +6.2V reference voltage. During phase 2, the voltage drop across Rx is connected to the A/D Converter where it is processed in the same manner as a DC input signal. During phase 3, the voltage drop across the selected range scale resistor is buffered by the unity gain amplifier, divided by 6.2 using the calibrated divider network, and connected to the converter as the Reference input.

The indicated circuit operation features the following:

a. The same current develops the unknown and reference voltage signals.

b. The contact resistance voltage drops do not affect performance.

4.12 A/D CONVERTER DETAILS

Operation of the Tri-Phasic A/D Converter in its 3 phases is described with the aid of simplified schematics of Figure 4-10A and Figure 4-10B, derived from the complete reference drawing in Section 6.

Referring to Figure 4-10A, during phase 1, switch Q1 is open, switches Q2, Q23, and Q25 are closed. Opening of Q1 removes the Signal Conditioned input from the A/D preamplifier A1. Closing of Q2 clamps the input to A1, and, with Q23, closes a path whereby C34 is charged from the ISO-Polar reference to 1 volt. Closing of Q25 permits capacitor C36 to store a charge compensating for the accumulated non-zero offset in A1, A2, and Z29.

Appearance of the trigger pulse in the secondary of transformer L2 (Figure 4-10B) signals the start of phase 2, and initiates the control actions by flip flop Z31A. The trigger causes pin 5 to go high and consequently Q1 to close. The output Z31A pin 8 goes low, and consequently opens transistor switches Q2, Q23, and Q25.

a. Opening Q23 opens the charging path to C34 (Figure 4-10A) and leaves C34 charged to 1 volt and isolated during phase 2.

b. Opening Q25 opens the charging path of C36 and leaves it charged with the accumulated compensation for zero drift applied to the input of the differential integrating amplifier A2.

c. Closing Q1 connects the Signal Conditioned output to the A/D Converter input.

Phase 2 integration action takes place in the chain of three active elements: amplifier A1, amplifier A2, and amplifier Z29. Amplifier A1 is a high gain, high input impedance, low offset amplifier whose feedback resistors R93 and R94 determine the closed loop gain.

The output of amplifier A1 is one input to integrating amplifier A2 whose integration constant is determined by C35 and R95. The other input to amplifier A2 is the voltage on C35, the stored value of the voltage compensating for the accumulated zero offset derived in phase 1.

Output of amplifier A2 drives high gain amplifier Z29 to saturation during phase 2. Its output polarity is used to indicate the sign of the unknown input.

Phase 2 integration proceeds until the appearance across the secondary of L4 of a positive-going pulse signalling a 10^5 carry from the digital block. This now appears as a negative pulse clocking flip flop Z30A pin 2 and as a direct set for flip flop Z31A (pin 4). The resulting actions controlled by these flip flops initiate the phase 3 operation of the A/D Converter.

The output, pin 5, of Z31A, which had been high from the start of phase 2, now goes low opening Q1 thereby removing the signal input from the A/D amplifier. Action of flip flop Z30A in response to the clocking pulse depends upon its input conditions just prior to receiving that pulse. This in turn was determined by the output of amplifier Z29 during phase 2. Amplifier Z29 was driven to saturation in the positive or negative direction corresponding to the sign of the input signal.

If the input signal had been positive, Z30A pin 11 would have been low and the clocking pulse would not have changed the high level at pin 6, thus producing no pulse across the primary of "sign" pulse transformer L5. If the input signal had been negative, Z30A pin 11 would have been high and the clocking pulse would cause Z30A pin 6 to go low producing a pulse across the transformer L5 primary and transmitting a negative sign indication to the Digital circuitry. The voltage level developed by flip flop Z30 at pin 9 controls the sign of the reference signal to be switched to the amplifier input at the start of phase 3. (Refer to Figure 4-11 in conjunction with Figure 4-10B.)

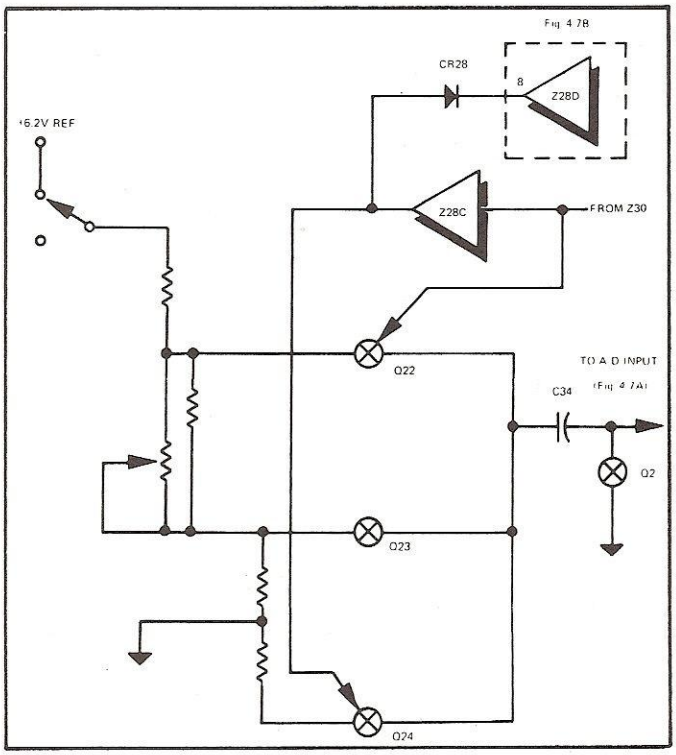


Figure 4-11. ISO-Polar Reference Switching Simplified Schematic

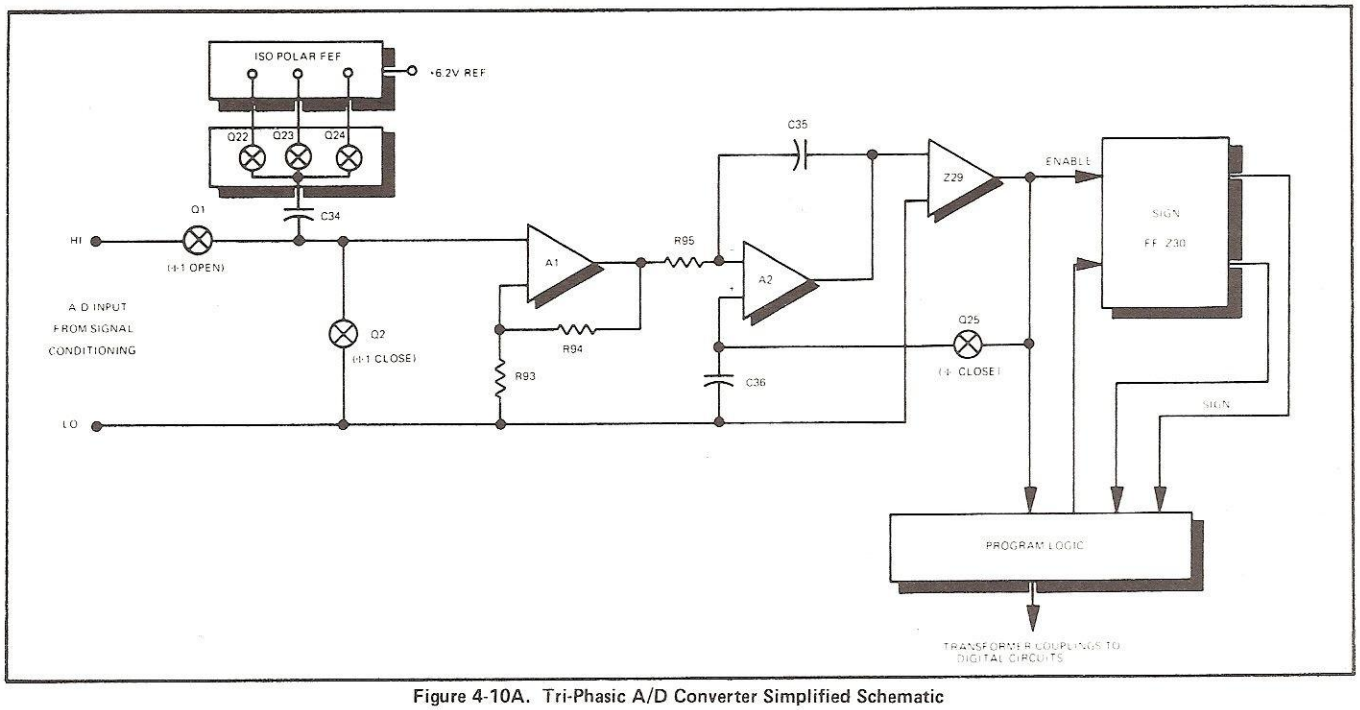


Figure 4-10A. Tri-Phasic A/D Converter Simplified Schematic

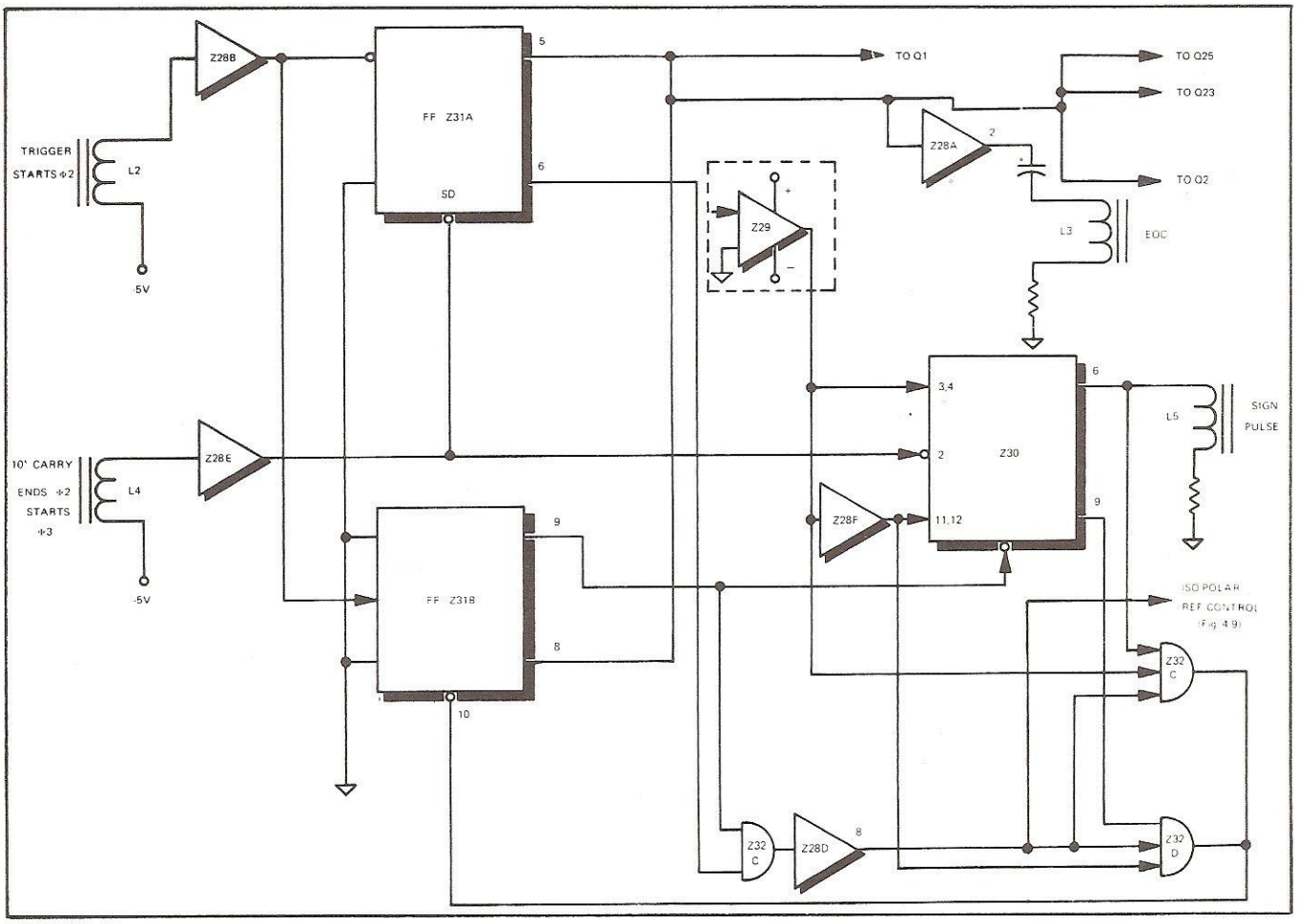


Figure 4-10B. Tri-Phasic A/D Converter Control Simplified Schematic

During phase 2, both Q22 and Q24 are open. The low level output at Z30 pin 9 had kept Q22 open; and the output of Z28 pin 6 had been clamped low through CR28 to Z28D, keeping Q24 open. If the input signal had been positive, Z30 pin 9 would have remained low, keeping Q22 open. The carry pulse control action removes the clamp on the Z28 pin 6 output permitting the output of Z28 pin 6 to go high, closing Q24. This action places the high side of C34 at reference zero potential and negative one volt at the A/D amplifier input. If the input signal had been negative, Z30 pin 9 would go high, closing Q22 and connecting the high side of C34 to reference +2V causing a positive one volt at the A/D amplifier input.

Control actions for the end of conversion (end of phase 3) are initiated by the zero crossing of the Z29 output, sensed by the gating action of Z32C and Z32D, and developed in digital control flip flops Z31. At each gate Z32C and Z32D, two of the three inputs are high during phase 3. As the output of Z29 crosses zero in either direction, one of these gates is enabled and develops the negative direct set pulse at flip flop Z31 pin 10. The Z31D output goes high, is inverted by Z28A, and develops a pulse across EOC transformer primary, signalling end of conversion to the digital circuitry. The Z31D output also controls the resetting of A/D converter to phase 1 operation. It --

a. Closes Q25
b. Closes Q2
c. Clamps Z28 pin 6; opens Q24
d. Direct sets Z30; opens Q22
e. Closes Q23
f. Opens Q1.

In summarizing the actions of the A/D converter circuitry during the three phases of operation, the levels and signals of the gates, flip flops, etc. are tabulated below.

LOGIC LEVELS

ACTION	COIL	PIN	LEVEL
INITIAL CONDITIONS Ø1	Z31	1	High
		2	High
		4	High
		5	Low
		6	High
		8	High
		9	Low
		10	High
	Z30	10	Low
		3	High
		6	High
		9	Low
		11	Low
	Q1		Open
	Q2		Closed
	Q22		Open
	Q23		Closed
	Q24		Open
	Q25		Closed
	Z28	8	Low
Ø2 STARTS WITH POSITIVE PULSE THROUGH L2	Z31	1	Clock pulse
		13	Clock pulse
		5	High
		6	Low
		8	Low
		9	High
	Z30	10	High
	Z28	8	Low
	Q1		Closed
	Q2		Open
	Q22		Open
	Q23		Open
	Q24		Open
	Q25		Open
Ø3 STARTS WITH CARRY PULSE THROUGH L4	Z31	4	Neg. pulse
		6	High
		5	Low
	Z30	2	Clock pulse
		3	High if input pos. Low if input neg.
		11	Low if input pos. High if input neg.
		6	High if input pos. Low if input neg.
		9	Low if input pos. High if input neg.

4.13 TRIGGER GENERATOR AND COUNTER

a. Trigger Generation

The trigger pulse initiating each conversion process may originate either from an external source or from internal circuitry shown in the simplified form of Figure 4-12. Capacitor C1 charges toward 180V through R14 until the firing voltage of DS8 is reached. The DS8 neon gap breaks down, and a pulse approximately 100 usec wide and 4 volts magnitude is developed across R16 and connected to the SET ENABLE input of the control flip flop (Z2 pin 2). The sawtooth charge-discharge signal at the junction of R15 and DS8 and resulting trigger timing signal across R16 are also included in Figure 4-12.

LOGIC LEVELS(cont.)

ACTION	COMP	PIN	LEVEL
	L5		Pulse if input neg. No pulse if input pos.
	Z28	8	High
	Q1		Open
	Q2		Open
	Q22		Closed if input neg. Open if input pos.
	Q23		Open
	Q24		Open if input neg. Closed if input pos.
	Q25		Open
END OF Ø3; Z29 PIN 7 CROSSES ZERO	Z32	6 or 8	Goes neg. pulse
	Z31	10	Low
		8	High
		9	Low

LOGIC LEVELS (Cont.)

ACTION	COMP	PIN	LEVEL
	Z30	10	Low
		6	High
END OF CONVERSION; NEGATIVE PULSE THROUGH L3		9	Low
	Z32	8	High
		6	High
	Z28	8	Low
	Q1		Open
	Q2		Closed
	Q22		Open
	Q23		Closed
	Q24		Open
	Q25		Closed
RETURNING TO Ø1 OPERATION			

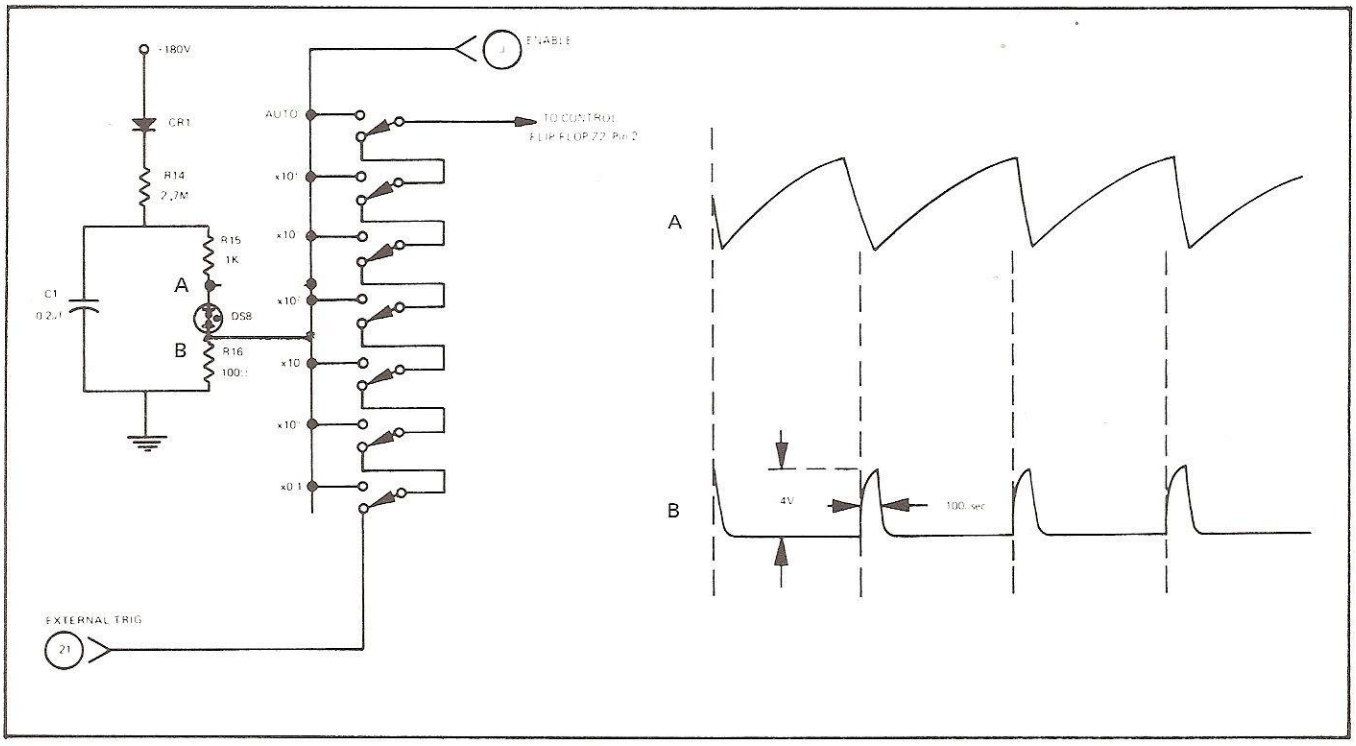


Figure 4-12. Trigger Generator Simplified Schematic and Waveforms

Non activation of all of the ranging push buttons disconnects this signal (Manual or Automatic) and permits an external trigger pulse to be connected to the DMM flip flop circuitry. If desired, the internal trigger generator may also be used during remote control of the DMM by connecting the output ENABLE of rear panel connector, tab J, to the EXTERNAL TRIGGER input, tab 21.

With the trigger pulse enabling Z2A, the next clock pulse toggles Z2. Pin 5 goes high and pin 6 goes low providing a control output with the following results:

1. After inversion through Z3 pin 3, transistor Q5 conducts; its collector goes low isolating the latching circuit from the counter. The latch and display retain the stored count until the next conversion update, and an output signal, READOUT, is available at the rear panel connector to indicate this event in the cycle. This is a High (T^2L/DTL) output level between conversions.

2. The leading edge of the negative going waveform is differentiated (C5, CR20, and R21) as the input to Z1 (pin 13), inverted, and generates a positive going pulse to reset the decade counter IC's, Z4 through Z8.

3. The inverted counter reset pulse, at the output of Z1 (pin 10) presets the control flip flops Z20 pin 10 and pin 4, and Z2 pin 10.

4. Z3 pin 4 is enabled, allowing the clock to drive the counter.

b. Counter Chain

The crystal-controlled clock is a series-mode crystal circuit consisting of crystal Y1 and inverter Z1. It develops 1 MHz pulses which are gated into the counter during phases 2 and 3. The counter registers accumulate the count during phases 2 and 3 until receipt of the EOC (End of Conversion) pulse at the EOC transformer secondary. This resets flip flop Z2, and pin 5 goes low, blocking the timing pulses at gate Z3 (4, 5, 6). Simultaneously, Z2 pin 6 goes high cutting off Q5, collector voltage goes high, permitting the count in Z4-Z8 and Z2 to be transferred to the latches, and through them to the decoding and display driving registers Z15 and Z19.

Outputs of the counter chain are transferred through the latching registers as BCD data. These are immediately available at the tab connector of the DMM rear panel for remote display or control purposes. In the DMM, the decoding registers Z15 through Z19 convert BCD to decimal signals for their respective NIXIE tubes.

If the DMM is in a manual range selection, and the developed count in phase 3 is less than 120,000, the conversion cycle is complete.

c. Overload

If an end of conversion pulse is not received during phase 3 by the time the counter reaches 120000 (a display of 120000), an OVERLOAD condition exists, and this event is sensed at gate Z3. One input to Z3 (pin 9) is set at a high level by the toggled output of Z20 pin 5 when the count reaches 10^5 in phase 3. When the counter reaches 20000, the second input to Z8 (pin 10) goes high and activates the gate. The gate output, Z3 pin 8 is a negative waveform, available atrear panel connection, pin Y, as an OVERLOAD indicating signal for remote transmission. The overload indicating negative level also is connected at the output of Z1 pin 2 and acts in the same way as the EOC pulse from the Analog Circuitry through Z11 pin 2 as a direct set for flip flop Z2 pin 4.

The overload condition, generating high levels of 10^5 and 2×10^4, back bias CR47 and CR46, respectively, and the combined action cuts off transistor Q2 to turn off the digit indicator (MSD-1) of the most significant digit in display tube DS2. At the start of the next conversion cycle, when the counter is reset, the back bias levels are removed, and the display responds to the 10^5 count to turn DS2 on during the conversion. Thus, the most significant digit blinks as a result of successive overload conditions.

d. Sign

DS1 is the display unit for the sign indication. It is enabled in DC mode only, and is turned on by the action of the sign pulse transformer L5 output via latch flip flops Z14, and strobed into first latch at carry pulse and transferred to second latch at EOC.

4.14 RANGING (Figure 6-4, Drawing 35-1003)

a. Manual Control

All range selections are controlled by the acitons of Relays K1 through K6, and decimal point selection is slaved to the relay acitons. Each relay activation is controlled by a switching transistor (Q12, Q13, Q14, or Q15) driven by its inverter Z24 pins 2, 4, 6, or 8. The truth table included in the reference detail schematic of Section 6 relates the relay actions for each full scale range selection. In manual ranging, grounding the appropriate line via the switch at the front panel, either by grounding the line, or by applying a logical zero at a remote station, operates the required relays via the appropriate inverter, for each selected range.

Selection of the highest range x 10^4 (for resistance measurement only) biases off all transistor switches Q12 through Q14, and satisfies the truth table conditions for that range.

b. Auto-Ranging

The non-Automatic position of the S7 switch (for Manual Mode) disables the control flip flops Z21 and Z22, A and B, gates Z23, and inverter Z24 (pin 12). The circuitry is enabled when switching to Auto Range, lifting the ground and operating in response to control signals through gates Z21 (pins 3 and 6).

Voltage Auto Ranging

Either of two events causes the Auto Ranging circuit to change its full scale range:

1. An overload indicated by count of 120000 sensed at gate Z21 pin 3;
2. An underrange, indicated by a count under 10000 at end of conversion, sensed at gate Z21 pin 6.

In either event, the gate output is negative going.

Overload

At the overload voltage event, the negative going action of gate Z21 pin 3 acts as a direct set on flip flop Z22A and Z22B. The flip flop outputs apply enabling levels to gate Z23 pins 12 and 13, and cause the output at pin 11 to go low, acting to select the highest voltage range, 10^3.

If the succeeding conversion results in an underrange condition, then, at the READ event, gate Z21 pin 6 is negative going and clocks both flip flops Z22A and Z22B resulting in the stepping of the range selection to the next lower range. The process is repeated, dictated by enabling levels at the flip flops, until the range of maximum resolution for the input signal is selected.

Resistance Measurement Auto Ranging

When in auto ranging during Resistance measurement mode, the mode-switched circuitry disables transistor Q21 and lifts the clamp from flip flop Z21 pins 10 and 11. When an overrange condition is sensed by gate Z21 pin 3, its output causes Z21 pin 11 to go high; then through inverter, Z24, causes pin 12 to go low, producing the same result as closing switch S6A. This action results in the selection of the highest ohms measurement range scale (10^4).

In addition to controlling the relay selection for x 10^4 scale, the action disables flip flops Z22B for the next event by a negative level at pin 2 of flip flop Z22B, and a consequent negative level at pin 12 of Z22A. If an underrange condition should occur at a succeeding conversion, Z21 pin 6 output will not change the states of flip flop Z22A or Z22B. It will, however, set flip flop Z21 pin 8 high and pin 11 low, and through the inverter action of Z24 pin 12 activate Q11 and the x 10^3 range scale select relay. In addition, it will enable flip flop Z22A, and thereby establish the conditions for subsequent toggling response to the next sensing of underrange conditions in the same manner as for voltage measurement auto ranging.